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A W-band wideband power amplifier using out-of-phase divider in 0.13-μm SiGe BiCMOS

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Dear editor,

More and more researchers focus on millimeter-wave applications for the resourceful unlicensed or light licensed frequencies such as 60 GHz, E-band (71–76 GHz and 81–86 GHz) for high data-rate communications, and 77/79 GHz, 94 GHz, and 122 GHz for automotive radar and imaging applications. As an important component of the system, the power amplifier (PA) with a wide frequency range and high output power is beneficial to high data-rate communication and imaging applications [1]. Together with the advantages of low cost and high-level integration with baseband circuits, a silicon-based (CMOS and SiGe BiCMOS) wideband PA has been widely investigated [1–6]. Amplifiers with a conventional matching network could potentially cover a wide bandwidth [1,2]. To further improve output power, the differential amplifier has been studied using a transformer [3,4]. The transformer has the advantages of wideband frequency response, compact size, and innate DC blocking. In the millimeter-wave range, the parasitic capacitance of the transformer is significant, which would worsen the amplitude and phase balance performance of the transformer balun used for single-to-differential conversion. This in turn leads to deterioration in the power combination efficiency and bandwidth [3]. Apart from the transformer balun, the rat-race coupler [7] and LC balun [5] could also provide balanced differential outputs. However, these components have limited bandwidth and are relatively large. The Marchand balun [6,8] is also a good candidate with a wide bandwidth and is compact in size; however, its insertion loss is too high (2–3 dB loss) in power combination applications.

In this study, we developed a compact wideband out-of-phase divider with low insertion loss using a previously reported wideband phase inverter [7]. The proposed divider is applied in a W-band differential amplifier design for power dividing and combining. The amplifier achieves a bandwidth of 49 GHz from 75 to 124 GHz and an output power of 12 dBm.

Out-of-phase divider design. Figure 1(a) presents the proposed structure of the out-of-phase divider with the phase inverter. The phase inverter has been previously investigated [7], and is of compact size and with a $-90°$ phase delay in wideband frequencies in silicon-based processes. The phase inverter has also been applied in the 180° and 90° wideband coupler designs. By replacing one branch of the divider with the phase inverter ($-90°$) while keeping the other branch with a 90° delay line ($l_1 + l_2$), the two output ports (P2 and P3) have a 180° phase difference and the same amplitude. To match the input port (P1) to be 50 Ω, the characteristic impedance of the two branches should be 70.7 Ω (w = 19 μm with $-90°$ length and w_1 = 7 μm with 90° length). The electromagnetism simulation shows that the input return loss is better than 15 dB between 80 and 130 GHz. The

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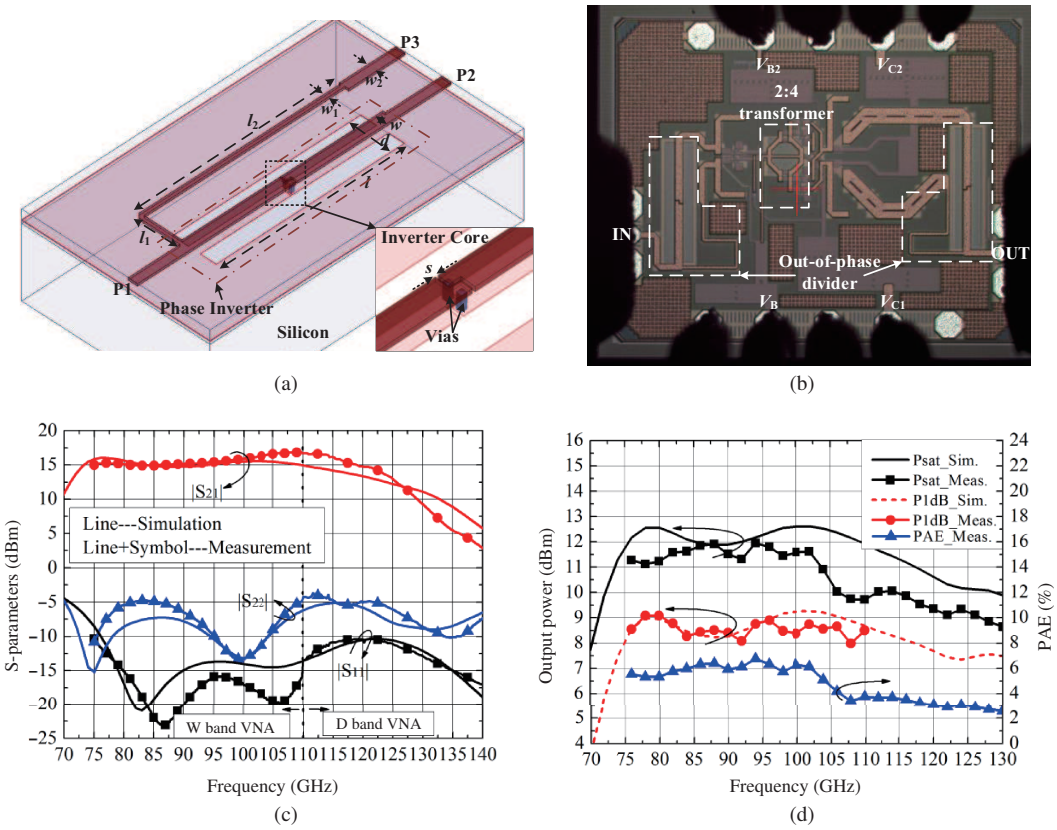

Figure 1 (Color online) (a) Structure of the out-of-phase divider with phase inverter. Dimensions: $l = 300$, $l_1 = 68$, $l_2 = 320$, $w = 19$, $w_1 = 7$, $w_2 = 15$, $d = 70$, $s = 2$, units: μm; (b) microphotograph of the amplifier; (c) simulated and measured S-parameters of the amplifier, under bias conditions of $V_B = 0.9$ V, $V_{B2} = 1.9$ V, $V_{C1} = V_{C2} = 3$ V, and $I_C = 64$ mA; (d) simulated and measured P1dB, Psat and PAE of the amplifier.

isolation between P2 and P3 is better than 6 dB. From 80 to 130 GHz, the amplitude imbalance of P2 and P3 is within ± 0.5 dB, and the phase imbalance is ± 10° with an insertion loss of 0.8 dB. The total size of the divider is only 120 μm × 330 μm. Compared with previously reported silicon-based rat-race couplers [7], the proposed divider has better bandwidth and is smaller in size. In addition, compared with the Marchand balun [8], the proposed divider has a lower insertion loss.

Wideband amplifier design. The out-of-phase divider was applied to the two-stage differential wideband amplifier design for power dividing in the input port and power combining in the output port. The amplifier has one cascode pair in the first stage and two cascode pairs in the second stage. All the transistors are equal in size, (0.84 × 0.12) μm × 8 μm. In the input stage, the L-shaped matching network is for wideband input matching. The two stages are interconnected using the 2-to-4 transformer splitter, which is realized with the top two metals for signals and the bottom metal for ground. The octagonal transformer splitter has a diameter of 80 μm and a metal width of 10 μm. In the output stage, the 4-way outputs are first classified into two channels (the in-phase outputs are grouped to one channel). The two channels are then connected to the two differential ports of the divider. The supply voltages V_{C1} and V_{C2} are set to be 3 V, as shown in Figure 1(b). The bias voltages V_B and V_{B2} are 0.9 V and 1.9 V, respectively, at the quiescent point, which yields optimum collector current density for the maximum operating frequency $f_{\max}$ condition. In the simulation, the amplifier is optimized for the tradeoff between the gain, output power, and bandwidth. The simulated results are shown in Figure 1(c) and (d). The gain is 15 dB and the 3-dB bandwidth is from 72 to 123 GHz. In the 3-dB bandwidth frequencies, the simulated saturated output power (Psat) is over 10 dBm with a peak value of 12.5 dBm.

To further investigate the bandwidth enhancement property of the proposed divider, the output stage of the amplifier has been replaced by the compact transformer balun for comparison. The amplifier with the transformer balun has also been matched for maximum output power. The simulation shows that, using the transformer balun, the amplifier achieved a peak gain and output power similar to that of the amplifier with the proposed

divider at 90 GHz; however, the gain bandwidth decreases from 52% to 34%. The output power bandwidth also reduces from 58% to 43%. Therefore, with the help of the wideband out-of-phase divider, the bandwidth performance of the amplifier has been dramatically improved.

Fabrication and measurement. The proposed amplifier is designed and fabricated using the 0.13-μm SiGe BiCMOS process featuring an f_T of 240 GHz and an $f_{\max}$ of 290 GHz. The microphoto of the amplifier is shown in Figure 1(b) with dimensions of 1 μm × 0.8 mm. For better layout placement, one branch of the divider is bent without performance deterioration. The S-parameters are measured using a Keysight vector network analyzer with a W-band (75–110 GHz) extender and a D-band (110–170 GHz) extender calibrated with the on-wafer LRRM standards. The power test setup involves a Keysight 8267D signal generator that is connected to W-band and D-band multiplier modules as signal sources, and W-band and D-band power sensors with a power meter for collecting the output signal. All results are based on on-wafer measurements.

Figure 1(c) shows the measured S-parameters of the amplifier in the W-band and D-band frequencies. Flat gain performance appears in the whole W band with the peak value of 16.8 dB at 110 GHz. The 3-dB gain bandwidth is over 49 GHz from 75 to 124 GHz (the lower point is limited by the test frequency limits) with relative bandwidth of over 49%. In the 3-dB frequency range, the input and output return losses are better than 10 dB and 5 dB, respectively. The measured and simulated results match well in the wideband frequencies. The output power of the amplifier has also been measured and is shown in Figure 1(d). The peak Psat is 12 dBm at 94 GHz and the corresponding power added efficiency (PAE) is 6.7%. The measured 3-dB bandwidth of the Psat is 51% from 75 to 126 GHz. In the W-band frequencies, the output P1dB is over 8 dBm. Due to the lack of a D-band variable attenuator, the input power could not be tuned and the P1dB in the D-band cannot be measured. The measured power exhibited similar performance as the simulation. Compared with the amplifiers using a transformer balun [3,4], the proposed amplifier occupies a larger area, but the bandwidth is dramatically improved. Using the out-of-phase divider, the amplifier achieved a better bandwidth while maintaining a comparative output power.

Conclusion. A W-band wideband PA using the 0.13 μm SiGe BiCMOS process was introduced in this study. To enhance the bandwidth, the compact wideband out-of-phase divider using a phase inverter was applied in the amplifier for power dividing and combining. The amplifier has a measured 3-dB small-signal bandwidth of 49 GHz centered at 100 GHz. The output power 3-dB bandwidth is also measured to be 51 GHz with a peak value of 12 dBm. The proposed amplifier has a promising bandwidth and an output power performance comparable with other silicon-based amplifiers in the W- and D-band frequencies.

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