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Analysis of delay from step response based on stretchable flexible interconnects

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Dear editor,

The interactive integration of humans and information demands stretchable and flexible electronic systems. A new type of electronic technology that was both portable and comfortable appeared in the early 1990s [1, 2] and gained widespread application [3, 4]. In recent years, flexible electronic technology has been applied and developed in many sectors leading to lifestyle changes globally.

In a flexible inorganic electronic system, the electrical properties of stretchable interconnects are affected by the strain on these interconnects. Signals take some time to be transmitted from one end of an interconnect to the other, causing a delay in signal transmission. This delay dramatically affects signal integrity as products reach smaller physical sizes and faster signal speeds. The shape of stretchable interconnects is similar to that of a serpentine line. As the distance between parallel strip lines decreases, the delay in a serpentine line decreases due to the effect of mutual inductance and can be much smaller than that in a straight line of the same length [5, 6]. For stretchable interconnects, crosstalk problems can occur between two symmetric segments in repeated units of the stretchable interconnects due to this special shape. The direction in which crosstalk noise leaps is the same as the original signal propagation direction. Therefore, compared with a straight interconnect of the same length, the noise-added signal in a stretchable interconnect arrives early. During the deformation of stretchable interconnects, parasitic parameters change as the shape changes, which affects the crosstalk noise and thereby varies the delay.

The flexible electronic design platform is used to analyze the delay associated with stretchable interconnects. The simulation for this analysis has three steps. First, the structure of the stretchable interconnect is defined in the platform and mechanical analysis is conducted to extract the associated deformation model in ANSYS. Second, the deformation model is imported into the ANSYS Q3D Extractor to extract the parasitic parameters and the Q3D model according to the shape of the three-dimensional structure. Finally, the required circuit is initialized and simulated in the Advanced Design System (ADS) to get the delay in stretchable interconnects in terms of the step response.

The Elmore model has become the most commonly used interconnect-delay model owing to its fast computing speed [5]. However, the Elmore delay model only considers the influences of resistance and capacitance [7]; hence, this model cannot describe the effects of deformation on the delay of stretchable interconnects. In flexible electronic systems, parasitic parameters of interconnects change during the stretching and bending process. Herein, based on the traditional delay model for electronic systems, a new delay model for stretchable interconnects is proposed to ana-

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lyze the delay of interconnects under various deformation conditions.

Figure 1(a) shows the equivalent circuit of stretchable interconnects used for the delay estimation tests. The parasitic resistance R hardly changes for the length, the width, and the thickness of the metal material remains nearly unchanged as the interconnects deform. The inductance L of the stretchable interconnect is smaller than the inductance of a straight interconnect of the same length because the magnetic field around the conductor is partially offset due to the shape of the stretchable interconnect, i.e., the inductance increases as the interconnect is stretched [8]. Similarly, as the bending angle increases, part of the magnetic field surrounding the two segments on both sides of the midpoint is canceled out and the inductance decreases. The parasitic capacitor C_{C}, which is affected by the surrounding medium and the conductor geometry, changes a little with deformation.

In the circuit for delay analysis shown in Figure 1(b), the driving gate is simulated as a voltage source including a certain internal resistance R_{S}, and the load is simulated as a capacitor C_{L}.

According to the relationship between the voltage across the stretchable interconnects and the current flowing through the interconnect in the delay analysis circuit, wherein the stretchable interconnects model is replaced by the equivalent circuit, the following complex-frequency domain-transfer function can be derived as

$$H(s)=\frac{1}{1+b_1 s+b_2 s^2}, \tag{1}$$

where

$$b_1=RC_{\mathrm{C}}+RC_{\mathrm{L}}+R_{\mathrm{S}}C_{\mathrm{C}}+R_{\mathrm{S}}C_{\mathrm{L}},$$
$$b_2=LC_{\mathrm{C}}+LC_{\mathrm{L}}.$$

As the voltage source is a step signal,

$$U_i(s)=\frac{V_i}{s}, \tag{2}$$

the output voltage can be expressed as

$$U_{\mathrm{o}}(s)=\frac{V_i}{s\left(1+b_1 s+b_2 s^2\right)}. \tag{3}$$

The case of a double pole when ${b_1}^2-4b_2=0$ rarely appears. Therefore, the poles of the output voltage can be either real or complex.

(a) In the case of single real poles, i.e., ${b_1}^2-4b_2>0$, the output response in the time domain is

$$u_{\mathrm{o}}(t)=V_i\left(1-\frac{s_2}{s_2-s_1}\mathrm{e}^{s_1 t}+\frac{s_1}{s_2-s_1}\mathrm{e}^{s_2 t}\right), \tag{4}$$

where the equation's roots are

$$s_1=\frac{-b_1+\sqrt{{b_1}^2-4b_2}}{2b_2},$$
$$s_2=\frac{-b_1-\sqrt{{b_1}^2-4b_2}}{2b_2}.$$

The magnitude of $|s_2|$ is greater than $|s_1|$, hence,

$$u_{\mathrm{o}}(t)\approx V_i\left(1-\frac{s_2}{s_2-s_1}\mathrm{e}^{s_1 t}\right). \tag{5}$$

The delay τ_d at a threshold λ can be obtained as

$$\lambda=1-\frac{s_2}{s_2-s_1}\mathrm{e}^{s_1\tau_d}. \tag{6}$$

When $\lambda=0.9$, the equation becomes

$$\tau_{0.9}=\frac{2b_2}{b_1-\sqrt{{b_1}^2-4b_2}}\cdot\ln\left[5\left(1+\frac{b_1}{\sqrt{{b_1}^2-4b_2}}\right)\right]. \tag{7}$$

(b) In the case of complex poles when ${b_1}^2-4b_2<0$, the output response is

$$u_{\mathrm{o}}(t)=V_i\left(1-\frac{\sqrt{\alpha^2+\beta^2}}{\beta}\mathrm{e}^{-\alpha t}\cdot\sin(\beta t+\rho)\right), \tag{8}$$

where

$$\alpha=\frac{b_1}{2b_2},\quad \beta=\frac{\sqrt{4b_2-{b_1}^2}}{2b_2},\quad \rho=\tan^{-1}\left(\frac{\beta}{\alpha}\right).$$

The delay τ_d at a threshold λ satisfies the following equation:

$$\sin(\beta\cdot\tau_d+\rho)=\frac{1-\lambda}{\frac{\sqrt{\alpha^2+\beta^2}}{\beta}}\mathrm{e}^{\alpha\cdot\tau_d}. \tag{9}$$

To approximate the delay value, the sine term is expanded as a Taylor series. Considering only the first term, we find

$$\tau_d=\frac{1}{\beta}K_{\mathrm{c}}=K_{\mathrm{c}}\frac{2b_2}{\sqrt{4b_2-{b_1}^2}}, \tag{10}$$

where

$$K_{\mathrm{c}}=\frac{1-\lambda}{\sqrt{1+\left(\frac{\alpha}{\beta}\right)^2}}\mathrm{e}^{\alpha t}-\rho,$$

which is a function of b_1 and b_2. If λ is 0.9 for stretchable interconnects with a wide range of source resistance and load capacitance, then K_{c} is almost constant and $K_{\mathrm{c}}=2.0$ is a good fit.

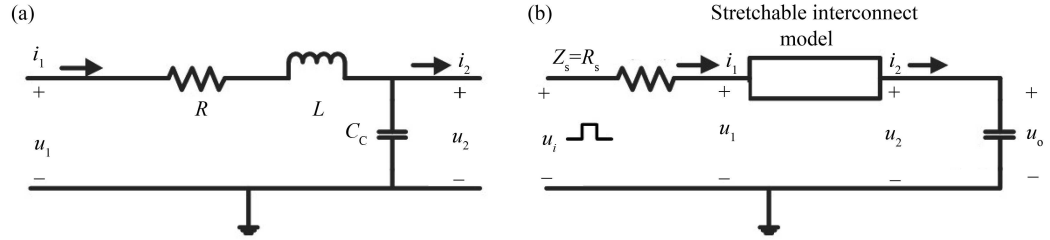

Figure 1 (a) Equivalent circuit of stretchable interconnects and (b) circuit for delay analysis.

According to the defined structure and the extracted parasitic parameters, the delay from step response of the stretchable interconnects under different driving and load conditions can be simulated to estimate the model. Appendix A shows the theoretical derivation of the model and the simulation results for the delay from step response based on stretchable flexible interconnects.

When the poles are real, R_S and C_L are the main sources of delay. As the electrical parameters of stretchable interconnects change within a limited range during deformation, their impact on the overall delay can be neglected. Compared with the signal transmitted over the stretched structure, the signal in the relaxed structure arrives ahead of time. As the voltage between the two ends of the load capacitor approaches the supply voltage, the current decreases. The inductance of interconnects increases as the interconnect length increases, hindering the decrease in the current and further increasing the voltage. Consequently, the delay decreases slightly as the length of the interconnect increases. When comparing the estimation results of the delay model with the step response of the stretchable interconnects, the error is less than 5%.

In the case of complex poles, as the interconnect length increases, the distance between two symmetric segments of stretchable interconnects in one unit increases. This increase in distance decreases the influence of crosstalk thereby increasing the overall delay. If the structure bends, the midpoint of the stretchable interconnects is fixed. Crosstalk then occurs between the two deformed segments of the stretchable interconnects. The signal superimposed with noise arrives ahead of time. As the bending angle increases, the distance between the two deformed segments decreases. Therefore, the influence of crosstalk increases, which decreases the overall delay. The validity of the proposed delay model within a tolerance of 13% was shown by comparing the simulation results with measurements in case of complex poles.

The parasitic parameters of the stretchable interconnects change as the device undergoes deformation, which contributes to the delay in the drive-interconnect-load circuit. The proposed analytical model for delay in terms of the step response of stretchable interconnects accurately describes the delay of the stretchable interconnects within a tolerance of 13%.

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Supporting information Appendix A. The supporting information is available online at info.scichina.com and link.springer.com. The supporting materials are published as submitted, without typesetting or editing. The responsibility for scientific accuracy and content remains entirely with the authors.

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