# Appendix A

## 1. Analysis Procedure

A flexible electronic design platform is used to analyze the delay associated with stretchable interconnects. The delay analysis procedure flow of stretchable interconnects is shown in Fig.1.

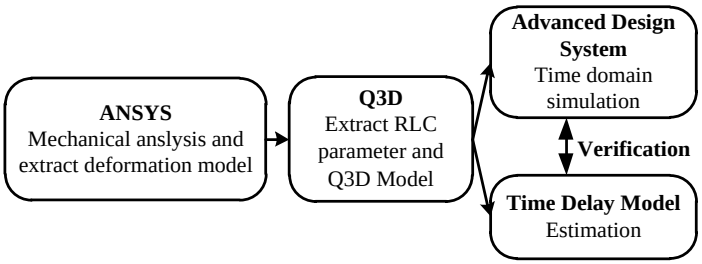


Fig.1 The Analysis Procedure Flow of The Stretchable Interconnects Delay

1.1 Stretchable Interconnects Structure

The electrical properties of stretchable interconnects would be changed with different type and degree of deformation. The initial structure of the stretchable interconnects as shown in Fig.2 were firstly defined in ANSYS software. In this paper, the stretchable interconnects consist of a copper (Cu) metal layer sandwiched between two polyimide (PI) layers. The sizes of the stretchable interconnects models selected for analysis are listed in Table.1.

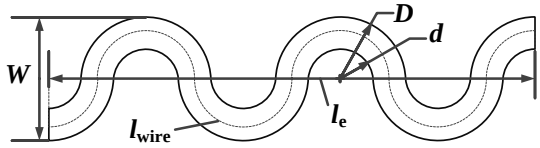


Fig.2 The Structure of The Stretchable Interconnects

Table 1 Initial Sizes of Stretchable Interconnects (unit: μm)

| Interconnects Number | Effective Length $l_e$ | Outer Radius $D$ | Inner Radius $d$ | Thickness | |
|---|---|---|---|---|---|
| | | | | Cu | Pi |
| 1 | 400 | 50 | 30 | 5 | 2 |
| 2 | 450 | 50 | 40 | 5 | 2 |
| 3 | 475 | 50 | 45 | 5 | 2 |
| 4 | 360 | 50 | 40 | 3 | 1 |

The stretching structure shown in Fig.3 (a) is formed by stretching the ends of the stretchable interconnects. The bending structure shown in Fig.3 (b) is formed by applying force perpendicular to the plane shown in Fig.2 on the ends of the stretchable interconnects, while the stretchable interconnects midpoint position and the structure width $W$ are fixed.

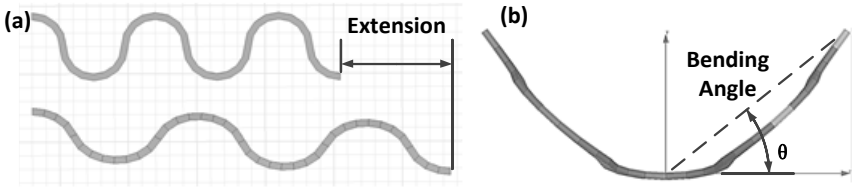


Fig.3 (a)The Stretching Structure and (b)The Bending Structure of Stretchable Interconnects

1.2 Parasitic Parameter Extraction

In order to extract the parasitic parameters, the stretchable interconnect with different deformation was built in Q3D Extractor. The Q3D model of the stretchable interconnects could be established and the obtained parasitic parameters are list in Table.2.

Table 2 Parasitic Parameters of The stretchable Interconnects

| Interconnects Number | Deformation | Resistance $R$ (mΩ) | Inductance $L$ (pH) | Capacitance $C_C$ (fF) |
|---|---|---|---|---|
| 1 | Initial | 104.8022 | 387.1516 | 7.403907 |
| 2 | Initial | 244.2285 | 527.8205 | 7.674722 |
| 2 | Stretched 20% | 244.9664 | 589.9651 | 7.899842 |
| 2 | Stretched 40% | 245.5780 | 657.7017 | 8.317020 |
| 2 | Stretched 60% | 246.1362 | 730.1843 | 8.849875 |
| 2 | Stretched 80% | 247.0095 | 806.3749 | 9.458680 |
| 2 | Stretched 100% | 247.2170 | 885.3097 | 10.07517 |
| 2 | Bended θ=21 ° | 243.2670 | 515.9012 | 7.587019 |
| 2 | Bended θ=35 ° | 244.1563 | 496.8566 | 7.578183 |
| 2 | Bended θ=43 ° | 244.6731 | 481.2232 | 7.372500 |
| 2 | Bended θ=53 ° | 243.7571 | 460.3202 | 7.285035 |
| 2 | Bended θ=64 ° | 243.9005 | 435.8585 | 7.219917 |
| 2 | Bended θ=74 ° | 243.8428 | 417.5162 | 7.035831 |
| 3 | Initial | 516.9298 | 624.8095 | 7.793077 |
| 3 | Stretched 20% | 518.0406 | 687.9922 | 8.102710 |
| 3 | Stretched 40% | 518.9060 | 758.6326 | 8.491949 |
| 3 | Stretched 60% | 518.8199 | 835.3294 | 9.138272 |
| 3 | Stretched 80% | 520.8087 | 917.2595 | 9.549586 |
| 3 | Stretched 100% | 520.7738 | 1003.3337 | 10.31244 |
| 4 | Initial | 325.9579 | 423.4869 | 5.801475 |
| 4 | Stretched 20% | 327.0753 | 475.5610 | 6.125242 |
| 4 | Stretched 40% | 328.3272 | 533.7794 | 6.868047 |
| 4 | Stretched 60% | 329.3757 | 596.1830 | 7.486235 |
| 4 | Stretched 80% | 329.7751 | 662.4745 | 7.990492 |
| 4 | Stretched 100% | 330.1667 | 731.0776 | 8.315011 |
| 4 | Bended θ=25° | 326.5638 | 408.7646 | 5.692512 |
| 4 | Bended θ=38° | 326.6110 | 391.2619 | 5.686570 |
| 4 | Bended θ=50° | 323.2550 | 369.5091 | 5.647110 |

| | | | | |
|---|---|---|---|---|
| 4 | Bended θ=65° | 323.9132 | 344.8636 | 5.539964 |
| 4 | Bended θ=70° | 326.7517 | 335.2422 | 5.441099 |

1.3 Delay Simulation from Step Response

Using the Q3D model of stretchable interconnect, the circuit as shown in Fig.4 can be built in Advanced Design System for time domain simulation. The driving gate is simulated as a voltage source including a certain internal resistance $R_S$ and the load across the interconnect terminal is a capacitor $C_L$.

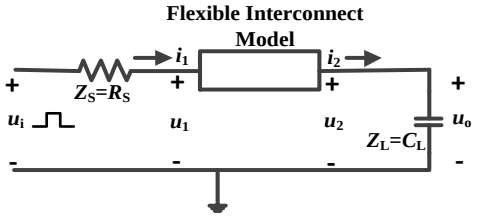


Fig.4 The Circuit for Delay Analysis

# 2 Analytical Delay Model

Figure 5 shows the equivalent circuit of stretchable interconnects used for the delay estimation tests.

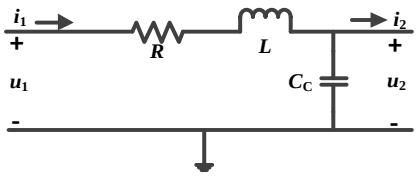


Fig.5 Equivalent Circuit Model of Stretchable Interconnects

The delay $\tau_d$ is the time required for the step response to reach a threshold value $\lambda(0<\lambda<1)$ from its initial value. the complex frequency domain ABCD parameter matrix for the equivalent circuit model of stretchable interconnects shown in Fig.5 is

$$\begin{pmatrix} 1+\dfrac{Z_1}{Z_2} & Z_1 \\ \dfrac{1}{Z_2} & 1 \end{pmatrix}, \tag{1}$$

where $Z_1 = R + sL$, $Z_2 = \dfrac{1}{sC_c}$. So, the voltage across the stretchable interconnects and the current flowing through it have the following relationships:

$$U_1(s)=\left(1+\frac{Z_1}{Z_2}\right)U_2(s)+Z_1I_2(s), \tag{2}$$

$$I_1(s)=\frac{1}{Z_2}U_2(s)+I_2(s). \tag{3}$$

Since $U_i(s)$ and $U_o(s)$ are defined respectively as the complex frequency domain function of the input voltage $u_i(t)$ and the load voltage $u_o(t)$ in the drive-interconnects-load structure shown in Fig.4, The transfer function is

$$H(s)=\frac{U_o(s)}{U_i(s)}=\frac{1}{1+\frac{Z_1}{Z_2}+\frac{Z_1}{Z_L}+\frac{Z_S}{Z_L}+\frac{Z_S}{Z_2}}, \tag{4}$$

where the source is modeled as a resistive impedance ( $Z_S=R_S$ ) and the load at the end of the interconnects is modeled using capacitive impedance ( $Z_L=C_L$ ). So the transfer function is:

$$H(s)=\frac{1}{1+b_1s+b_2s^2}, \tag{5}$$

where

$$b_1=RC_C+RC_L+R_SC_C+R_SC_L, \tag{6}$$

$$b_2=LC_C+LC_L. \tag{7}$$

As the voltage source is a step signal,

$$U_i(s)=\frac{V_i}{s}, \tag{8}$$

the output voltage can be expressed as:

$$U_o(s)=\frac{V_i}{s\left(1+b_1s+b_2s^2\right)}. \tag{9}$$

The poles of the output voltage can be either real or complex. The case of a double pole when $b_1^2-4b_2=0$ rarely appears. Therefore, the poles of the output voltage can be either real or complex.

A. Case 1: Real poles

The condition for real poles is

$$b_1^2-4b_2>0. \tag{10}$$

The output response in the case of two different real poles in time domain is

$$u_o(t)=V_i\left(1-\frac{s_2}{s_2-s_1}e^{s_1t}+\frac{s_1}{s_2-s_1}e^{s_2t}\right), \tag{11}$$

where the equation's roots are

$$s_1 = \frac{-b_1 + \sqrt{b_1^{\,2} - 4b_2}}{2b_2}, \tag{12}$$

$$s_2 = \frac{-b_1 - \sqrt{b_1^{\,2} - 4b_2}}{2b_2}. \tag{13}$$

The magnitude of $|s_2|$ is greater than $|s_1|$ and $s_2 - s_1$ is negative, hence,

$$u_o(t) \approx V_o\left(1 - \frac{s_2}{s_2 - s_1} e^{s_1 t}\right). \tag{14}$$

The delay at a threshold $\lambda$ is

$$\lambda = 1 - \frac{s_2}{s_2 - s_1} e^{s_1 \tau_d}. \tag{15}$$

When $\lambda$=0.9, the equation becomes

$$\tau_{0.9} = \frac{2b_2}{b_1 - \sqrt{b_1^{\,2} - 4b_2}} ln\left[5\left(1 + \frac{b_1}{\sqrt{b_1^{\,2} - 4b_2}}\right)\right]. \tag{16}$$

B. Case 2: Complex Poles

In the case of complex poles, condition to be satisfied is

$$b_1^{\,2} - 4b_2 < 0. \tag{17}$$

The output response for this case is

$$u_o(t) = V_i\left(1 - \frac{\sqrt{\alpha^2 + \beta^2}}{\beta} e^{-\alpha t} \cdot \sin(\beta t + \rho)\right), \tag{18}$$

where $\alpha = \frac{b_1}{2b_2}$, $\beta = \frac{\sqrt{4b_2 - b_1^{\,2}}}{2b_2}$, $\rho = \tan^{-1}\left(\frac{\beta}{\alpha}\right)$. The delay satisfies the following equation

$$\sin(\beta t + \rho) = \frac{1 - \lambda}{\frac{\sqrt{\alpha^2 + \beta^2}}{\beta}} e^{\alpha t}. \tag{19}$$

To approximate the value of delay, the sin term is expanded as a Taylor series. Considering the first term only, we find

$$\tau_d = \frac{1}{\beta} K_c = K_c \frac{2b_2}{\sqrt{4b_2 - b_1^{\,2}}}, \tag{20}$$

where

$$K_c = \frac{1-\lambda}{\sqrt{1+\left(\frac{\alpha}{\beta}\right)^2}} e^{\alpha t} - \rho, \tag{21}$$

which is a function of $b_1$ and $b_2$. As shown in Fig.6, when $\lambda$ is 0.9, comparing the simulated delay value and $\frac{1}{\beta}$ for stretchable interconnects with a wide range of source resistance and load capacitance, $K_c$ is almost constant and $K_c$=2.0 is a good fit.

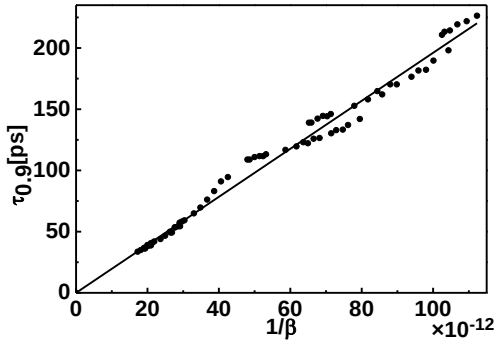


Fig.6 Relationship Between Stretchable Interconnects Delay and 1/$\beta$ in Case of Complex Poles

# 3 Accuracy of The Delay Model

According to the defined structure and the extracted parasitic parameters, the delay from the step response of the stretchable interconnects under different driving and load conditions can be simulated to estimate the model.

For the stretchable interconnects, crosstalk occurs between two symmetric segments in repeated units of the stretchable interconnects due to the special structure. The leap direction of crosstalk noise is same as the original signal. Therefore, compared with the same length straight interconnect, in stretchable interconnect the signal with superimposed noise arrives ahead of time. In the case of complex poles, the delay of the No.2 and No.4 stretchable interconnects subjected to stretching deformation is shown in Fig.7 (a) and (b). As the interconnect length increases, the distance between two symmetric segments of stretchable interconnects in one unit increases. This increase in distance decreases the influence of crosstalk thereby increasing the overall delay.

If the structure bends, the midpoint of the stretchable interconnects is fixed. Crosstalk-like problems occur between the two deformed segments of the stretchable interconnects. The signal with superimposed noise arrives ahead of time. The delay of the No.2 and No.4 stretchable interconnects subjected to bending deformation when the poles are complex is shown in Fig.7 (c) and (d). As the bending angle increases, the distance between the two deformed segments decreases. Therefore, the influence of crosstalk increases, which decreases the overall delay. As shown in Fig.7, the validity of the proposed delay model within a tolerance of 13\% was shown by comparing the simulation results with measurements in case of complex poles.

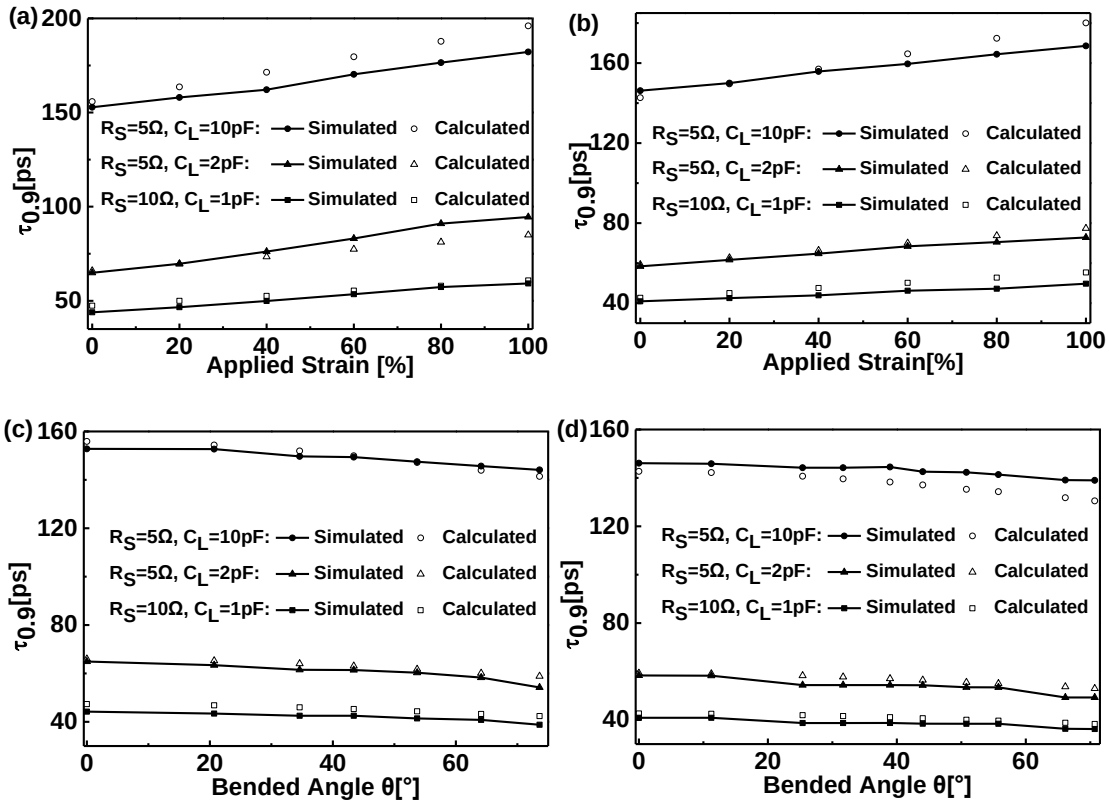


Fig.7 The Delay of Stretchable Interconnects Subjected to Deformation in Case of Complex Poles: (a) No.2 Interconnect Stretched, (b) No.4 Interconnect Stretched, (c) No.2 Interconnect Bended, (d) No.4 Interconnect Bended

The estimation results and simulation results of delay for the stretchable interconnects without deformation in single real pole condition are shown in Table 3. Different interconnects structures had little influence on the delay under the same driving and load conditions. The condition for the case of a single real pole to be satisfied is $b_1^2 - 4b_2 > 0$, so the parameters in the circuit have the following relationship:

$$\left(R_S + R\right)\sqrt{C_L + C_C} > 2\sqrt{L} \tag{22}$$

The $R_S$ and $C_L$ are the main sources of delay. Comparing the estimation results of the delay model with step response of the stretchable interconnects with the simulation results, the error is less than 5%. As the variation range of the electrical parameters of stretchable interconnects deformation is limited, the impact on the overall delay of the circuit can almost be ignored when deformation of stretchable interconnects under force occurs. The step response of NO.2 stretchable interconnect with $R_S$=30Ω， $C_L$=5fF is shown in Fig.8. Compared with the signal transmitted in the stretched structure, the signal in initial structure arrives ahead of time. As the voltage between the two ends of the load capacitor approaches the supply voltage, the current decreases. The inductance of interconnects increases as the interconnect length increases, hindering the decrease in the current and further increasing the voltage. Consequently, the delay decreases slightly as the length of the interconnect increases.

Table 3 The Delay of Initial Stretchable Interconnects in Case of Real Poles

| Interconnects Number | $R_S$ (Ω) | $C_L$ (pF) | Simulated Delay (ps) | Estimated Delay (ps) | Error (%) |
|---|---|---|---|---|---|
| 1 | 30 | 3 | 190.1 | 182.5 | 4.16 |
| 2 | 30 | 3 | 184.2 | 181 | 1.77 |
| 3 | 30 | 3 | 183.3 | 182.5 | 0.438 |
| 4 | 30 | 3 | 189.8 | 187.9 | 1.01 |
| 1 | 30 | 5 | 329.4 | 331.7 | 0.693 |
| 1 | 30 | 10 | 676.5 | 684.7 | 1.20 |
| 1 | 30 | 20 | 1370 | 1370 | 0.00 |
| 2 | 100 | 3 | 687.3 | 693.2 | 0.851 |
| 2 | 500 | 3 | 3463 | 3464 | 0.029 |

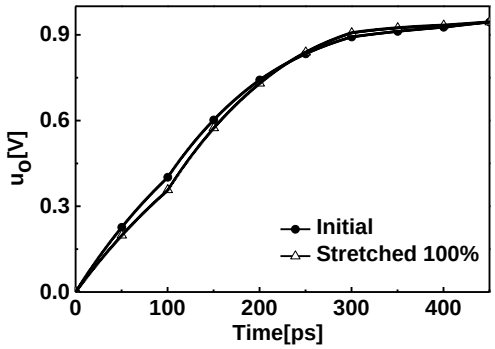


Fig.8 Step Response of Stretchable Interconnects in Case of Complex Poles