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6 Gbps 16QAM fully integrated receiver using optimized neutralization technique LNA in 90 nm CMOS

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Dear editor,

The research of multi-Gb/s wireless communication applications in millimeter wave, especially in 60 GHz unlicensed band has become attractive in recent years. Many fully-integrated complimentary metal oxide semiconductor (CMOS) receivers have been reported with great performance [1–5]. To achieve satisfied performance of power gain, bandwidth and linearity, the power efficiency is still a big challenge during 60 GHz circuits design. On the other hand, the noise factor, which determines the sensitivity of the receiver, deteriorates significantly in 60 GHz band.

A 60 GHz receiver is proposed to realize 6 Gbps 16QAM modulation communication. The two-stage low noise amplifier (LNA) using under/over neutralization technique improves the power efficiency, reduces the noise factor and provides sufficient power gain as well as bandwidth. The radio-frequency (RF) mixer using transformer peaking architecture further increases the overall gain of the receiver and reduce the noise figure. A fully differential programmable gain amplifier (PGA) with direct current (DC) offset is achieved to drive 50 Ω load. And the clock of the receiver is realized by a 24 GHz fully-differential phase-locked loop (PLL) along with frequency divider and doubler.

Receiver architecture. The block diagram of the presented receiver is shown in Figure 1. It consists of a LNA, followed by the first stage down-conversion mixer with 48 GHz local oscillation (LO) signals and the second stage down-conversion mixer with 12 GHz I/Q LO signals. The PGA with DC offset circuits is in the final stage to drive 50 Ω output load. The 48 GHz and 12 GHz LOs for the two down-conversion mixer are generated from a 24 GHz PLL followed by a frequency doubler and a frequency divider.

LNA. The main design goals are lower-power consumption, high conversion gain, good sensitivity, and lower noise figure. Such requests features of the receiver are achieved by optimising the design of LNA mixer, and PGA. The proposed LNA employs two-stage common source topology to achieve high gain as well as high linearity. From the simulation results, there are two region on the two sides of the neutralized point. In the over-neutralization region, the $G_{\max}$ improves along with the neutralization capacitance increasing significantly. However, the $\mathrm{NF}_{\min}$ also increases along with the capacitance. In the under-neutralization region, the $G_{\max}$ improves when the neutralization capacitance reduces. Besides, the $\mathrm{NF}_{\min}$ also decreases along with the capacitance. However, the peak $G_{\max}$ of under neutralization region is a little lower than over-neutralization. To achieve the optimal gain and noise performance, the neutralization capacitance is chosen around the boundary of the under/over neutralization region, where the K_f equals to one. The equation

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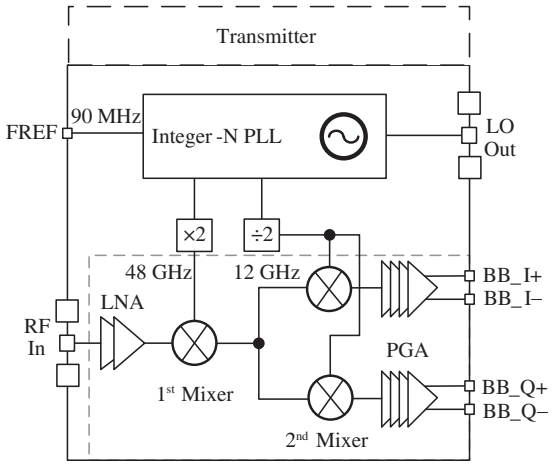

Figure 1 Block diagram of the proposed receiver.

of stability factor can be expressed as

$$K_f = \frac{2\mathrm{Re}[Y_{11}]\mathrm{Re}[Y_{22}] - \mathrm{Re}[Y_{12}Y_{21}]}{|Y_{12}Y_{21}|}, \quad (1)$$

and by using the small-signal equivalent circuit, we can write the equation where K_f equals one,

$$\begin{aligned}&[(g_m - \omega^2 C_{gd}^2 R_{gd})^2 - 2M](C_n - C_{gd})^2 \\ &+ 2[g_m C_m \omega^2 C_{gd}^2 R_{gd} - C_m(\omega^2 C_{gd}^2 R_{gd})^2 \\ &+ C_m M](C_n - C_{gd}) + C_m^2(\omega^2 C_{gd}^2 R_{gd})^2 \\ &- \frac{M^2}{\omega^2} - \frac{2g_m\omega^2 C_{gd}^2 R_{gd} M}{\omega^2} = 0, \end{aligned} \quad (2)$$

where M equals $2\mathrm{Re}[Y_{11}]\mathrm{Re}[Y_{22}]$. Eq. (2) is a two order equation of the unknown variable $C_n - C_{gd}$ and there are two roots of the equation on both sides of zero. From (2), we can figure out the boundary of both under and over neutralization region. In the first stage of LNA, under neutralization technique is used as the noise performance is the priority. And in the second stage, over neutralization increases the power gain more to suppress the following mixer. Since both the under and over neutralization technique improve the performance of the common-source (CS) differential pair without any addition of power consumption, the fewer stages of cascade are utilized, which increases the overall efficiency of the LNA significantly. From the simulation results, two stage LNA can employ 20 dB gain, 9 GHz bandwidth and only 4.9 dB noise factor. The power consumption of LNA is only 14.4 mW.

Mixer. The double-balanced architecture is used for the mixers in both transmitter and receiver due to its higher linearity and superior suppression of spurious products. In the first down-converter in the proposed receiver, a transformer peaking structure is introduced to boost the conversion gain and suppress the noise figure. The mixer conversion gain is given as

$$A_v = \frac{2}{\pi} g_m R_L \left(1 - \frac{\sqrt{2V_{\mathrm{ov}}^2}}{\pi V_{\mathrm{LO}}}\right), \quad (3)$$

where g_m is the transconductance of the RF input transistors, R_L is the load impedance, V_{ov} is the overdrive voltage of the switching transistors and V_{LO} is the LO swing. From (3), increasing the swing of LO signal and decreasing the overdrive voltage of the switch pair can boost the conversion gain of the mixer. However, in millimeter wave frequency, increasing the amplitude of LO results in massive additional power consumption as well as nonlinearity of the switch pair. And low overdrive voltage will reduce the transconductance of the input transistors which limits the conversion gain. Increasing the g_m of the input transistors is a proper way for gain-boosting and noise suppression. On the other hand, the parasitics at the drain of the input transistors are extremely large, which will lead to the critical leakage of RF signal to ground. The peaking transformer introduced in the proposed mixer is a commendable solution. The g_m of the input transistors is increased due to the independent supply from the common tap of the transformer and the parasitics are resonated at the same time. The overdrive voltage of the switch pair can be configured independently without concerning the reduction of the g_m. The linearity of the mixer is increased thanks to the DC blocking effect of the transformer. The proposed transformer peaking architecture provides 16 dB gain boosting and 5 dB noise suppression by simulation.

PGA. The analog baseband is integrated on chip to provide necessary dynamic range and DC offset. The three stage PGA with dc-offset calibration (DCOC) loops is proposed. The modified Cherry-Hooper amplifier with negative capacitive neutralization technique is employed to achieve wideband performance. In order to attain wide gain adjustment ability, each g_m-cell is partitioned into several units, where digitally-controlled switches turn each unit on/off to realize different voltage gain. Simulation shows a programmable gain from 20 to 48 dB with a 3 dB bandwidth of above 3 GHz.

LO path. The LO signal is generated by the 24 GHz fractional-N synthesizer combined with injection-lock frequency doubler and current mode logic (CML) divider. Injection-lock doubler enables the large amplitude of the second-order harmonic without introducing multi-stage buffer, which is power hungry. The push-push pair extracts the second-order harmonic current signal, and injects into the cross-coupled resonator. The

transformer provides the benefits of DC blocking, thus the bias of the push-push pair and cross-coupled pair can be optimized independently. The bias of the push-push pair is optimized for the strongest second-order nonlinearity and the cross-coupled pair is biased based on the trade-off between injection locking range and quality factor of the resonator. The switched capacitor array (SCA) provides sufficient tuning range of the injection locking range. From the simulation result, the frequency doubler locking range covers 44–54 GHz of the second-order output with −6 dBm input power.

Measurement result. The proposed 60 GHz receiver is fabricated in 90 nm CMOS technology. All measurements were performed in a chip-on-board configuration by directly probing mm-wave signals at ground-signal-ground (GSG) port. The small signal characteristics of receiver (RX) is measured using Keysight PNA-X. The maximum conversion gain of the receiver is 69 dB and the minimum noise figure is about 6.5 dB. The large signal measurement result exhibits the output P_1 dB of −5 dBm in the condition of 1 GHz baseband frequency, which ensures the driving ability of the baseband analog-to-digital converter (ADC). The total power consumption of the receiver is only 60 mW thanks to the power saving LNA.

To measure the system error vector magnitude (EVM), the integrated transmitter is introduced to transmit 16QAM signal through horn antenna. The 16QAM signal is generated by Keysight M8190A. And the output waveform is measured using Keysight MSOS804A oscilloscope. The data rate of the 16QAM signal is setting to 6 Gbps and the EVM value is below −26 dB. The RX draws 60 mW from a 1.2 V supply, of which the LNA only consumes 14.4 mW and the PLL with divider and doubler consumes 40 mW.

Conclusion. A 6 Gbps 60 GHz 16QAM receiver for 802.11ad applications is designed and fabricated in 90 nm CMOS technology. Under/over neutralization LNA, transformer peaking mixer and digitally controlled Cherry-Hooper PGA are proposed for high power efficiency, low noise figure, high conversion gain and broadband requirements. The measured EVM of 6 Gbps data rate 16QAM modulation is −26 dB and only 60 mW power consumed from the receiver.

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Supporting information Appendixes A–C. The supporting information is available online at info.scichina.com and link.springer.com. The supporting materials are published as submitted, without typesetting or editing. The responsibility for scientific accuracy and content remains entirely with the authors.

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