SCIENCE CHINA
Information Sciences

• LETTER •

June 2018, Vol. 61 069404:1–069404:3
https://doi.org/10.1007/s11432-017-9227-4

Design of mm-wave amplifiers based on over & under neutralization techniques

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Received 27 May 2017/Accepted 31 August 2017/Published online 19 April 2018

Citation Li D, Zhang L, Zhang L, et al. Design of mm-wave amplifiers based on over & under neutralization techniques. Sci China Inf Sci, 2018, 61(6): 069404, https://doi.org/10.1007/s11432-017-9227-4

Dear editor,

Recently high-speed wireless communications in 60 GHz unlicensed band become increasingly attractive for both academia and industry [1–5]. Millimeter wave amplifiers are believed difficult in complimentary metal oxide semiconductor (CMOS) process when the operating frequency is close to the cut-off frequency of transistors even the CMOS technology is scaled into the nanometer range. Although the unity current gain frequency (f_T) and the maximum oscillation frequency ($f_{\max}$) improve, CMOS transistors can hardly provide considerable maximal available gain ($G_{\max}$) and minimum noise figure ($\mathrm{NF}_{\min}$) limited by the gain-to-drain parasitic capacitance C_{gd}. On the other hand, the stability of amplifier is also degraded due to these parasitic effects.

In this article, two-stage low noise amplifier (LNA) and power amplifier (PA) operating at 60 GHz band employing the proposed over & under neutralization techniques are demonstrated for verification in a 65 nm CMOS process. Measured results show that the proposed LNA achieved a power gain of 19 dB and a noise figure of 4.9 dB, with a bandwidth of 7 GHz and a total power consumption of only 14.4 mW. The proposed PA achieved a bandwidth of 8 GHz and a 20 dB power gain, consuming 100.8 mW of power from a 1.2 V supply, while the output P_{1dB} and power added efficiency (PAE) are 10.4 dBm and 17%, respectively.

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Over/under neutralization. The poor reverse isolation caused by the gain-to-drain parasitic capacitances C_{gd} becomes one of the most critical issues in the design of a 60 GHz CMOS amplifier, which may incur the degradation of gain, minimal noise figure ($\mathrm{NF}_{\min}$), and stability as well. The neutralization capacitors (C_n) are introduced in prior arts to compensate the parasitic capacitance C_{gd} so as to improve the $G_{\max}$ and reduce the $\mathrm{NF}_{\min}$ of the differential pair.

The value of C_n will be chosen to maximize the stability factor (K_f) for conventional neutralization, thus maximizing the stability of the amplifier. It can be noticed that the C_n is chosen for a maximal K_f so as to guarantee the stability of the amplifier, resulting in a compromised $G_{\max}$. However, we can figure out that the neutralization technique cannot achieve the gain and noise figure optimization of a single stage differential pair. In next paragraph, the theoretical analysis of the small signal equivalent circuit of the common source differential pair is given. Thus, it can be figured out that the over & under techniques are optimizing methods to improve the single stage gain and the noise performance.

The parameters of the parasitic resistance and capacitance are extracted from the measurement data of single transistor. Where R_{gs} and C_{gs} are the gate-to-source resistance and capacitance, R_{gd} and C_{gd} are the gate-to-drain resistance and capacitance, R_{ds} and C_{ds} are the drain-to-source

resistance and capacitance, $R_{\rm sub}$ and $C_{\rm sub}$ are the substrate resistance and capacitance. g_m represents the real part of transconductance and C_m represents the imaginary part of transconductance. According to the parasitic parameters, Y-parameters can be written as follows:

$$Y_{11}=\omega^2(C_{\rm gs}^2R_{\rm gs}+C_{\rm gd}^2R_{\rm gd})+{\rm j}\omega(C_{\rm gs}+C_{\rm gd}+C_n), \quad (1)$$

$$Y_{12}=-\omega^2C_{\rm gd}^2R_{\rm gd}-{\rm j}\omega(C_{\rm gd}-C_n), \quad (2)$$

$$Y_{21}=g_m-\omega^2C_{\rm gd}^2R_{\rm gd}-{\rm j}\omega(C_{\rm gd}+C_m-C_n), \quad (3)$$

$$Y_{22}=\left(\frac{1}{R_{\rm ds}}+\omega^2(C_{\rm gd}^2R_{\rm gd}+C_{\rm sub}^2R_{\rm sub})\right)+{\rm j}\omega(C_{\rm gd}+C_{\rm sub}+C_{\rm ds}+C_n). \quad (4)$$

The stability factor K_f can be expressed as

$$K_f=\frac{2{\rm Re}[Y_{11}]{\rm Re}[Y_{22}]-{\rm Re}[Y_{12}Y_{21}]}{|Y_{12}Y_{21}|}. \quad (5)$$

The maximum available gain is the theoretical maximum power gain which assumes the input and output ports are ideally matched to the conjugate impedance. The $G_{\rm max}$ can be expressed by the function of S-parameters and K_f as

$$G_{\rm max}=\left|\frac{S_{21}}{S_{12}}\right|(K_f-\sqrt{K_f^2-1}). \quad (6)$$

It can be noticed that there are two regions which named under/over neutralization region, on the both sides of the neutralized point where the maximum K_f is achieved. In the under neutralization region, the $G_{\rm max}$ improves when the neutralization capacitance reduces. Besides, the $\rm NF_{min}$ also decreases along with the capacitance. In the over-neutralization region, the $G_{\rm max}$ improves along with the neutralization capacitances increasing significantly. However, the $\rm NF_{min}$ also increases along with the capacitance. It is shown from the simulation result that the $\rm G_{max}$ of the transistors in under-neutralization region is 1.5 dB larger than the normal in the 60 GHz frequency. On the other hand, the minimum noise figure of the under-neutralization technique is 0.1 dB lower than normal. The $G_{\rm max}$ of the transistors in over-neutralization region is 3 dB larger than the normal, while the $\rm NF_{min}$ is 0.05 dB larger. Thus, the under-neutralization region is a better choice of neutralized differential pair when both the noise figure and power gain are under concern. The over-neutralization region is more noticeable in the gain boosting effect. In our design, the pre-stage of LNA is neutralized in the under-neutralization region to guarantee the noise figure of the stage as well as the capability of noise suppression, and the PA as well as the post-stage of LNA is neutralized in the over-neutralization region where the power gain is more valuable.

Nevertheless, both of the over/under neutralization regions have boundaries, where the stability factor equals to one. Exact calculation of the boundaries is necessary to choose the value of the neutralization capacitance reasonably. When K_f equals to one, we have

$$P^2-2P{\rm Re}[Y_{12}Y_{21}]={\rm Im}^2[Y_{12}Y_{21}], \quad (7)$$

where $P=2{\rm Re}[Y_{11}]{\rm Re}[Y_{22}]$.

Jointing the (1)–(4) and (7), the boundary of the over/under neutralization region can be calculated through the quadratic (8). Eq. (8) can be simplified as (9) by ignoring the high order terms of ω. It is clear that there are two roots of the (9) on the both sides of the $C_{\rm gd}$, corresponding the two boundaries of the over/under neutralization region

$$\begin{aligned}&[(g_m-\omega^2C_{\rm gd}^2R_{\rm gd})^2-2M](C_n-C_{\rm gd})^2\\&+2[g_mC_m\omega^2C_{\rm gd}^2R_{\rm gd}-C_m(\omega^2C_{\rm gd}^2R_{\rm gd})^2\\&+C_mM](C_n-C_{\rm gd})+C_m^2(\omega^2C_{\rm gd}^2R_{\rm gd})^2\\&-\frac{M^2}{\omega^2}-\frac{2g_m\omega^2C_{\rm gd}^2R_{\rm gd}M}{\omega^2}=0, \end{aligned} \quad (8)$$

$$\begin{aligned}&g_m^2(C_n-C_{\rm gd})^2+2[g_mC_m\omega^2C_{\rm gd}^2R_{\rm gd}+MC_m]\\&\times(C_n-C_{\rm gd})-\frac{M^2}{\omega^2}-\frac{2g_m\omega^2C_{\rm gd}^2R_{\rm gd}M}{\omega^2}=0. \end{aligned} \quad (9)$$

Measurement results. The measured S-parameters of the two stage differential LNA achieves a peak power gain of 19 dB and the S_{11} behaves well below −10 dB over a bandwidth of above 10 GHz around 60 GHz as shown in Figure 1(a). The 3 dB bandwidth of S_{21} is 7 GHz. In the whole band, K_f is over 1 and the stability performance is guaranteed. Due to the proposed over & under neutralization techniques, the stability factor is compromised to the 5.9 min. The noise figure is measured as 4.9 dB at 60 GHz, and maintains below 5 dB over the entire 7 GHz bandwidth. Linearity measurements show an output $P_{\rm 1dB}$ of 2.1 dBm and an IIP3 of −6.2 dBm at 60 GHz. The power consumption of the proposed LNA is only 14.4 mW from a 1.2 V supply with only two cascaded stages.

The PA achieves a peak power gain of 20 dB and with an S_{22} of lower than −10 dB over the entire band. The 3 dB bandwidth of the PA is 9 GHz as shown in Figure 1(b). An output $P_{\rm 1dB}$ of 10.4 dBm at 63 GHz is achieved and the peak PAE is 18.6%. The stability factor of proposed power amplifier is above 1 in the whole band and

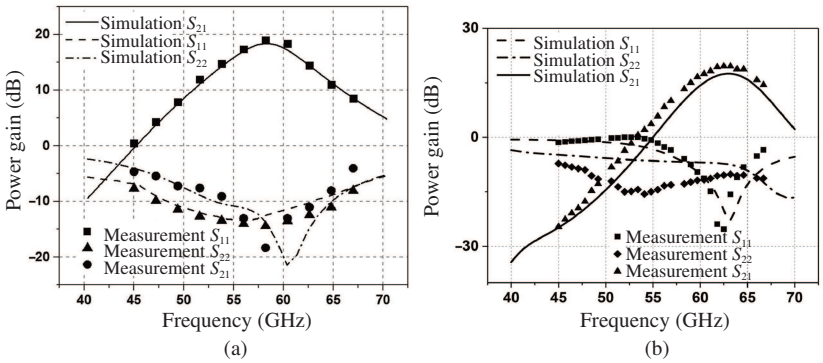

Figure 1 S-parameters measurement results of proposed (a) LNA and (b) PA.

the minimum K_f is still larger than 160. The total power consumption of PA is 100.8 mW.

From the measurement results, it can be figured out that both small signal parameters measurement results and the linearity measurement results match the simulation perfectly. It verifies the accuracy of our modeling and design methods.

Conclusion. In this article, under & over neutralization techniques are proposed for the design of millimeter-wave amplifiers. The proposed techniques are realized on a 60 GHz two LNA and a two stage PA in 65 nm low power (LP) CMOS process. The LNA achieves a 19 dB gain, 7 GHz 3 dB bandwidth, 2.1 dBm $P_{1\mathrm{dB}}$ with a noise figure of 4.9 dB, while consuming only 14.4 mW from a supply of 1.2 V. And the PA features 20 dB gain, >8 GHz bandwidth, a 10.4 dBm $P_{1\mathrm{dB}}$ with 17% PAE and 14 dBm P_{SAT}, verifying the correctness of the proposed neutralization techniques as well as the small signal equivalent model of transistors.

Acknowledgements The authors would like to thank Lorentz solution for Peakview EM (electromagnetic) design and Keysight for measurement supports.

Supporting information Appendixs A–D. The supporting information is available online at info.scichina.com and link.springer.com. The supporting materials are published as submitted, without typesetting or editing. The responsibility for scientific accuracy and content remains entirely with the authors.

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