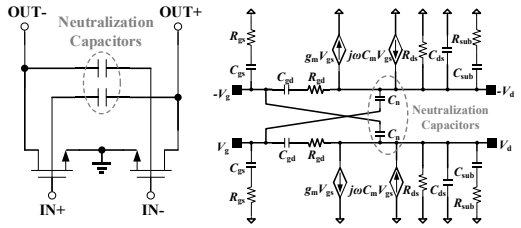
Appendix A

Over and under neutralization: Topology of a conventional neutralized common source differential pair is shown in Figure S1(a), and the small signal equivalent circuit is depicted in Figure S1(b).

Figure S2 depicts the G_{max}, K_f and NF_{min} as functions of the neutralization capacitance, where the G_{max} and K_f results are calculated through the formula above and the noise figure obtained from simulation.



(a) (b)

Figure S1 (a) A simplified schematic of neutralized differential pair; (b) small signal equivalent circuit of neutralized differential pair.

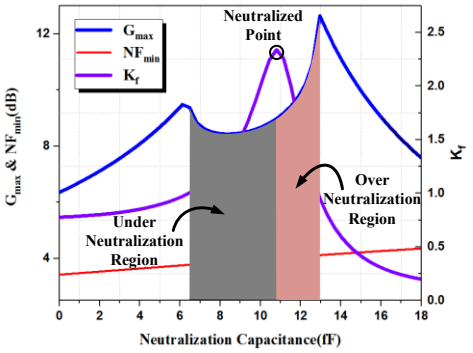


Figure S2 Characteristics of neutralized differential pair.

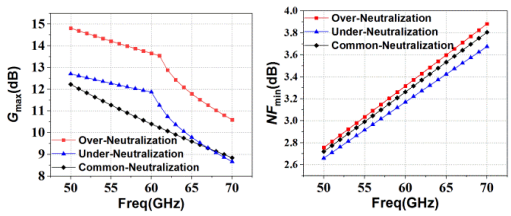


Figure S3 Characteristics of over and under-neutralized differential pair. (a)G_{max}, (b)NF_{min}.

Figure S3 shows the G_{max} and NF_{min} of the both regions of neutralization against the normal neutralization technique. It is clear that the G_{max} of the transistors in under-neutralization region is 1.5dB larger than the normal in the 60GHz frequency. On the other hand, the minimum noise figure of the under-neutralization technique is 0.1dB lower than normal. And the G_{max} of the transistors in over-neutralization region is 3dB larger than the normal, while the NF_{min} is 0.05dB larger. Thus, the under-neutralization region is a better choice of neutralized differential pair when both the noise figure and power gain are under concern. And the over-neutralization region is more noticeable in the gain boosting effect. In our design, the pre-stage of LNA is neutralized in the under-neutralization region to guarantee the noise figure of the stage as well as the capability of noise suppression, and the PA as well as the post-stage of LNA is neutralized in the over-neutralization region where the power gain is more valuable.

Appendix B

Neutralization Capacitor: The neutralization capacitance is extremely small since the value of the capacitance is nearly the same as the transistor's parasitic capacitance of gate-to-drain. The tiny capacitance is hardly to realize accurately in such high working frequency. This paper proposes a simple structure to achieve such small capacitance and the value of capacitance is relatively fixed in the required band.

Figure S4 shows the layout of the proposed neutralization capacitance. It adopts the MOM structure and the metal layers used are from M4-M7 since the metal thickness and conductivity of these layers are the same in process. The metal width is adjusted to match the required capacitance and the EM simulation result of the MOM cap is shown in Figure S5. The capacitance of the MOM cap changes little

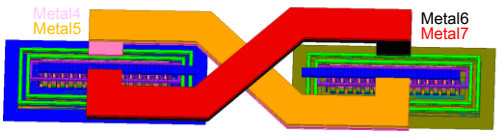


Figure S4 Layout of proposed neutralization capacitance.

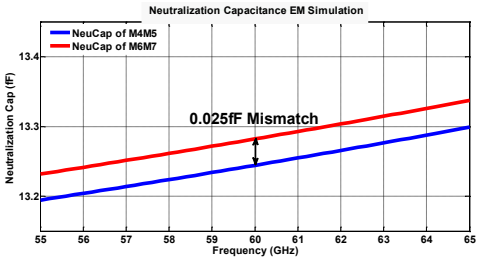


Figure S5 EM simulation results of proposed neutralization capacitance.

from 55GHz-65GHz and only 0.025fF mismatch between the two differential capacitance. The mismatch can hardly affects the amplifier since the common mode rejection ratio is large enough.

Appendix C

Matching Network: Conventional conjugate matching in mm-wave amplifiers are realized through transmission line T-junction network with the blocking capacitor. The intrinsic loss of transmission lines and finger-cap in millimeter-wave frequency band results in large insertion loss of the matching network. Furthermore, the bandwidth of the amplifier is limited due to the matching network mentioned above. Figure S6 shows the topology of the traditional matching network based on T-junction as well as the proposed matching network based on transformer. The input impedance of the differential pair is capacitive with a high quality factor because of the neutralization capacitance's feedback and the output impedance of the single-stage amplifier is capacitive with a low Q. Figure S7 shows the impedance matching process between the two impedance of the different matching methods. When matching from transistors' gate to the previous stage's drain, the traditional finger-cap blocking capacitor will lead to the impedance turning toward to the higher Q region even the capacitance is large enough. The higher Q matching network leads to the bandwidth limitation. In the contrary, the matching network using single transmission line and transformer will not cause the impedance transfer curve crossing the constant Q circle. The similar condition occurs when matching from transistors' drain to next stage's gate. The traditional matching network will still lead to the high Q matching network compared with our proposed matching network.

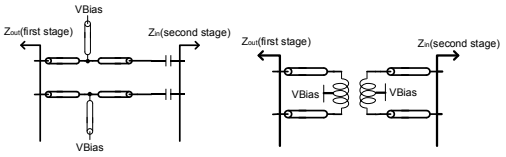


Figure S6 (a) Traditional matching network based on T-junction (b) Proposed matching network based on transformer.

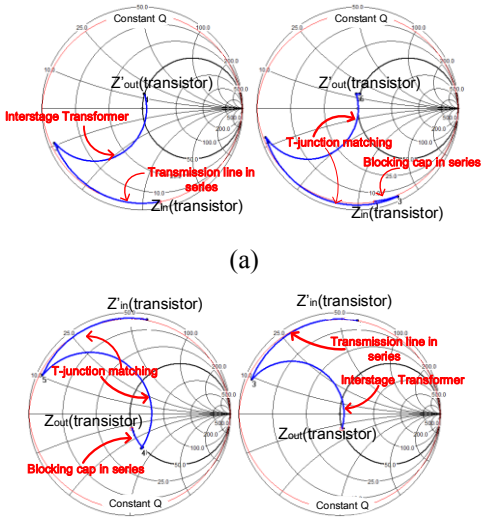


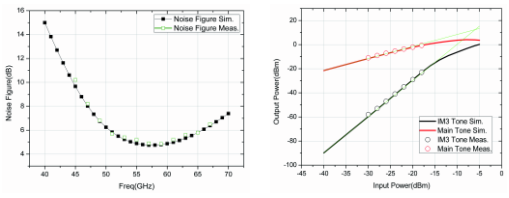
Figure S7 (a) Matching from transistors' gate to drain. (b) Matching from transistors' drain to gate.

The advanced matching network using single transmission line instead of the T-junction structure, in combination with the transformers of scalable radius for DC blocking. By properly designing the radius of transformers and the lengths of the transmission lines, the proposed matching network can match any two impedance in 60GHz.

The proposed topology of inter-stage matching network enables broader bandwidth versus the T-junction counterpart, by virtue of the transformer and single transmission line. The injection loss is also reduced due to the simplified transmission lines networks. According to simulations, the overall injection loss of the proposed inter-stage matching network can be reduced to <1.5dB.

Appendix D

Measurement Results: In the whole band, K_f of proposed LNA is over 1 and the stability performance is guaranteed. Due to the proposed over\&under neutralization techniques, the stability factor is compromised to the 5.9 minimum. Figure S8(a) shows the measured noise performance and Figure S8(b) shows the large signal characteristics measurement results. The noise figure is measured as 4.9dB at 60GHz, and maintains below 5dB over the entire 7GHz bandwidth. Linearity measurements show an output P_{1dB} of 2.1dBm and an IIP3 of -6.2dBm at 60GHz.



(a) (b)

Figure S8 (a) Noise figure of LNA (b) output P_{1dB} and IIP3 of LNA.

Large signal measurement results and power-added efficiency of proposed PA are shown in Figure S9. An output P_{1dB} of 10.4dBm at 63GHz is achieved and the peak PAE is 18.6%. Figure S10 shows the measured output P_{1dB} and stability factor changed with frequency of the proposed power amplifier. The largest P_{1dB} is 10.8dBm in 64GHz. The stability factor of proposed power amplifier is above 1 in the whole band and the minimum K_f is still larger than 160.

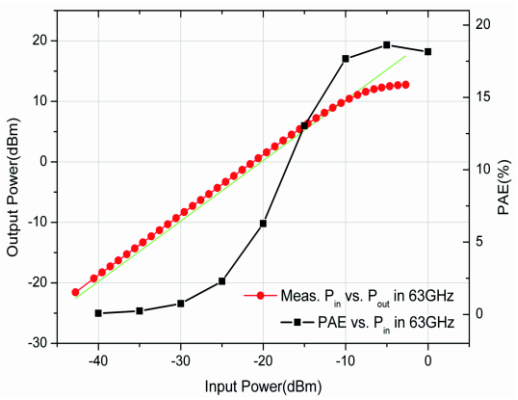


Figure S9 Measured output P_{1dB} and PAE in 63GHz of the PA.

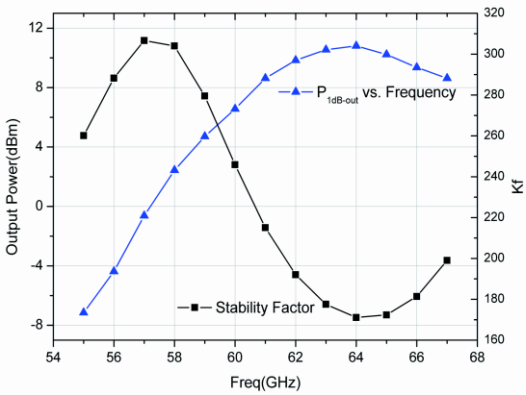


Figure S10 Measured output P_{1dB} and stability factor versus frequency of the PA.