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A study of residual characteristics in floating gate transistors

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Dear editor,

The floating gate transistor is a device that has been extensively applied to non-volatile memories, such as EEPROM and Flash memories. The residual characteristics of floating gate transistors after program and erase (P/E) cycles are closely related to information security and have received a great deal of attention for decades [1]. Data remanence in floating gate transistors is the residual physical characterization, which is embodied in the differences of threshold voltages after different P/E cycles, and in the meanwhile confidential information theft is brought about by detecting threshold voltages of floating gate transistors [2]. The shift of the threshold voltage $V_{\rm th}$ is mainly caused by the residual charges in the floating gate after erase operation and the degradation of thin tunnel gate oxide [3]. In order to ensure that data would not be restored, the government agencies such as the US department of defense declared that EEPROM and Flash memories should be sanitized by overwriting all locations [4].

At first, we explain two phrases that will be used for this letter. The initial P/E cycles are regarded as the operations that contain confidential information. The overwriting operations represent the operations which are used to overwrite the initial P/E cycles. The purpose of this letter is to eliminate differences in threshold voltages of different initial P/E cycles by means of overwriting operations. In this letter, the effects of different overwriting operations are investigated in the approach of two-dimensional simulations, and a specific P/E sequence used as overwriting operations is proposed, which makes the probability of recovering confidential data reduced effectively in a floating gate transistor.

Device structure. The basic structure of the floating gate transistor with 180 nm floating-gate technology is illustrated in Figure 1(a). The Si substrate is p-type with a boron concentration of 1×10^{12} cm^{-3}. The thickness of the tunneling oxide is approximately 10 nm. The floating gate is formed by depositing a poly silicon layer with a phosphorus concentration of 6×10^{14} cm^{-3} and the thickness is 150 nm. It is followed by the deposition of the ONO ($SiO_2/Si_3N_4/SiO_2$) layer with the thickness of 5, 10 and 5 nm, respectively. The thickness of the n-type poly-Si control gate is 150 nm. The source/drain (S/D) implant is performed with an arsenic dose of 1×10^{15} cm^{-3} after an oxide etching process. The value of the S/D junction depth is extracted as approximately 0.14 μm.

Device operations. According to the characteristic of P/E cycles in Flash memories that the program operation can only be followed by the erase operation but not the program [5], all possible initial P/E cycles regarded as confidential information are performed on a floating gate transis-

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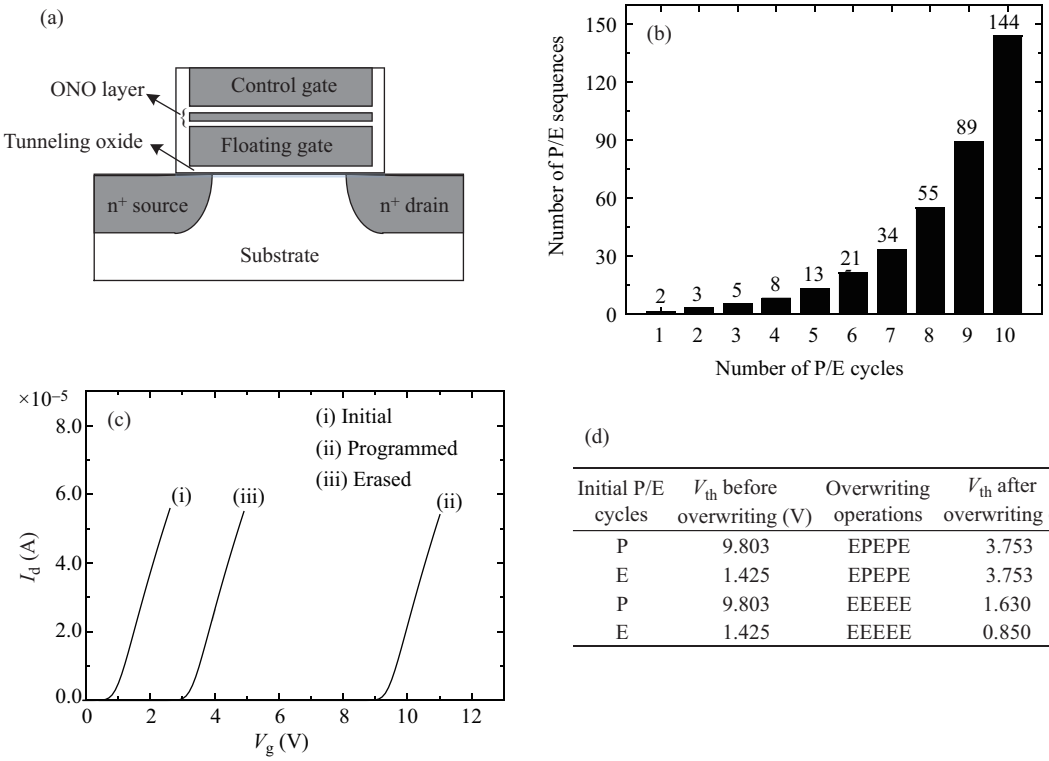

Initial P/E cycles	V_{th} before overwriting (V)	Overwriting operations	V_{th} after overwriting (V)
P	9.803	EPEPE	3.753
E	1.425	EPEPE	3.753
P	9.803	EEEEE	1.630
E	1.425	EEEEE	0.850

Figure 1 (a) Structure of the floating gate transistor. (b) Illustration of the number of P/E sequences at 1-10 P/E cycles. (c) The Id-Vg characteristics of the floating gate transistor (i) before it is first programmed; (ii) after it is first programmed; (iii) after it is first erased for previously programmed cell. (d) The V_{th} after overwriting operations when 1 initial P/E cycle is performed.

tor. With the increase in the number of overwriting operations, all possible overwriting operations are executed until threshold voltages of all different initial P/E cycles are the same. For example, when 1 initial P/E cycle is performed on a floating gate transistor, there are 2 possible P/E sequences which are either P or E. The P represents the program operation and the E represents the erase operation. When 2 overwriting operations are executed, there are 3 possible P/E sequences which include PE, EE and EP. The PE indicates that the program operation is performed first and then the erase operation is performed. The number of P/E sequences at 1–10 P/E cycles is illustrated in Figure 1(b).

It is channel hot electron injection that is utilized to the program operation in the floating gate transistor, increasing electrons in the floating gate [6]. The Luck-Electron Hot Carrier Injection model is used for simulating the program operation. The voltage value of the control gate, the drain and source in the program operation is 10 V, 5 V and 0 V, respectively. The typical erase operation to move electrons from the floating gate to the source diffusion is accomplished by Fowler-Nordheim (FN) tunneling [7]. The FN model and band to band tunneling model are applied to the simulation of the erase operation. 0 V is applied to the gate of the floating gate transistor in the erase operation, and the voltage value of the source is 10 V. The drain is unconnected and in the high-impedance state.

The V_{th} of the floating gate transistor can be extracted by calculating the maximum slope of the I_d-V_g curve, and getting the difference of the intercept with the X axis of the curve and half of the V_{ds} [8]. Figure 1(c) shows the I_d-V_g characteristics of the floating gate transistor (i) when it is virgin; (ii) after it is first programmed; (iii) after it is first erased for previously programmed cell. The drain-to-source voltage V_{ds} is 0.15 V.

Results and discussion. When 1 initial P/E cycle is performed on a floating gate transistor, there are 2 P/E sequences which are either P or E, thus the minimum probability of restoring the content of the initial P/E cycle in one floating gate cell is 1/2. By detecting the V_{th} for 9.803 or 1.425 V, the initial P/E cycle can be 100% restored to P or E. After all possible overwriting operations are executed, it is observed that the EPEPE are the shortest P/E sequence which makes threshold voltages be the same as 3.753 V and minimizes the recovery probability. By comparison, the V_{th} difference between P and E is maximum and recov-

ery probability is still 100% after the EEEEE is overwritten. As shown in Figure 1(d), the $V_{\rm th}$ difference between P and E is respectively 0 V and 0.78 V after EPEPE or EEEEE is overwritten. What is more, when 2–4 initial P/E cycles are performed on a floating gate transistor, it is observed that the EPEPE is also the shortest P/E sequence which makes the threshold voltages of all possible initial P/E cycles be the same and minimizes the recovery probability.

If the number of initial P/E cycles is known, the possible P/E sequences would be known according to the principle of programming operations. A database of P/E sequences and threshold voltages will be created. In this case, the initial P/E sequence in a floating gate transistor can be 100% restored by detecting the $V_{\rm th}$. If the number of different initial P/E sequences is M, the minimum probability of recovering initial P/E sequences is $1/M$. Though different initial P/E cycles have been performed on a floating gate transistor, it can be found that threshold voltages tend to be the same by using a specific P/E sequence to overwrite initial P/E cycles, which is defined as the centralized phenomenon of threshold voltages. Figure 1(d) also presents the centralized phenomenon of the $V_{\rm th}$ after overwriting EPEPE when 1 initial P/E cycle is performed. The specific P/E sequence used as overwriting operations, EPEPE, minimizes probability of of recovering initial P/E sequences in a floating gate transistor. Based on the idea of mathematical introduction, the EPEPE is still applicable to N (N>4) initial P/E cycles.

Conclusion. In this work, the effects of the overwriting operations performed on a floating gate transistor are studied so as to eliminate data remanence. We define the centralized phenomenon of threshold voltages. In addition, based on the analysis of the probability of recovering the initial P/E cycles, the specific P/E sequence, EPEPE, is suggested as optimal overwriting operation for eliminating data remanence in a floating gate transistor, and the recovery probability is reduced effectively. The residual characteristics of floating gate transistors are improved by the method proposed in this work, which will have important applications in the field of information security for non-volatile memories.

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