SCIENCE CHINA
Information Sciences

• RESEARCH PAPER •

June 2018, Vol. 61 062401:1–062401:9
doi: 10.1007/s11432-016-9106-x

Impact of self-heating effects on nanoscale Ge p-channel FinFETs with Si substrate

Longxiang YIN, Lei SHEN, Hai JIANG, Gang DU & Xiaoyan LIU*

Institute of Microelectronics, Peking University, Beijing 100871*, China*

Received 13 December 2016/Revised 17 March 2017/Accepted 4 May 2017/Published online 20 November 2017

Abstract In this paper, self-heating effects (SHE) in nanoscale Ge p-channel FinFETs with Si substrate are evaluated by TCAD simulation. Hydrodynamic transport with modified mobilities and Fourierś law of heat conduction with modified thermal conductivities are used in the simulation. Ge p-channel single-fin FinFET devices with different S/D extension lengths and fin heights, and multi-fin FinFETs with different fin numbers and fin pitches are successively investigated. Boundary thermal resistances at source, drain and gate contacts are set to 2000 $\mu m^2K/W$ and the substrate thermal boundary condition is set to 300 K so that the source and drain heat dissipation paths are the first two heat dissipation paths. The results are listed below: (i) 14 nm Ge p-channel single-fin FinFETs with a 47 nm fin pitch experience 9.7% on-state current degradation. (ii) Considering the same input power, FinFETs with a longer S/D extension length show a higher lattice temperature and a larger on-state current degradation. (iii) Considering the same input power, FinFETs with a taller fin height show a higher lattice temperature. (iv) The temperature in multi-fin FinFET devices will first increase then saturate with the increasing fin number. At last, thermal resistances in Ge p-channel single-fin FinFETs and multi-fin FinFETs are investigated.

Keywords Germanium, FinFET, self-heating effect, thermal resistance, TCAD

Citation Yin L X, Shen L, Jiang H, et al. Impact of self-heating effects on nanoscale Ge p-channel FinFETs with Si substrate. Sci China Inf Sci, 2018, 61(6): 062401, doi: 10.1007/s11432-016-9106-x

1 Introduction

Many high-mobility materials [1–6], such as Germanium, III-V are widely used as alternative Si channel materials to improve the device current density. Germanium (Ge) is a promising candidate of sub-14 nm technology for the p channel device due to its high hole mobility. 3D device structures such as FinFETs, nanowires [7–12] are used to strengthen the electrostatic control and improve the subthreshold properties. However, serious self-heating effects (SHE) are predictable [13–18] due to new materials and non-planar structures. For Germanium, bulk thermal conductivity is 53 W/m/K [19], lower than Silicon (148 W/m/K) [19], which means a weaker ability to dissipate heat out of hotspots. A more serious SHE can be expected in Ge FinFETs than in Si FinFETs. Although some experimental studies have shown serious SHEs in Ge FinFETs [15, 20], the systematical investigation of geometry impact on self-heating in Ge FinFETs is not yet reported. In this work, 3D electro-thermal device simulations are performed to investigate the SHE in the 14 nm Ge p-channel FinFETs. The SHEs in single-fin FinFETs and multi-fin FinFETs are evaluated. In these simulations, lattice temperature, on-current degradation, and thermal resistance are investigated.

* Corresponding author (email: xyliu@ime.pku.edu.cn)

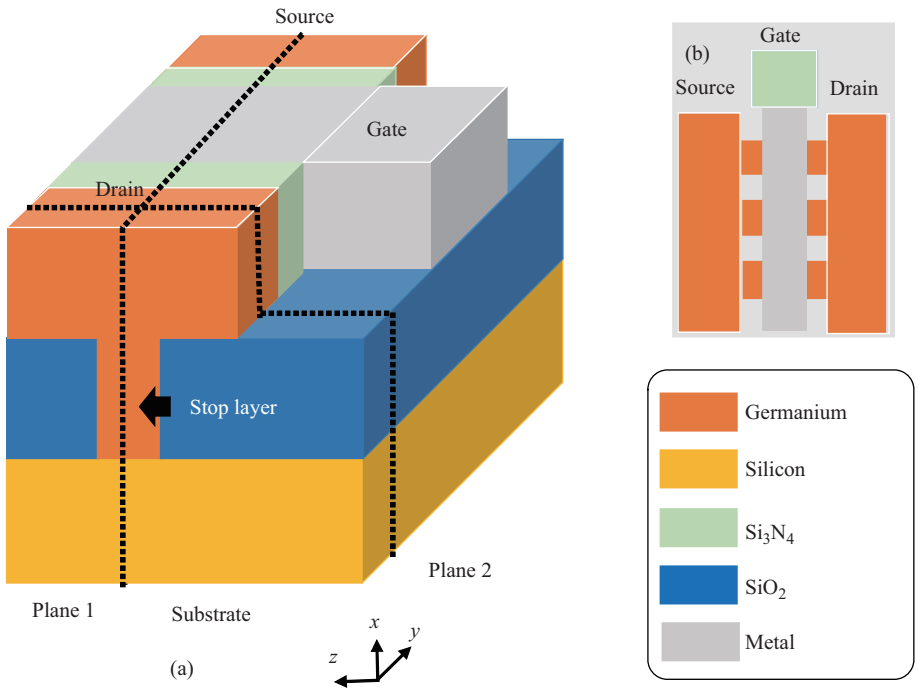

Figure 1 (Color online) Schematic structure of the 14 nm Ge p-channel FinFET. The structure parameters are listed in Table 1.

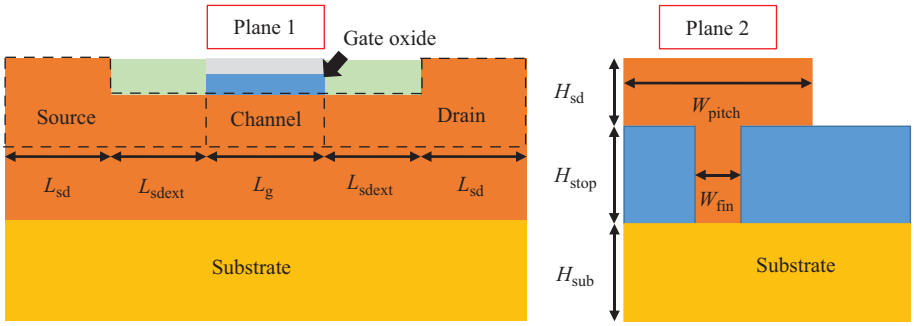

Figure 2 (Color online) Cross-sectional views at Planes 1 and 2. The definitions of the structure parameters are presented.

2 Device structure and simulation method

Figure 1 shows the schematic FinFET structure used in our simulation, where the cross-sectional views at Planes 1 and 2 are shown in Figure 2. The structure parameters are listed in Table 1 and their definitions can be found in Figure 2.

We use Sentaurus TCAD [21] to perform the 3D electro-thermal simulations. In the simulations, the semi-classical hydrodynamic transport model is used. Arora Model [22] (low-field mobility model), Enhanced Lombardi Model [23] (perpendicular-field dependent mobility model) and Extended Canali Model [24] (lateral-field dependent mobility model) are included, which respectively characterize the impact on carrier transport by phonon scattering, ionized impurity scattering, surface roughness scattering and surface phonon scattering. The mobility model parameters are listed in Table 2. All the parameters in the Enhanced Lombardi Model for holes are adjusted according to [25]. Hole saturation velocity in the Extended Canali Model is adjusted to 1.4×10^7 cm/s and default values are used in the other parameters not listed in Table 2, which are chosen to make sure that the device characteristics meet the requirements in ITRS 2013 [1)]. Besides, quantum correction is considered by using the density gradient method. The gate dielectric used in the simulation is SiO_2 and the interface defects are not considered. Figure 3 shows

1) ITRS. www.itrs2.net/itrs-reports.html, ITRS Reports, 2013.

Table 1 Structure parameters of the simulated FinFET

Structure parameter	Value
Raised S/D height, $H_{\rm sd}$	52 nm
Stop layer height, $H_{\rm stop}$	40 nm
Substrate layer height, $H_{\rm sub}$	40 nm
Fin height, $H_{\rm fin}$	42 nm
Raised S/D length,$L_{\rm sd}$	20 nm
S/D extension length, $L_{\rm sdext}$	20 nm
Gate length, L_g	20 nm
Pitch, $W_{\rm pitch}$	47 nm
Fin width, $W_{\rm fin}$	7 nm
Channel doping, n type	$1\times10^{15}{\rm cm}^{-3}$
Stop layer doping, n type	$1\times10^{18}{\rm cm}^{-3}$
Source/drain doping, p type	$2\times10^{19}{\rm cm}^{-3}$
Gate oxide thickness (EOT)	0.68 nm

Table 2 Mobility model parameters [a)]

Parameter	Unit	Hole	Parameter	Unit	Hole
Arora Model			Extended Canali Model		
$A_{\rm min}$	${\rm cm}^2/{\rm Vs}$	1900	$\nu_{\rm sat}$	cm/s	1.4×10^7
α_m	1	-2.3	$\beta_{\rm exp}$	${\rm cm}^{5/3}{\rm V}^{-2/3}{\rm s}^{-1}$	0.17
Enhanced Lombardi Model					
B	cm/s	1.993×10^5	A	1	1.5
C	${\rm cm}^{5/3}{\rm V}^{-2/3}{\rm s}^{-1}$	4875	$\alpha_\perp$	${\rm cm}^3$	0
N_0	${\rm cm}^{-3}$	1	N_l	${\rm cm}^{-3}$	1
N_2	${\rm cm}^{-3}$	1	ν	1	1
λ	1	0.0317	η	${\rm V}^2{\rm cm}^{-1}{\rm s}^{-1}$	2.0546×10^{30}
k	1	1	$a_{\rm other}$	1	0
δ	${\rm cm}^2/{\rm Vs}$	1.705×10^{11}	$l_{\rm crit}$	cm	1×10^{-7}

a) Other mobility parameters not listed here are default values in Sentaurus [21].

the I_d-V_g characteristics of a single-fin 14 nm Ge p-channel FinFET and it shows satisfactory on-state and off-state performance which meet the ITRS requirements.

Degraded thermal conductivity considering classical size effects is utilized in the channel region and the stop layer region instead of the bulk thermal conductivity in this simulation. It is 3.6 W/m/K calculated by the model proposed in [26]. The bulk Ge thermal conductivity (53 W/m/K) is used in the S/D region and the bulk Si thermal conductivity (148 W/m/K) in the substrate region.

Thermal boundary condition of contacts is very important in the electro-thermal simulations. Lumped thermal resistance is mostly used [26–29]. In this work, we use equivalent boundary thermal resistances to characterize the thermal behaviors at source, drain and gate contacts. Heat sink boundary condition of 300 K is considered at the bottom of the substrate [23, 30].

In a normal-working device, source and drain contacts are the main heat flux paths [31]. Figure 4 shows the relationshsips of the heat flux percentages of these four contacts with different boundary thermal resistances. Thermal resistances lower than 2800 $\mu{\rm m}^2{\rm K/W}$ are reasonable. In the following simulation, we use the boundary thermal resistance of 2000 $\mu{\rm m}^2{\rm K/W}$ to investigate the self-heating effects in the 14 nm Ge pFinFETs.

3 Results and discussion

3.1 SHE in single fin devices

Figure 5 compares the spatial temperature distributions of the single-fin FinFET at different gate voltages.

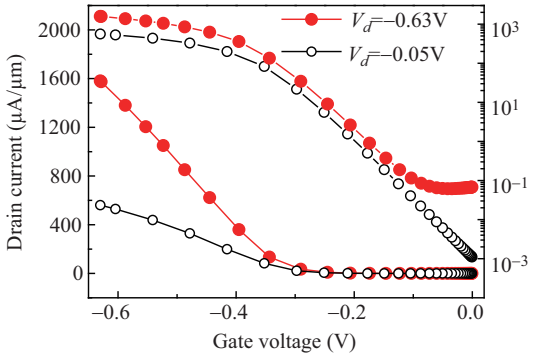

Figure 3 (Color online) I_d-V_g characteristics of the simulated 14 nm Ge p-channel FinFET. On-state current density is 1581 μA/μm. Off-state leakage current density is lower than 100 nA/μm. Subthreshold Slope is 76.2 mV/dec and DIBL is 4.5 mV/V.

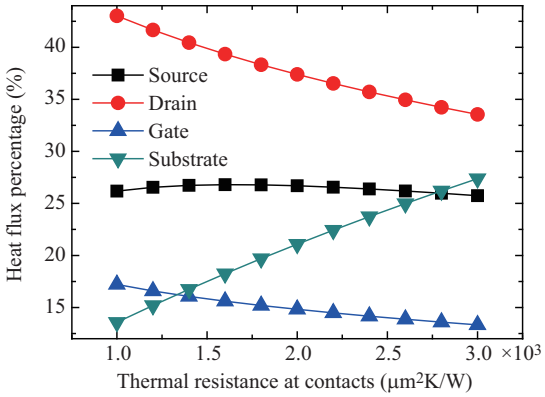

Figure 4 (Color online) Heat flux percentage in four different heat dissipation paths with boundary thermal resistances varying from 1000 to 3000 μm^{2}K/W. Heat sink boundary condition of 300 K is considered at the bottom of the substrate.

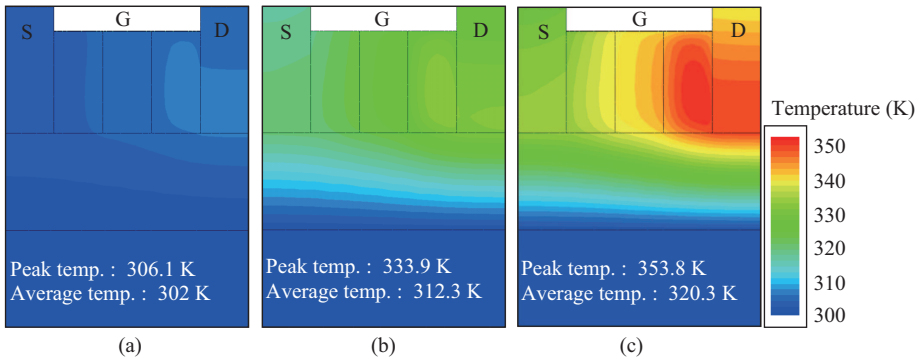

Figure 5 (Color online) Spatial temperature distributions of the Ge p-channel single-fin 14 nm FinFET in Plane 1 at different gate voltages. Here V_d is −0.63 V. (a) V_g = −0.35 V; (b) V_g = −0.5 V; (c) V_g = −0.63 V.

The input power increases with the increasing gate voltage, and the device will experience a much larger temperature. The peak temperature in FinFET can be 353.8 K at a −0.63 V gate voltage. The hotspots are distributed in the channel near the drain region, the drain extension region and even in the drain region in all the three conditions. This can be understood that carriers get most of energy from the peak electric field which locates near the junction between the channel region and the drain extension region and the heated carriers cannot have enough chance to exchange energy to the lattice by scatterings till they approach to the drain contact.

Figure 6 compares the $I_d - V_d$ characteristics with and without the self-heating effect in the single-fin FinFET. This figure shows that the self-heating effects can lead to an obvious current degradation in the Ge p FinFETs.

Take the four characterized scattering mechanisms into consideration. The phonon scattering and the surface phonon scattering are inelastic scattering. Along with the increasing temperature, both of them will increase due to the more frequent lattice vibrations and this will degrade the carrier transport and lead to the current degradation. However, the ionized impurity scattering and the surface roughness scattering are elastic scattering. They are not sensitive to the temperature and have no contribution to the current degradation caused by SHE.

On-state current degradation rate ΔI can be calculated as follows:

$$\Delta I = \frac{\mathrm{Id_{normal}} - \mathrm{Id_{heat}}}{\mathrm{Id_{normal}}} \times 100\%. \tag{1}$$

In (1), $\mathrm{Id_{normal}}$ refers to the on-state current without considering the impact of SHE and Idheat refers to

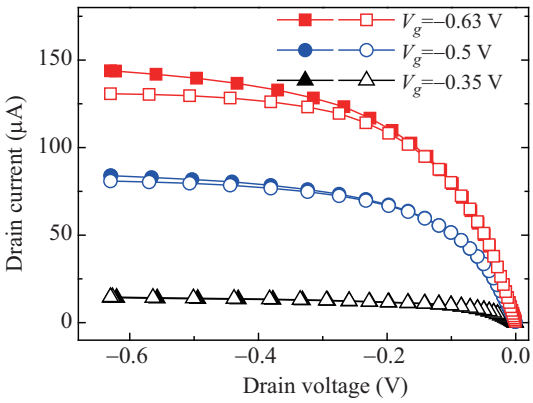

Figure 6 (Color online) $I_d - V_d$ characteristics of a 14 nm single-fin FinFET comparing the situations with and without self-heating effects.

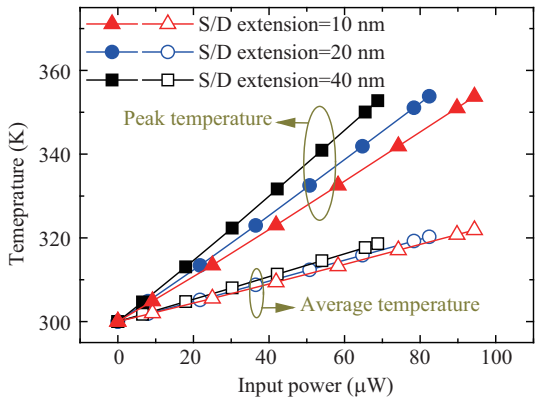

Figure 7 (Color online) Relationships between the peak, average temperature and the input power with different L_{sdext}s. Here V_{gs} is −0.63 V.

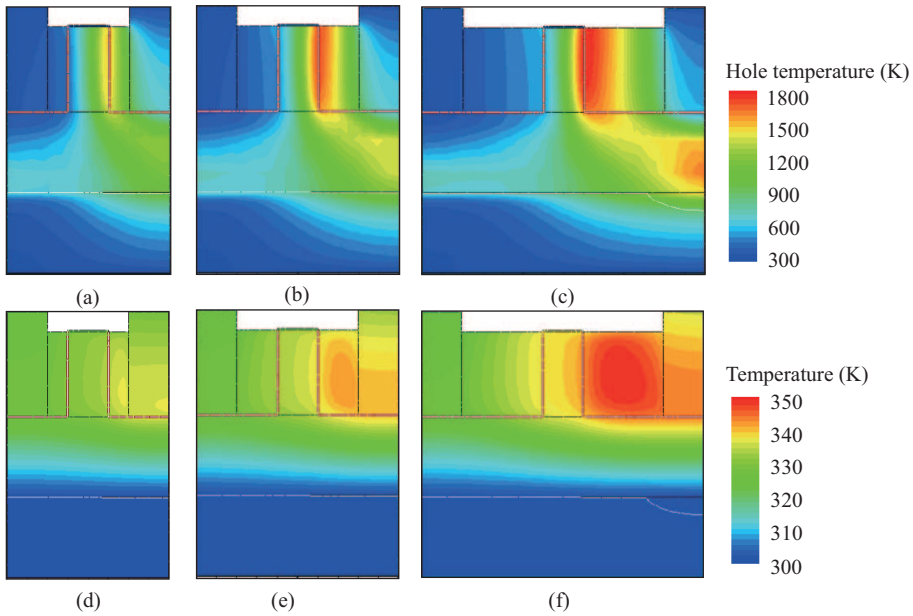

Figure 8 (Color online) Hole temperature distributions (a)–(c) and lattice temperature distributions (d)–(f) in the Ge FinFETs with three different L_{sdext}s 10, 20, 40 nm from left to the right, where the input powers are all 60 μW.

the on-state current considering the impact of SHE. We can see that the largest drain current degradation can be 9.1% at a V_g of −0.63 V. Therefore, self-heating effects in the 14 nm Ge p-channel FinFETs should not be neglected.

On-state current of FinFET structures varies with different S/D extension lengths and fin heights, which will lead to variations in SHEs. In the following, we will investigate the SHEs of the Ge p-channel single-fin FinFET with different S/D extension lengths (L_{sdext}) and fin heights (H_{fin}). The results can be used to optimize the structure of Ge p-channel FinFETs.

First, we will investigate the self-heating effects in Ge FinFETs with different S/D extension lengths.

Figure 7 shows the relationships of the peak, average temperature with the input power. Three different L_{sdext}s 10, 20, 40 nm are compared. The gate voltage is −0.63 V in all three situations and the drain voltage varies from 0 to −0.63 V. We can see that considering the same input power, FinFETs with a longer L_{sdext} experience a higher average and peak temperature.

Figure 8 shows the spatial distributions of hole temperature (a)–(c) and the lattice temperature (d)–(f) in the Ge FinFETs with three different L_{sdext}s 10, 20, 40 nm from left to the right. The input power

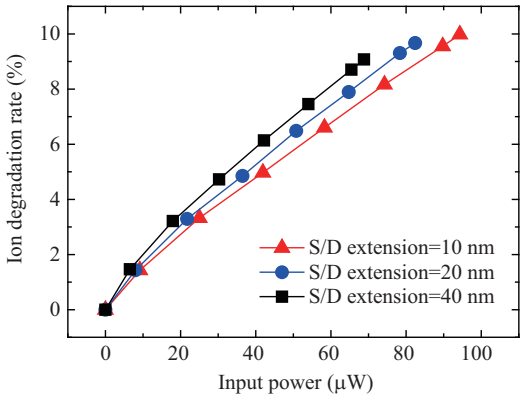

Figure 9 (Color online) Comparison of the different on-state current degradation rates with different L_{sdext}s.

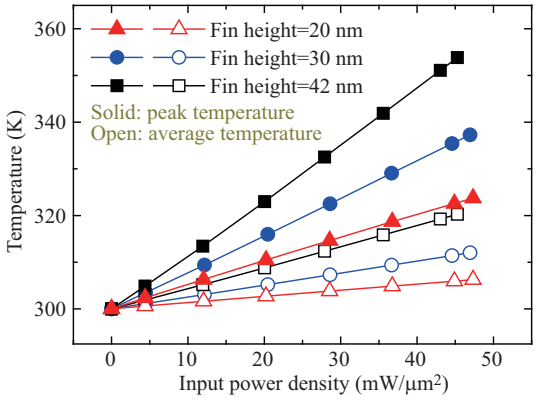

Figure 10 (Color online) Relationships between the peak, average temperatures and the input power density of the channel cross section in devices with different H_{fin}s.

considered here is 60 μW. We can see that with the same input power, the longer S/D extension length leads to a much higher hole temperature and lattice temperature. In this situation, the ΔI of the Ge FinFETs with three different L_{sdext}s 10, 20, 40 nm are 7%, 7.65%, 8.27% respectively, which shows that a longer S/D extension length can also lead to a larger on-state current degradation. The relationships between the on-state current degradation and the input power in Ge FinFETs with three different L_{sdext}s are shown in Figure 9.

Next, the self-heating effects in the Ge FinFETs with different fin heights are investigated.

To exclude the impact of the different input power brought in by different fin heights, we compare the relationships between the peak, average temperature and the input power density of the channel cross section in the FinFETs with different fin heights, which is shown in Figure 10. The input power density of the channel cross section is calculated as the result of the input power divided by the cross section area of the fin (W_{fin}*H_{fin}). Considering the same input power density, the temperature in a taller FinFET is much higher.

3.2 SHE in multi-fin devices

In the following, we investigate the self-heating effects in the multi-fin FinFET devices. The S/D contact sizes and substrate area size are in proportion to the fin number while the gate contact size keeps 20 nm × 20 nm in the multi-fin devices. The variation tendency of the peak and average temperatures along with the different fin numbers are shown in Figure 11, where three different fin pitches 47, 67 and 87 nm are simulated. It first presents a rising trend and then saturates with 5 and more fins in the three different situations. The saturation temperature reveals the existence of thermal crosstalk. Besides, multi-fin FinFETs with a smaller fin pitch show a much higher temperature.

We compare the spatial temperature distributions along $0.5\times H_{sd}$ of Plane 2 in Figure 12. In the figure, each peak reflects a location of a fin. The spatial temperature distributions of multi-fin FinFETs with different fin numbers are compared in Figure 12(a). The fin pitch is 47 nm. We can see that the temperature keeps growing with the increasing fin number. The difference from 1 to 5 fin is much larger than that from 5 to 11 fin, which reflects the same trend as in Figure 11. Figure 12(b) shows the temperature distributions of 5-fin FinFETs with 47 and 57 nm fin pitch.

Figure 13 compares the current degradations in the multi-fin FinFETs with three different fin pitches. We can see that the current degradation is larger in the FinFETs with a smaller fin pitch. The on-state current degradation increases with the increasing fin number and the thermal crosstalk will lead to the saturation of on-state current degradation. Large fin pitch can effectively minimize the current degradation in the multi-fin FinFETs.

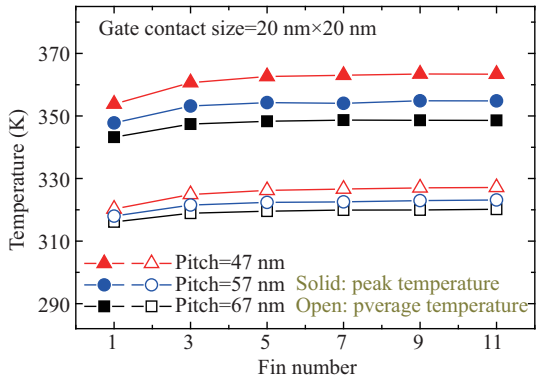

Figure 11 (Color online) Relationships between the peak, average temperatures and the fin number. Different fin pitches are compared.

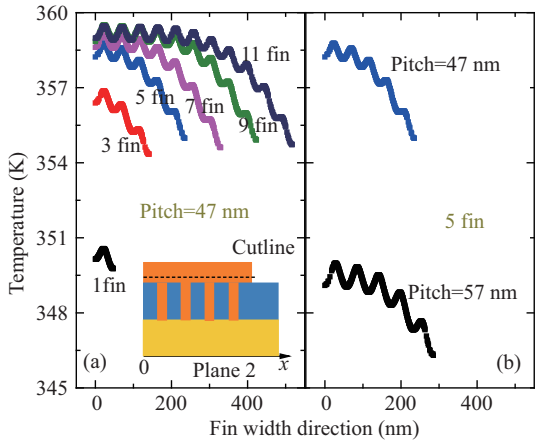

Figure 12 (Color online) Comparison of (a) temperature distributions of multi-fin FinFETs with different fin numbers and (b) temperature distributions of multi-fin FinFETs with different fin pitches along the cutline shown in the inset figure.

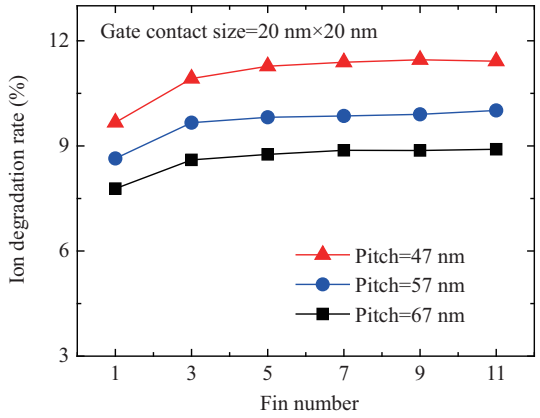

Figure 13 (Color online) Comparison between different on-state current degradations of multi-fin FinFETs with different fin pitches.

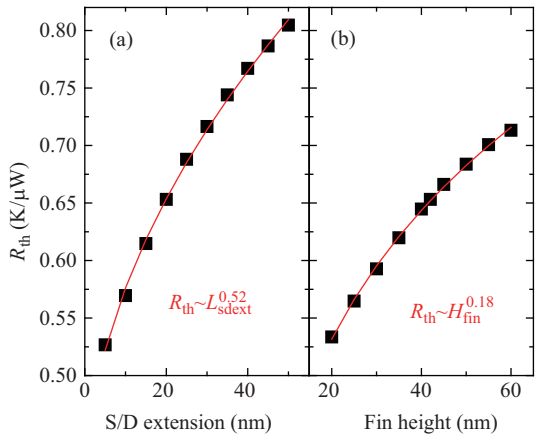

Figure 14 (Color online) Relationships between thermal resistance and the $L_{\rm sdext}$ (a) and the $H_{\rm fin}$ (b) in the single-fin FinFETs. Thermal resistance has exponential relationships with the two factors. The exponential indexes are 0.52 and 0.18 respectively.

3.3 Thermal resistances

The thermal resistances of the single-fin FinFETs and the multi-fin FinFETs are investigated.

The thermal resistance $R_{\rm th}$ is defined as below:

$$R_{\rm th} = \frac{\Delta T}{\Delta Q}. \tag{2}$$

In (2), T and Q respectively refer to the peak temperature and the input power of the device.

The relationships between the thermal resistances of the Ge p-channel single-fin FinFETs with different $L_{\rm sdext}$s are shown in Figure 14(a), which shows that the FinFETs with a longer $L_{\rm sdext}$ have a larger thermal resistance. The thermal resistance has an exponential relationship with $L_{\rm sdext}$, where the exponential index is 0.52.

Figure 14(b) also shows an exponential relationship between the thermal resistances of the Ge p-channel single-fin FinFETs and the different $H_{\rm fin}$s, where the exponential index is 0.18. The FinFETs with a

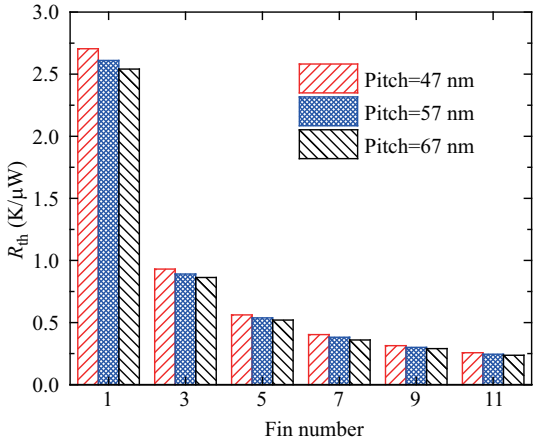

Figure 15 (Color online) Variation tendency of the thermal resistances in multi-fin FinFETs with different fin numbers. Different fin pitches are compared.

larger fin height have a larger thermal resistance, which is the result of a fixed gate contact area and a larger input power.

Figure 15 shows the relationship between the thermal resistances and the different fin numbers and fin pitches. We can see that the device with a smaller fin pitch has a much larger thermal resistance, which leads to a higher device temperature in Figure 11. It also shows that the thermal resistance of device decreases with the fin number and the decrement becomes smaller with the increasing fin number.

4 Conclusion

In this paper, the self-heating effects in the 14 nm Ge p-channel FinFETs are investigated. Self-heating effects are serious in 14 nm Ge p-channel FinFETs and they can lead to the on-state current degradation. Due to the longer distance which allows the carriers release more energy to the lattice, FinFETs with a longer S/D extension length will have more generated heat considering the same input power, which will lead to a higher lattice temperature and a larger current degradation. Considering the same input power density of channel cross section, FinFETs with a taller fin height also have a higher lattice temperature. Along with the increasing fin number, the temperature in the multi-fin FinFETs will first increase then saturate. The thermal crosstalk in the multi-fin FinFETs can lead to the saturation of the on-state current degradation. A larger fin pitch will minimize the current degradation. Thermal resistance has exponential relationships with the S/D extension length and the fin height in the 14 nm Ge p-channel FinFET, where the exponential indexes are 0.52 and 0.18 respectively.

Acknowledgements This work was supported by National Natural Science Foundation of China (Grant Nos. 61404005, 61674008, 61421005) and National High Technology Research and Development Program of China (863) (Grant No. 2015AA016501).

Conflict of interest The authors declare that they have no conflict of interest.

References

1 Yeo Y-C, Gong X, van Dal Mark J H, et al. Germanium-based transistors for future high performace and low power logic applications. In: Proceedings of IEEE International Electron Device Meeting, Washington, 2015. 28–31
2 Kim R, Avci U E, Young I A. CMOS performance benchmarking of Si, InAs, GaAs, and Ge nanowire n- and pMOSFETs with Lg=13 nm based on atomistic quantum transport simulation including strain effects. In: Proceedings of IEEE International Electron Device Meeting, Washington, 2015. 875–878
3 Wu H, Luo H, Zhou H, et al. First experimental demonstration of Ge 3D FinFET CMOS circuits. In: Proceedings of Symposium on VLSI Technology, Kyoto, 2015. 58–59
4 Kang E S, Anwar S, Ahmadi M T, et al. The impact of germanium in strained Si/relaxed Si1-xGex on carrier performance in nondegenerate and degenerate regimes. J Semicond, 2013. 34: 062001

5 Waldron N, Sioncke S, Franco J, et al. Gate-all-around InGaAs nanowire FETS with peak transconductance of 2200μS/μm at 50 nm Lg using a replacement Fin RMG flow. In: Proceedings of IEEE International Electron Device Meeting, Washington, 2015. 799–802

6 Zhou J H, Chang H D, Zhang X F, et al. Fabrication of a novel RF switch device with high performance using In0.4Ga0.6As MOSFET technology. J Semicond, 2016. 37: 024005

7 Sasaki Y, Ritzenthaler R, Keersgieter A D, et al. A comparison of arsenic and phosphorus extension by room temperature and hot ion implantation for NMOS Si bulk-FinFET at N7 (7 nm) technology relevant fin dimensions. In: Proceedings of Symposium on VLSI Technology, Kyoto, 2015. 30–31

8 Veloso A, Hellings G, Cho M J, et al. Gate-all-around NWFETs vs. Triple-gate FinFETs: junctionless vs. extensionless and conventional junction devices with controlled EWF modulation for multi-Vt CMOS. In: Proceedings of Symposium on VLSI Technology, Kyoto, 2015. 138–139

9 Mertens H, Ritzenthaler R, Hikavyy A, et al. Gate-all-around MOSFETs based on vertically stacked horizontal Si nanowires in a replacement metal gate process on bulk Si substrates. In: Proceedings of Symposium on VLSI Technology, Honolulu, 2016. 158–159

10 Yakimets D, Eneman G, Schuddinck P, et al. Vertical GAAFETs for the ultimate CMOS scaling. IEEE Trans Electron Dev, 2015, 62: 1433–1439

11 Deleonibus S. Looking into the future of Nanoelectronics in the Diversification Efficient Era. Sci China Inf Sci, 2016, 59: 061401

12 Cheng K G, Khakifirooz A. Fully depleted SOI(FDSOI) technology. Sci China Inf Sci, 2016, 59: 061402

13 Stellari F, Jenkins K A, Weger A J, et al. Self-heating measurement of 14-nm FinFET SOI transistors using 2-D time-resolved emission. IEEE Trans Electron Dev, 2016, 63: 2016–2022

14 Wahab M A, Shin S H, Alam M A. 3D modeling of spatio-temporal heat-transport in III-V gate-all-around transistors allows accurate estimation and optimization of nanowire temperature. IEEE Trans Electron Dev, 2015, 62: 3595–3604

15 Jang D, Bury E, Ritzenthaler E, et al. Self-heating on bulk FinFET from 14nm down to 7 nm node. In: Proceedings of IEEE International Electron Device Meeting, Washington, 2015. 289–292

16 Jiang H, Xu N, Chen B, et al. Experimental investigation of self-heating effect (SHE) in multiple-fin SOI FinFETs. Semicond Sci Tech, 2014. 29: 115021

17 Ma L, Feng S W, Zhang Y M, et al. Evaluation of the drain-source voltage effect on AlGaAs/InGaAs pHEMTs thermal resistance by the structure function method. J Semicond, 2014, 35: 094006

18 Gong X Q, Feng S W, Yue Y, et al. Thermal analysis in high power GaAs-based laser diodes. J Semicond, 2016. 37: 044011

19 Dames C, Chen G. Theoretical phonon thermal conductivity of Si/Ge superlattice nanowires. J Appl Phys, 2004. 95: 682–693

20 Bury E, Kaczer B, Mitard J, et al. Characterization of self-heating in high-mobility Ge FinFET pMOS devices. In: Proceedings of Symposium on VLSI Technology, Kyoto, 2015. 60–61

21 Synopsys. Sentaurus device user guide, v D-2010.03, 2010

22 Arora N D, Hauser J R, Roulston D J. Electron and hole mobilities in silicon as a function of concentration and temperature. IEEE Trans Electron Dev, 1982, ED-29: 292–295

23 Darwish M N, Lentz J L, Pinto M R, et al. An improved electron and hole mobility model for general purpose device simulation. IEEE Trans Electron Dev, 1997, 44: 1529–1538

24 Canali C, Majni G, Minder R, et al. Electron and hole drift velocity measurements in silicon and their empirical relation to electric field and temperature. IEEE Trans Electron Dev, 1975, 22: 1045–1047

25 Hellings G, Eneman G, Krom R, et al. Electrical TCAD simulations of a germanium pMOSFET technology. IEEE Trans Electron Dev, 2010, 57: 2539–2546

26 Wang L P, Brown A R, Nedjalkov M, et al. Impact of self-heating on the statistical variability in bulk and SOI FinFETs. IEEE Trans Electron Dev, 2015, 62: 2016–2112

27 Marco G P, Alessandro C. Quantum simulation of self-heating effects in rough Si nanowire FETs. In: Proceedings of IEEE International Workshop on Computational Electronics, Paris, 2014. 65–67

28 Fiegna C, Yang Y, Sangiorgi E, et al. Analysis of self-heating effects in ultrathin-body SOI MOSFETs by device simulation. IEEE Trans Electron Dev, 2008, 55: 233–244

29 Chiang T Y, Banerjee K, Saraswat K C. Analytical thermal model for multilevel VLSI interconnects incorporating via effect. IEEE Electron Dev Lett, 2002, 23: 31–33

30 Sadi T, Thobel J L, Dessenne F. Microscopic simulation of electron transport and self-heating effects in InAs nanowire MISFETs. In: Proceedings of IEEE International Conference on Simulation of Semiconductor Processes and Devices, Bologna, 2010. 107–110

31 Shrivastava M, Agrawal M, Mahajan M, et al. Physical insight toward heat transport and an improved electrothermal modeling framework for FinFET architectures. IEEE Trans Electron Dev, 2012, 59: 1353–1363