SCIENCE CHINA
Information Sciences

• RESEARCH PAPER •

June 2018, Vol. 61 060419:1–060419:9
https://doi.org/10.1007/s11432-018-9430-2

Special Focus on Flexible Electronics Technology

Parylene-MEMS technique-based flexible electronics

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Received 10 January 2018/Revised 9 March 2018/Accepted 27 March 2018/Published online 14 May 2018

Abstract This paper reports a novel fabrication strategy for flexible electronics based on the parylene-MEMS (micro-electromechanical system) technique. A set of parylene-filled trenches is used to mechanically connect silicon-based functional units and realize a flexible 4×6 temperature controlling array as a preliminary demonstration. The trench-filling performance of the parylene deposition is carefully studied, and an optimized process is established to minimize the keyhole inside the parylene-filled trench. The effect of trench width on the flexibility and bendability of the prepared flexible electronics devices is analyzed by finite element modeling. Performances of the thermal/electrical isolation and the mechanical connection of the prepared parylene-filled trenches have been tested. The experimental results indicate that the highest thermal isolation efficiency is approximately 72.5% with the 10 paralleled, 7 μm wide and 50 μm deep parylene-filled trenches. The leakage current of the 10 paralleled, 5 μm wide and 100 μm deep parylene-filled trenches is less than 2 pA under a voltage of 100 V. Besides, these parylene-filled trenches acting as the flexible linkage of connected silicon-based functional units exhibit high connection performance without rupture when the loading pressure is under 200 kPa. Due to the powerful silicon microfabrication capability and excellent compatibility of the parylene-MEMS technique, the present flexible electronics strategy holds a promising potential for applications in various areas.

Keywords flexible electronics, parylene, MEMS, trench filling, temperature controlling array

Citation Dong X, Zhang M X, Lei Y H, et al. Parylene-MEMS technique-based flexible electronics. Sci China Inf Sci, 2018, 61(6): 060419, https://doi.org/10.1007/s11432-018-9430-2

1 Introduction

Flexible electronics, which is an electronic device or system that integrates a variety of functions and materials on a flexible substrate to achieve deformability or stretchability, has been widely studied in the past ten years due to its promising applications in electronic artificial skin for robotics [1, 2], implanted devices for neural recording, drug delivery and cell control [3], flexible displays [4, 5], flexible sensors [6, 7]. To achieve high flexibility in electronic devices, various fabrication strategies have been developed [8–10]. Generally, the existing methods can be categorized into two strategies: utilizing organic materials (conducting and semiconducting polymers) [11, 12] and transferring inorganic ultrathin structure (usually semiconductor nanomembranes [13]/nanoribbons [14]) to elastomers such as PDMS (polydimethylsiloxane) and polyimide substrates. Although possessing excellent flexibility due to the

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† Dong X and Zhang M X have the same contribution to this work.

Table 1 Comparisons of the three fabrication strategies for flexible electronics

	Organic semiconductor-based approach	Thin-functional structure transferring approach	MEMS-based hybrid fabrication/integration approach
Materials	Organic semiconductor	Ultrathin inorganic materials, PDMS	Silicon/parylene
Fabrication	Printing and surface modification	Microfabrication and transferring assembly methods	MEMS
Advantages	Intrinsically flexible	High performance (mobility of silicon: 710 $cm^2V^{-1}s^{-1}$ [16])	High and complex performance
	Relatively high stretchability (fracture strain of 800% [11])	Good flexibility (radius of 0.5 mm [17])	Compatible with mass production
Limitation	Limited performance and function (low mobility, recent report of record: 1.32 $cm^2V^{-1}s^{-1}$ [12])	Limited functionality and reliability due to the ultrathin structure	Limited flexibility /stretchability

intrinsic stretchability of polymers, organic materials still face critical challenges in establishing high-performance flexible electronics, especially those where fine feature size and high electrical properties are required. For example, a stretchable polymer semiconducting film supported on a PDMS substrate can be stretched to 200% strain, however, its mobility only reaches a maximum value of 1.32 $cm^2V^{-1}s^{-1}$ at 100% strain, which is far below the carrier mobility of silicon [12]. On the contrary, the method transferring nanomembranes/ribbons to elastomer (usually PDMS) can realize functional structures with high resolution and the electrical performance is as good as the regular silicon devices. However, to fulfill the transfer, the inorganic structure should be as thin as possible, which limits its functionality and reliability. For instance, a sensing system for in vivo electrocorticogram including 128 MOSFETs with doped silicon nanomembranes serving as the active semiconductor material has both flexibility and bioresorbability. However, the threshold voltage, mobility and on/off ratio of this n-doped MOSFET are 1 V, 400 $cm^2V^{-1}s^{-1}$ and 10^8, respectively, indicating limited performance. Additionally, the pinholes in the encapsulating layer may cause failures in leakage currents [15].

This paper reported a novel fabrication strategy for flexible electronics based on the parylene-MEMS technique. A set of parylene-filled trenches was used to mechanically connect silicon-based functional units and realize a flexible 4×6 temperature controlling array as a preliminary demonstration. Preliminary tests demonstrated that excellent thermal/electrical isolation and reliable mechanical connection were successfully achieved. Due to the powerful silicon microfabrication capability and excellent compatibility of the parylene-MEMS technique, the present flexible electronics strategy holds a promising potential for various applications. Table 1 shows the comparison between this novel fabrication approach for flexible electronics and the existed other two strategies.

2 Working principle

The work principle of the proposed parylene-MEMS based flexible electronics was schematically illustrated in Figure 1. A robust parylene-filled-trench technique was used to realize the flexibility of silicon-based functional unit array. Parylene C has been chosen to fill the trench and function as the flexible linkage for the following three reasons: (1) Parylene C, which can be prepared by a CVD (chemical vapor deposition) based process and patterned by oxygen plasma etching, is compatible with the microfabrication process of MEMS [18]. (2) It is easy to implement a conformal deposition of parylene C with a thickness of about tens of microns. (3) The breaking elongation of parylene C is approximately 200%, which makes the parylene C structure workable under a high mechanical load without rupture. Figure 1(b) shows the cross-sectional view of the parylene-MEMS based flexible electronics. The connection between two adjacent units comprises a set of parallel, high-aspect-ratio trenches, which is designed to form a parylene-silicon-parylene sandwich structure after being filled with parylene C. These narrow trenches require only a thin parylene deposition to fill up and the surface of the parylene-silicon-parylene sandwich structure after deposition is flat enough to accomplish the following fabrication, such as patterning,

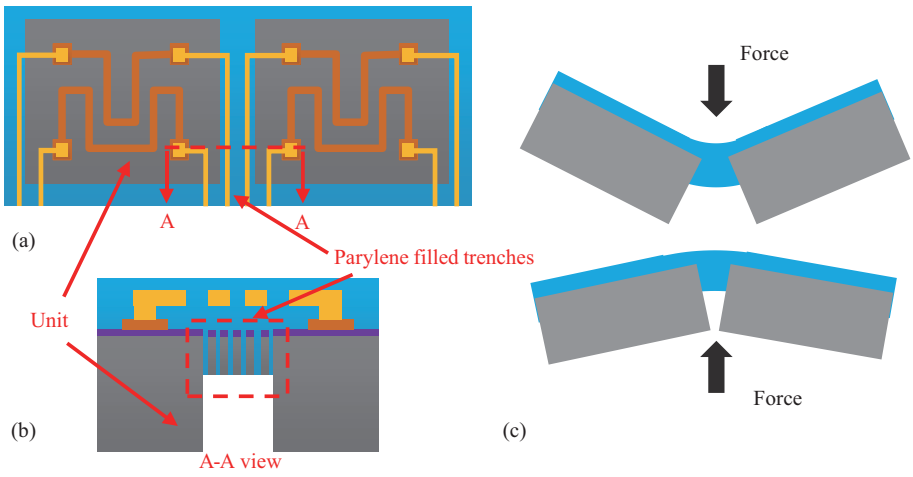


Figure 1 (Color online) Schematic illustration of the work principle of the proposed parylene-MEMS based flexible electronics. (a) Top view of two units and the parylene-filled trenches around them; (b) cross-sectional view of a set of parallel parylene-filled trenches; (c) the bended structure upon applied forces.

metallization [18]. Meanwhile, the parylene C is an excellent passivation material and thereby multi-layer electrical connection can be easily achieved. The silicon beneath the trenches was subsequently removed, leaving the parylene-filled trenches to be the only connection between the adjacent functional units. Further simulation results showed that the flexibility of this functional array was greatly improved after removing the remnant silicon. For specific purposes, a variety of functional structures can be fabricated on the top of each unit in advance. A flexible 4×6 temperature controlling array was fabricated as a preliminary demonstration in this work. As shown in Figure 1(c), the parylene-filled trenches act as a good flexible connection making the prepared device bendable upon the applied forces. The influence of bending direction as well as trench width on the flexibility of the array will be carefully and quantitatively studied in this work.

3 Fabrication and simulation

As a demonstration of the proposed parylene-MEMS based flexible electronics, a 4×6 temperature controlling array was fabricated. Each unit contained two Pt resistors as the heater and the temperature sensor respectively, which can be controlled individually. The functional unit in this work was designed with a relatively large feature size of 2 mm×3 mm, and the size could be further scaled down for specific requirements.

To test the trench-filling performance of parylene, various trenches with different geometrical parameters and profiles were prepared and deposited with parylene. The microfabrication process mainly consisted of three steps: (1) patterning and etching the trenches by DRIE (deep reactive ion etching), (2) depositing parylene C to fill the trenches, and (3) removing the remnant silicon beneath the trench from the back. The samples were diced for the SEM (scanning electron microscope) investigation to obtain detailed structure information. Figure 2 schematically illustrated the overall fabrication process of the flexible temperature controlling array. The substrate adopted in the fabrication was a 4 inch, double polished, single crystal ⟨100⟩ silicon wafer (400 ± 15 μm). A layer of 300 nm silicon oxide was thermally grown on the wafer as the electrical isolation layer firstly. After the first photolithography and sputtering Cr/Pt (20 nm/200 nm), the heating and sensing elements were prepared by a lift-off process (Figure 2(a)). The second photolithography was then applied, followed by the BHF (buffered hydrofluoride acid) etching to make the mask for the trenches. The trenches, with a width of 7 μm and a depth of 50 μm each, were etched by a standard silicon ICP (inductive coupled plasma) dry etching process (Figure 2(b)). The 5 μm thick parylene C was deposited by a vapor deposition machine (PDS 2010, SCS, USA) to fill the trenches, as shown in Figure 2(c). Then, another photolithography and a following 20 min oxygen plasma etch-

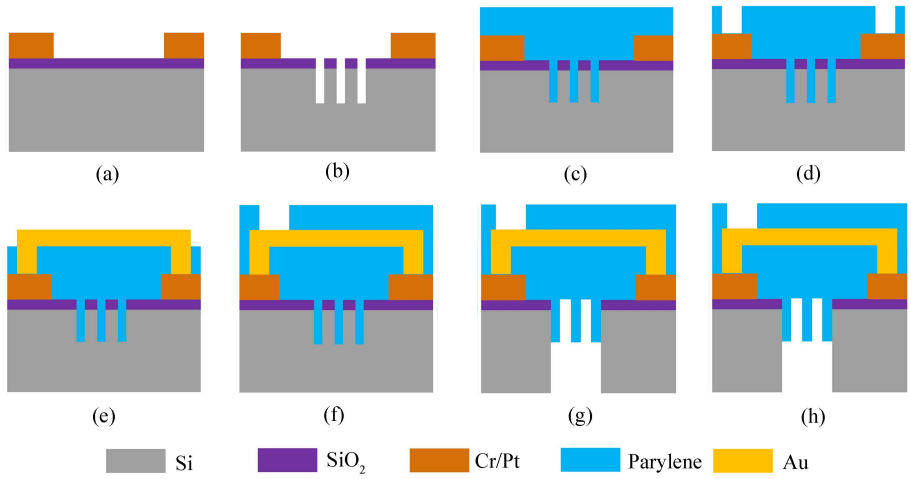


Figure 2 (Color online) Microfabrication process of the flexible temperature controlling array. (a) Metal pattering on the silicon oxide layer; (b) trench etching; (c) parylene deposition to fill the trenches; (d) parylene etching by the oxygen plasma; (e) Au wires electroplating; (f) parylene deposition and patterning; (g)removing the silicon beneath the trench; (h) parylene deposition after removing all the remnant silicon.

ing for selectively etching off the parylene were applied to create the electrical connecting windows as illustrated in Figure 2(d). After wiring the functional units with 4 μm thick gold wires prepared by a standard electroplating process (Figure 2(e)), another 5 μm thick parylene was deposited to protect and passivate the electrical connections. The bonding pads were opened by a selective parylene etching after the fifth photolithography (Figure 2(f)). To remove the silicon beneath the parylene-filled trenches, a precise double-side photolithography on the backside of the wafer was carried out and the silicon was etched off using the DRIE process, as indicated in Figure 2(g). Considering that silicon has a much higher Young's Modulus (190 GPa) than parylene C (3.2 GPa), the high-aspect-ratio silicon structure between the parylene-filled trenches were expected to be etched off in this step to obtain a more flexible connection between the units. As a final step, another parylene layer was deposited after all the remnant silicon was removed to protect the back portion and form a pure parylene connecting structure.

The mechanics of the flexible array can be captured quantitatively using comsol multiphysics software. A three-dimensional FEA (finite element analysis) is used to study the strains and displacements of the deformation model before and after the removal of the remnant silicon, as well as examine the curving degree of the array under different widths of the trench in two bending directions. The FEA model is a 4×6 parylene-silicon array, where pressure in two directions is applied on the surface of the array, causing the array bending toward front side (direction 1) and back side (direction 2) respectively, and the displacement of the whole array in both directions of pressure is measured on condition that the parylene reaches a volume deformation of 3%, which is the boundary of parylene from elastic deformation to plastic deformation. This limit will guarantee that the parylene can be restored after the removal of external forces. The simulation results and analysis will be elaborated in the next section.

4 Results and discussion

The deposition of parylene C is highly conformal, making it an efficient material to fill the narrow high-aspect-ratio trenches with a deposition of a few micrometers. However, a keyhole can be easily formed inside the trench during the trench-filling process [19]. Parylene has been found to grow faster at the trench opening, resulting in the closing of the trench at its opening before the trench was completely filled [20]. Figure 3(a) shows the typical conformal deposition of parylene and the keyhole inside the trench. To study how the geometrical parameters (width, depth, and the slant angle of the side wall) of the trench influenced the conformal deposition, we have defined the "conformal ratio" as X_b/X_t, where X_b and X_t were the thicknesses of the parylene deposited on the side wall near the bottom and the top

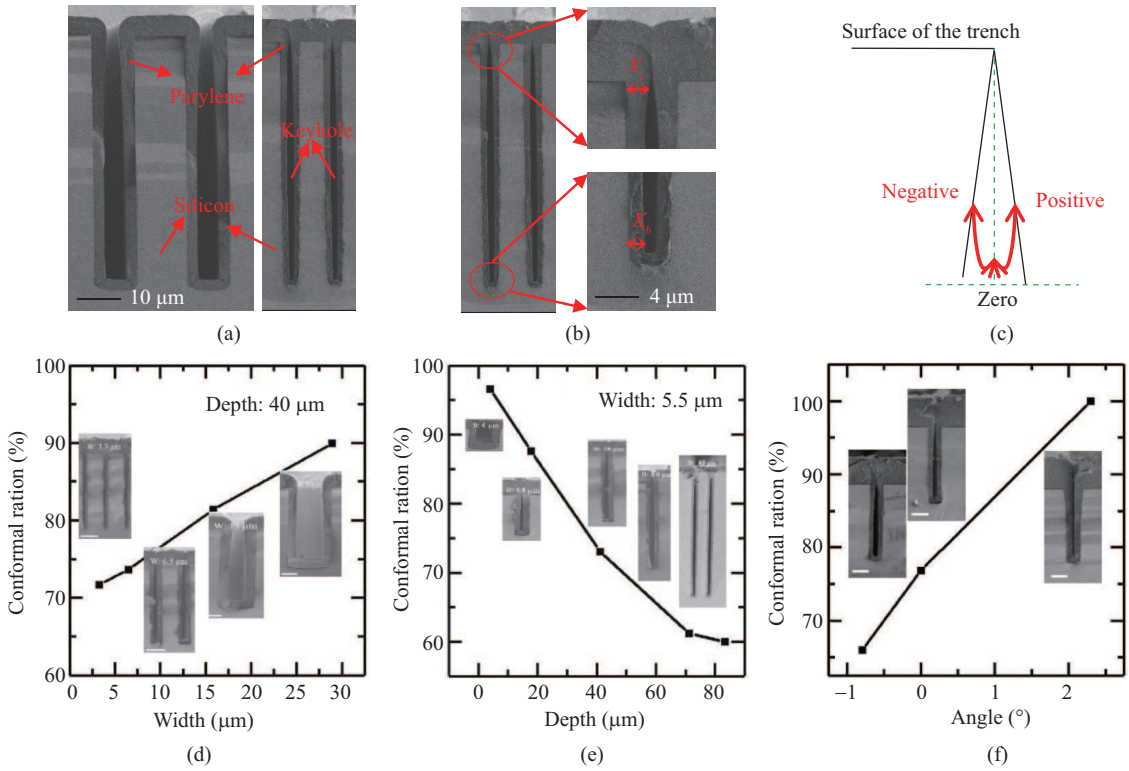
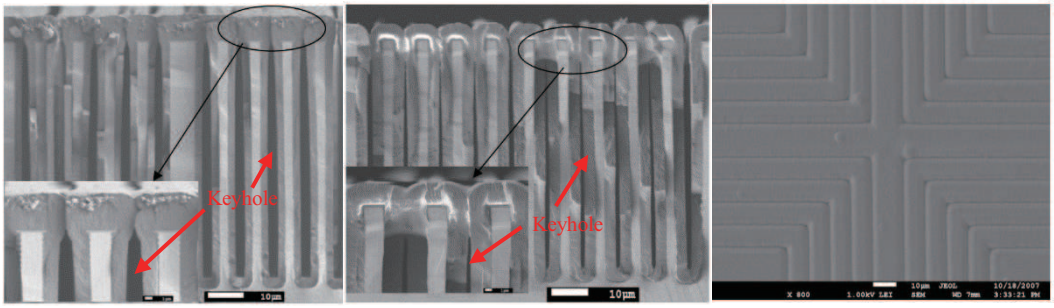


Figure 3 (Color online) Results of the parylene trench-filling experiments. (a) SEM photos of the conformal deposition and the keyhole in the parylene-filled trench; (b) definitions of X_b and X_t; (c) definition of the slant angle; (d) conformal ratios for the cases with different width of the trench: 3.3, 6.5, 15, 30 μm, the depth was 40 μm; (e) conformal ratios for the cases with different depth of the trench: 4, 18, 38, 60, 92 μm, the width was 5.5 μm; (f) conformal ratios for the cases with different slant angle of the trench: −0.8°, 0°, 2.3°; the depth was 18 μm and the width of the bottom was 3 μm.

of the trench, respectively, as indicated in Figure 3(b). In Figure 3(c), we also defined the slant angle as zero when the side wall of the trench was vertical. When the opening of the trench was wider than the bottom, the slant angle was defined as positive. On the contrary, when the bottom of the trench was wider, the slant angle was negative. Figure 3(d) clearly showed that the conformal ratio decreased as the trench became narrower and the keyhole formed when the width of the trench was 6.5 μm for the given depth of 40 μm. The SEM photos of the typical samples were shown as insets. Figure 3(e) illustrated that conformal ratio decreased as the trench depth increased, and a keyhole appeared at trench depth greater than 18 μm for the given width of 5.5 μm. Figure 3(f) also showed that the keyhole became smaller when the trench opening got wider for the given width of 3 μm and the given depth of 18 μm. From the SEM photos shown in the Figure 3(f), keyhole-free trench filling of parylene deposition was achieved when the slant angle was 2.3°.

Generally, the trench formed by the DRIE had a negative or close to 0° slant angle. To tune the slant angle of the trench to a positive value, an isotropic RIE (reactive ion etching) after the DRIE was applied. A "V"-shaped trench with a wide opening was successfully obtained, as shown in the inset of Figure 3(f). Besides, a multiple etching-filling process was able to improve the filling performance and realize a keyhole-free trench, as reported in our previous publication [21]. Figures 4(a) and (b) showed the profile SEM images of the parylene-filled trenches which were filled with a one-step deposition in Figure 4(a) while the trenches in Figure 4(b) were etched to expose the opening of the trenches and refilled with parylene after the first deposition. It was clear that the hole after the multiple etching-filling process was smaller than before. Comparing the inserted images which gave a magnified view of the trench opening, we could confirm that the closed point of the trench at the opening moved downwards from the surface after the second deposition, which improved the mechanical connecting strength of the structure. Figure 4(c) showed the surface of the parylene-filled trenches, which was flat enough to



(a) (b) (c)

Figure 4 (Color online) SEM images. (a) Profile of one-step-filled trenches, the inserted one is a magnified view of the trench opening; (b) profile of the trenches after a filling-etching-refilling process, the inserted one is a magnified view of the trench opening; (c) surface of the parylene-filled trenches.

Table 2 Geometrical parameters of different parylene-filled trenches and the thermal isolation efficiency

	Width of the trench (μm)	Depth of the trench (μm)	Width between two units (μm)	Thermal isolation efficiency (%)
Control	–	–	–	3
Sample 1	2	100	150	69.7
Sample 2	4	100	150	70.8
Sample 3	7	50	100	72.5

complete the following fabrication.

The thermal isolation performance of the parylene-filled trenches was studied by measuring the temperature variation of two adjacent units, i.e., units 1 and 2 as shown in Figure 5(a), with unit 1 being heated. The isolation efficiency was defined as follows [18]:

$$\alpha = 1 - (\Delta T_2)/(\Delta T_1),$$

where ΔT_1 and ΔT_2 were the temperature rises of units 1 and 2, respectively, when unit 1 was heated with power P. α should be near 100% if the thermal connection was totally isolated, while it would be close to zero if there was a direct contact. We have tested the thermal isolation performance of three different parylene-filled trenches with a control group which was fabricated without parylene-filled trenches between the silicon units. Table 2 showed the geometrical parameters of different parylene-filled trenches and the thermal isolation efficiency. Compared with the control group, the samples with parylene-filled trenches showed excellent thermal isolation efficiency, which is more than 20 times of the efficiency in the control group. Sample 2, which had a larger trench width than sample 1 with other parameters remaining unchanged, showed a better thermal isolation performance. The highest thermal isolation efficiency was achieved to be 72.5% in sample 3 with the 10 paralleled, 7 μm wide and 50 μm deep parylene-filled trenches. Figure 5(d) illustrated the stable temperatures of units 1 and 2 when different heating powers were applied on unit 1 in sample 3.

Besides the thermal isolation performance, the electrical isolation performance of the parylene-filled trenches was also tested. As shown in Figure 5(b), the silicon at the back was exposed by removing the covered parylene film and the I-V relationship of the trench was measured. Meanwhile we tested the electrical isolation performances of air, PMMA (polymethyl methacrylate) (3 mm thick) and glass (500 μm thick) as controls. Figure 5(e) showed that when the voltage rose from 0 to 100 V, the leaking current of the 10 paralleled, 5 μm wide and 100 μm deep parylene-filled trenches increased to approximately 2 pA, while for the glass substrate with the same distance, the leaking current was approximately 140 pA, which indicated the present parylene-filled trench had an excellent electrical isolation character.

The mechanical connection performance of the 10 paralleled, 5 μm wide and 100 μm deep parylene-filled trenches was tested as shown in Figure 5(c). A force was applied on the unit and its displacement was measured by a nano indenter (Nano Indenter G200, Agilent, USA). When the force rose to 1.57 N,

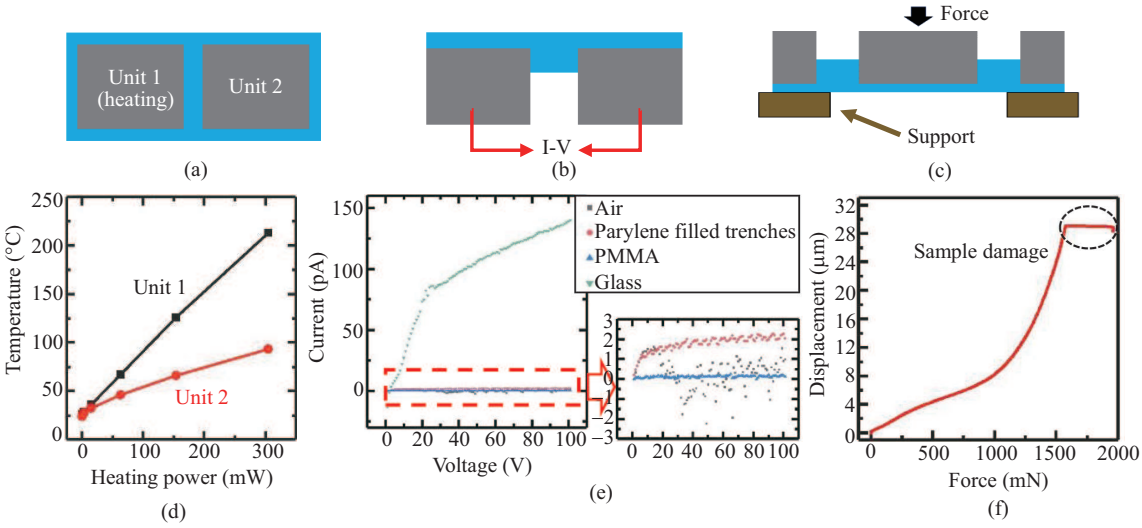


Figure 5 (Color online) Performances of thermal isolation, electrical isolation and mechanical connection of the parylene-filled trenches. (a) Schematic of the thermal isolation test; (b) schematic of the electrical isolation test; (c) schematic of the mechanical connection test; (d) the temperature variation of units 1 and 2 when unit 1 was heated; (e) I-V relationship of air, parylene-filled trenches, PMMA and glass, inset showed the details of the former three samples; (f) displacement of the unit when force was applied.

the displacement reached its maximum value 28.5 μm, as shown in Figure 5(f), and the structure was destroyed when the force was increased. Based on the measurement, the maximum pressure which the parylene-filled trench could work was approximately 200 kPa, which was high enough for most flexible electronics applications. As a comparison, the break-up pressure for the same silicon structure was only 50 kPa.

The simulation results shown in Figure 6 illustrate the mechanics and deformation of the flexible array based on the parylene-MEMS technique. Figure 6(a) demonstrates the displacement (the first row) and the local stress (the second row) of the bending array before (the left column) and after (the right column) the removal of silicon inside the parylene-filled trenches on condition that the parylene reaches a volume deformation of 3%. The FEA results show that the largest displacement of the array without remnant silicon is 1.7 times larger than that before etching, indicating improved flexibility after removing the silicon inside the trenches. The local stress of the silicon array without remnant silicon in trenches only reaches a maximum value of 237 MPa as shown in the lower right of Figure 6(a). Besides, the maximum volume deformation of the chip is only 0.096%, indicating that the deformation of the array can barely result in the deformation of the silicon functional unit, whereby a high performance can be guaranteed. The influence of trench width on the flexibility of the array is shown in Figure 6(b). As expected, the displacement of the array increases with the increase of the trench width in both bending directions. In order to represent the curving degree of the array more intuitively, the radius of the array is estimated, as shown in Figure 6(c). The results show that the radius of the curvature array decreases as the trench width increases, indicating higher degree of bending. By comparing the two curves in both Figures 6(b) and (c), it is observed that the bending directions have little influence on the curving degree of the whole array on condition that the parylene reaches a volume deformation of 3%. As a result, in the actual processing, the required flexible performance can be achieved by the specific design of parylene-filled trench width.

The flexibility of the prepared flexible temperature controlling array with the 10 paralleled, 7 μm wide and 50 μm deep parylene-filled trenches was shown in Figure 7. It is clear that the device had good bendability when bending toward the front side, i.e., the temperature unit faced inwards, while the bending was limited if the bend happened to the back side due to the constraint between chip size and trench width. The device could be easily rolled on to a cylinder with a diameter of 5 mm, as shown in Figure 7(c).

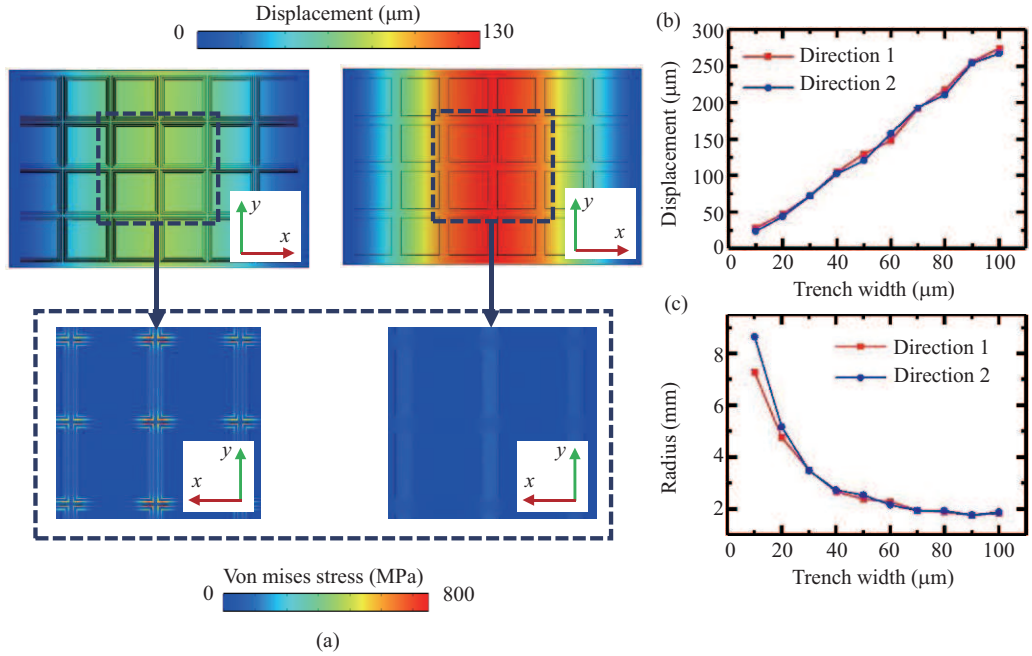


Figure 6 (Color online) Simulation results. (a) Strains and displacements of the deformation model before and after the removal of the remnant silicon; (b) the influence of trench width on the displacement of array; (c) the influence of trench width on the approximate radius of array.

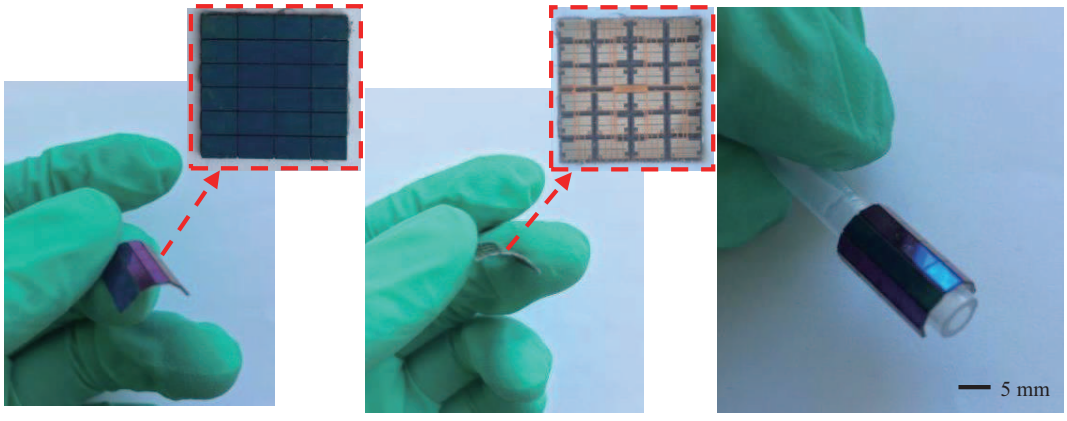


Figure 7 (Color online) Photos of the flexible temperature controlling array. (a) Bending to the front side; (b) bending to the back side; (c) rolling the flexible array on a cylinder with a diameter of 5 mm.

5 Conclusion

In this work, a flexible 4×6 temperature controlling array is successfully fabricated as a preliminary demonstration of the parylene-MEMS technique-based flexible electronics. After process optimization, high-aspect-ratio trenches are filled by parylene with small keyholes and a flat top surface for the following micro/nanofabrication and reliable flexible electronics applications. The experimental results show that the highest thermal isolation efficiency is approximately 72.5% in the sample with the 10 paralleled, 7 μm wide and 50 μm deep parylene-filled trenches. The electrical isolation performance and mechanical connection performance are excellent in the test of the 10 paralleled, 5 μm wide and 100 μm deep parylene-filled trenches whose leakage current is approximately 2 pA while affording a 200 kPa pressure load before rupture. The prepared 4×6 temperature controlling array shows good bendability, which can be applied on a curved surface for digital temperature control or other applications.

The present technique shows a promising potential in manufacturing high-end flexible electronics. Due to the excellent compatibility of the parylene-MEMS technique, more functional structures and units, even IC (integrated circuit), can be prepared and integrated into a single device with the help of the parylene-filled trenches as the flexible hinge. Although the present device only shows a capability of bending operations, with the help of the kirigami technique [22], a stretchable device can be achieved, which will further expand the application fields of the present technique.

Acknowledgements This work was financially supported by National Natural Science Foundation of China (Grant No. U1613215), Beijing Natural Science Foundation (Grant No. L172005), and National Basic Research Program of China (973) (Grant No. 2015CB352100).

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