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Special Focus on Flexible Electronics Technology

A stretchable flexible electronic platform for mechanical and electrical collaborative design

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Abstract With the extensive application of stretchable flexible electronic circuits to wearable equipment and biomedicine, research on the electrical properties of such circuits has become a hot topic. In this paper, a flexible electronic design platform is established for the first time, realizing co-simulation of the mechanical and electronic aspects. The main functions of this platform include the design of stretchable interconnects, flexible devices, stretchable flexible electronic circuits, and stretchable flexible circuit-layout wiring. The following conclusions can be obtained: (1) With increased applied strain, the inductance of a stretchable interconnect will increase, while the delay and crosstalk will become non-negligible. (2) Although the performance of flexible passive devices does not change after transfer printing, the gate capacitor of the flexible MOS at the cut-off area does decrease. (3) Taking a flexible comparator as an example, the function and electrical performance of a flexible circuit are verified. (4) Taking a flexible amplifier circuit as an example, the flexible interconnection layout and wiring are simulated and verified.

Keywords flexible electronic design platform, stretchable interconnect, flexible device, stretchable flexible electronic circuit, stretchable flexible circuit layout wiring

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1 Introduction

A conventional electronic product is rigid and non-malleable, restricting its ductility and flexibility to a certain degree. Stretchable flexible electronics have been heavily studied in recent years due to their deformability in bending, twisting, and stretching. This unique deformability allows such systems to be widely used in wearable devices [1, 2], medical devices [3], energy collection [4], sensing [5], and other fields. In addition, some achievements have been made in areas such as artificial skin [6, 7], artificial retinas [8, 9], nerve probes [10, 11], imaging arrays [12], and solar cells [13, 14].

Inorganic semiconductor materials are applied to stretchable flexible electronic technology. The biggest challenge facing inorganic semiconductors is that of brittle fracture in the process of stretching and bending. Thus, flexible inorganic electronics are mainly manufactured by transferring the electronic components onto a flexible substrate. Using silicon-based electronic technology, a flexible circuit can be obtained by a clever transfer process [15]; however, due to the special requirements of transfer processes, design costs are high, production cycles are long, and test methods are complex, discouraging many flexible-electronic-design engineers. Therefore, to realize such design by reducing design cost and saving time, an accurate flexible-electronic computer-simulation environment should be built.

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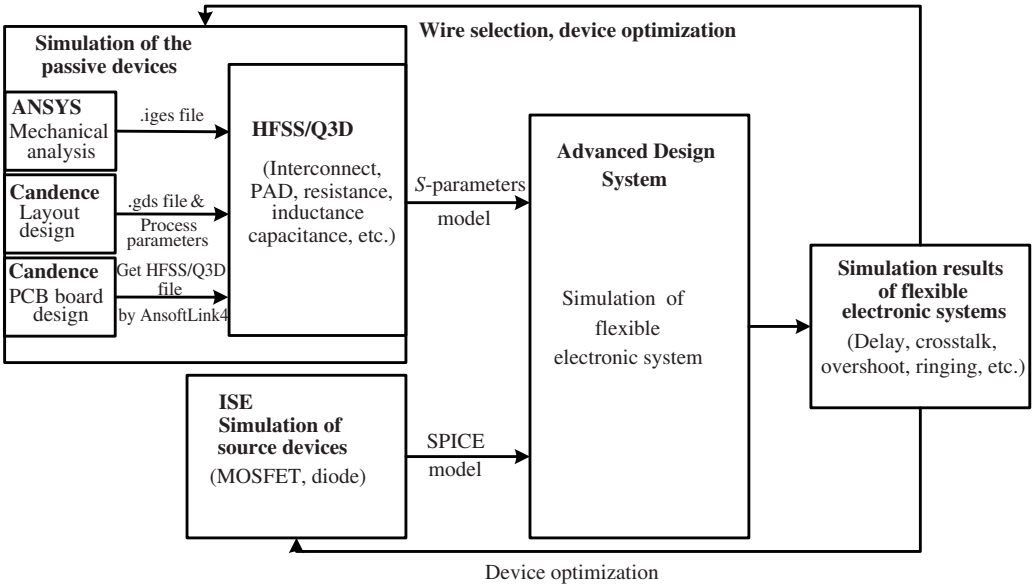

Figure 1 Stretchable-interconnect research.

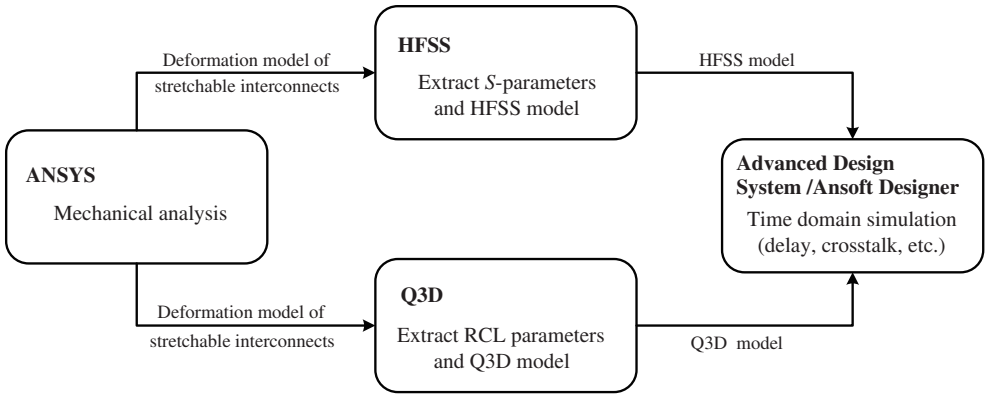

Figure 2 Stretchable-interconnect-simulation flow.

The design of flexible electronic system cannot be separated from the corresponding electronic system design platform. As shown in Figure 1, a flexible electronic design platform is presented in the paper, as shown in Figure 1. Unlike traditional electronic-system design, the flexible-electronic design platform should co-simulate both mechanical and electronic aspects to enable the design of stretchable interconnects, flexible devices, stretchable flexible electronic circuits, and stretchable flexible circuit-layout wiring.

2 Stretchable-interconnect research

Research on stretchable interconnects is a critical scientific issue in flexible-inorganic-electronics research. Stretchable interconnects are crucial objects that can ensure the deformation of flexible circuits. In addition, the signal integrity of electronic systems would be significantly affected by deformation of stretchable interconnects. However, little study has been done on the electrical properties of such interconnects. Therefore, it is very important to obtain the electronic performance of the stretchable interconnects and to establish an electromechanical model; this is a necessary prerequisite for optimizing the performance of the flexible electronic system and optimizing the wiring and routing. The specific simulation flow of a stretchable interconnect in the proposed flexible electronic-design platform is shown in Figure 2.

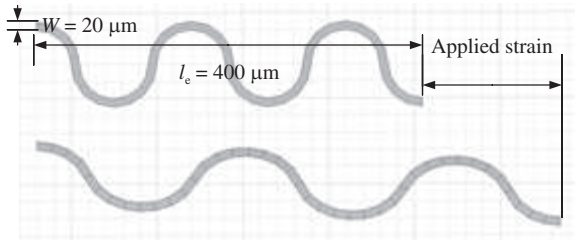

Figure 3 Single stretchable interconnect.

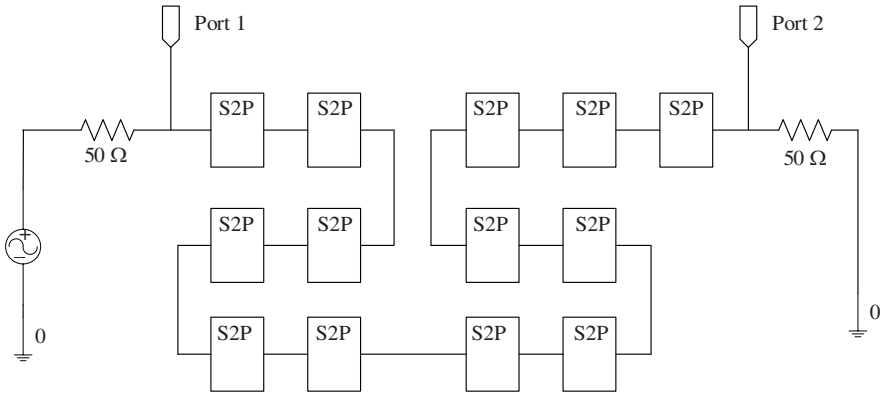

Figure 4 Multiple-stretchable-interconnect series circuit.

2.1 Single stretchable interconnect

The properties of stretchable interconnects are usually characterized as mechanical or electrical. At present, more research has been done on the mechanical properties; the authors have done much work on the electronic performance of a single stretchable interconnect. In [16], the single interconnect's parasitic parameter and electronic performance in the frequency domain were discussed; however, the results of time-domain analysis are more vivid and intuitive [17]. In the paper, we mainly discussed its electronic performance in the time domain.

In the frequency domain, the impedance of the interconnect is known to increase with frequency, thus worsening its transmission performance. To obtain the electronic performance of the stretchable interconnect, a circuit with multiple stretchable interconnects in series is built using Ansoft Designer software. The selected stretchable interconnect is shown in Figure 3. A 400-μm-long and 20-μm-wide stretchable interconnect is selected in the paper; this interconnect consists of a copper metal layer (Cu) sandwiched between two polyimide layers (PI). The thicknesses of each layer from top to bottom are 2, 5, and 2 μm, respectively. The multiple-stretchable-interconnect series circuit is shown in Figure 4. The S2P module is the S-parameters model of interconnect with a 20-μm width W. Moreover, the drive-impedance capability is low, so the ports of the circuit need be connected in series with 50 Ω. The input signal is a sine wave with an amplitude of 1 V.

Delay-simulation results are shown in Figure 5. At 10 MHz, the voltage peak in Port 1 is 0.518 V and the output voltage in Port 2 is 0.49 V. Therefore, the amplitude of the signal barely changes in the transmission process. In addition, the phase does not change substantially. However, at 10 GHz, the voltage peak of Port 1 is 0.851 V and the output voltage of Port 2 is 0.353 V. The amplitude is reduced by 58.5%. In addition, comparing the signals of Ports 1 and 2, delay is up to 0.05 ns, which accounts for 25% of the cycle. With increasing frequency, the amplitude of the output signal is reduced notably and serious delay can be detected.

The delay is described by

$$\tau = \Sigma RC. \tag{1}$$

When the signal frequency is small, that is, when the signal period is relatively large, the delay caused by

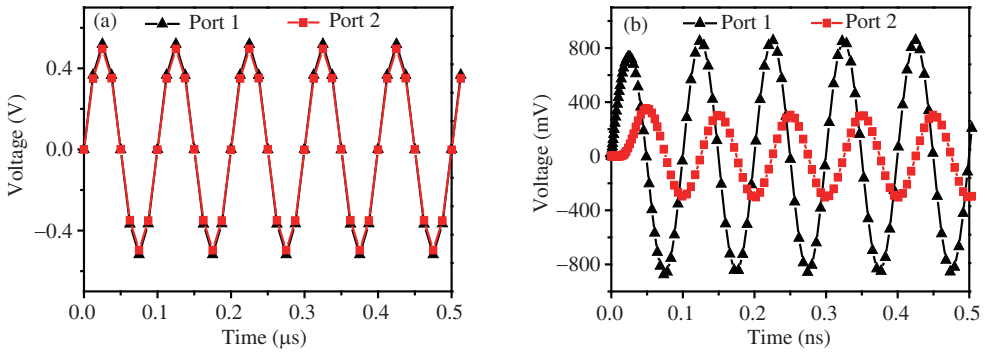

Figure 5 (Color online) Delay simulation results. (a) $f = 10$ MHz; (b) $f = 10$ GHz.

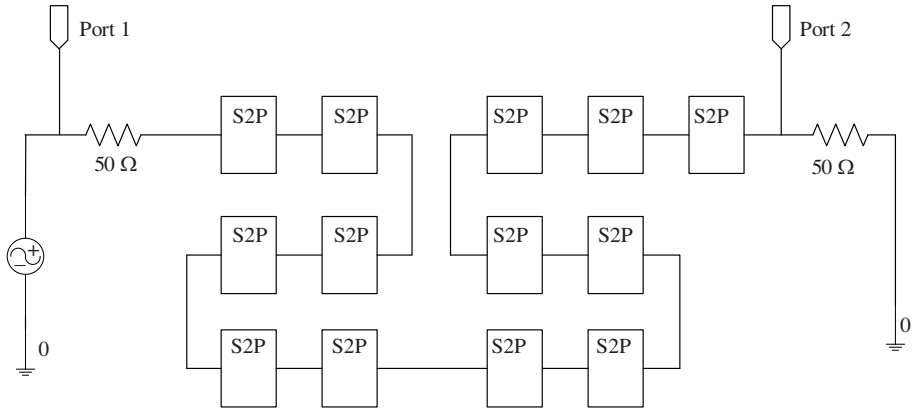

Figure 6 Multiple-stretchable-interconnect series circuit.

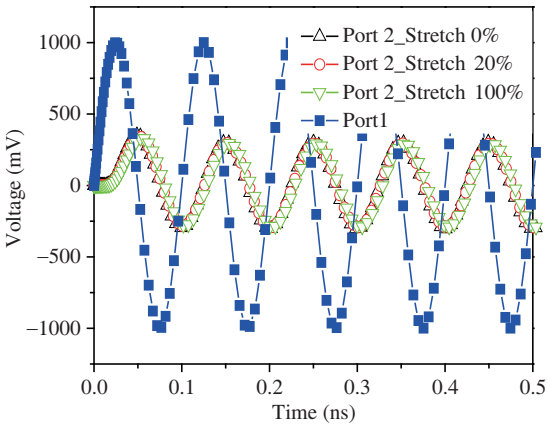

Figure 7 (Color online) The delays of the multiple-stretchable-interconnect series circuit with various applied strains at 10 GHz.

stretching the interconnect has a negligible influence on the signal; however, when the signal frequency is large, that is, the signal period is relatively small, the impact caused by the delay on the signal can be clearly seen. This should be taken into consideration in the stretchable design.

In the time domain, the multiple-stretchable-interconnect series circuit is illustrated in Figure 6. The S2P module is the S parametric model of the stretchable interconnect, where the modules are 0%, 20%, and 100% stretchable interconnects, respectively. The input signal is a sine wave with an amplitude of 1 V and a frequency of 10 GHz.

At 10 GHz, the delays of a multiple-stretchable-interconnect series circuit under various applied strains are shown in Figure 7. Because the impedance of the interconnect increases with applied strain, the transmission performance of the stretchable interconnect worsens. Applied strains from 0% to 100% are

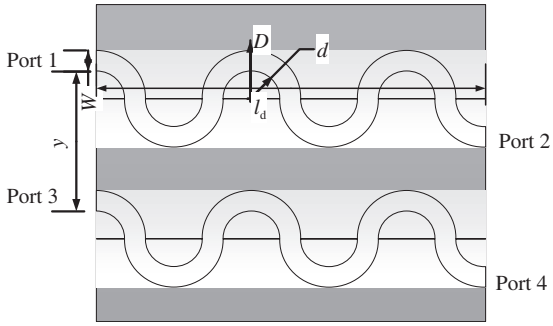

Figure 8 Coupled-stretchable-interconnect structure and port-definition diagram.

considered and the output-signal amplitude in Port 2 decreases by 33.27 mV at 10 GHz. The phase shift increases and a greater delay occurs. Therefore, this phenomenon illustrates that the impedance of a stretchable interconnect increases and the transmission performance worsens with increasing applied strain.

2.2 Coupled stretchable interconnects

In stretchable, flexible electronic circuits, devices should be connected by numerous stretchable interconnects. When coupled stretchable interconnects are close to one another, noise is generated in the adjacent interconnect. This phenomenon is called crosstalk. In a large and complex stretchable electronic-circuit system, crosstalk voltage will be generated in each interconnect from the adjacent and even superimposed in high-density circuits [18]. Crosstalk seriously affects the performance of the stretchable electronic system. The crosstalk between coupled stretchable interconnects is explored in the present paper.

(1) Coupled-stretchable-interconnects structure. The coupled-stretchable-interconnect structure and port-definition diagram are illustrated in Figure 8. Here, D is the outer radius of the stretchable interconnect, d is the inner radius of the wire, l_d is the effective length of the wire, and W is its width. 0%, 40%, and 100% strains are applied to coupled stretchable interconnects.

(2) Frequency-domain performance of coupled stretchable interconnects. Coupled stretchable interconnects can be seen as a two-port network. The S-parameters describing the crosstalk between coupled stretchable interconnects can be subdivided into two general categories, namely near-end crosstalk (S_{31}, S_{13}, S_{24}, S_{42}) and far-end crosstalk (S_{41}, S_{14}, S_{23}, S_{32}). Since the coupled interconnects are symmetric structures in this paper, we have $S_{31} = S_{13} = S_{24} = S_{42}$ and $S_{41} = S_{14} = S_{23} = S_{32}$. Thus, the S_{31} and S_{41} parameters need to be studied.

In the frequency domain, the S_{31} parameter represents the ratio between the transmitted signal and the near-end-crosstalk signal [16]. Eq. (2) presents the near-port crosstalk.

$$S_{31} = 20 \lg \frac{P_3}{P_1}, \tag{2}$$

where P_3 is the power measured from Port 3 and P_1 is that measured from Port 1.

The near-end crosstalk between coupled stretchable interconnects is shown in Figure 9(a). Since crosstalk between interconnects is consists of capacitive and inductive crosstalk, changes in impedance can cause crosstalk variations between interconnects.

When the applied strain is constant, the impedance between coupled interconnects increases with increasing frequency, and the influence of Port 3 on Port 1 grows, i.e., S_{31} becomes larger when P_3 becomes larger. Moreover, as the frequency ranges from 0 to 10 GHz, S_{31} will increase from -106.89 to -29.9 dB in a stretchable interconnect wit 100 % applied strain, increasing by 76.99 dB.

When the frequency is constant, the impedance between the coupled interconnections increases with increasing applied strain, and the influence from Port 1 to Port 3 becomes stronger, that is, S_{31} becomes larger when the P_3 becomes larger. As shown in Figure 9, as applied strain increases from 0% to 100%,

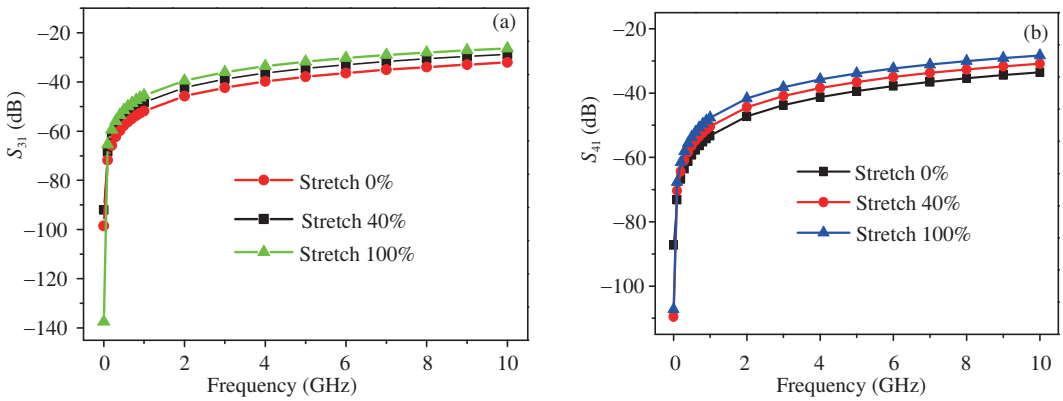

Figure 9 (Color online) (a) Near-end crosstalk; (b) far-end crosstalk.

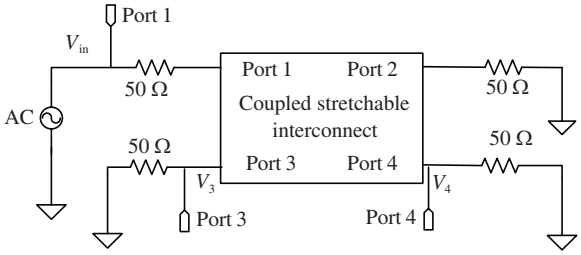

Figure 10 Simulation circuit of coupled stretchable interconnects.

S_{31} increases from −28.8 to −26.4 dB at 10 GHz, increasing by 4.2 dB, and the crosstalk between the coupled interconnects will decrease.

In the frequency domain, S_{41} is the far-end crosstalk, which represents the ratio of the transmitted signal to the far-end crosstalk signal [18]. This term is given by

$$S_{41} = 20 \lg \frac{P_4}{P_1} \tag{3}$$

where P_1 is the power measured from Port 1 and P_4 is the power measured from Port 4.

The simulated far-end-crosstalk results of coupled stretchable interconnects are shown in Figure 9(b). The impendence between the coupled interconnects increases with increasing frequency and the influence of Port 1 on Port 4 grows stronger, meaning that S_{41} becomes larger with the increase of P_4.

When the amount of stretching is constant, the impedance of the coupled interconnects increases with increasing frequency, and the influence of the signal in Port 1 upon that in Port 4 becomes stronger, i.e., S_{41} becomes larger with increasing P_4. Moreover, as the frequency ranges from 0 to 10 GHz, S_{41} will increase from −107.3 to −28.3 dB in the stretchable interconnect with 100% applied strain, increasing by 76.99 dB.

When the frequency is constant, the impedance between the coupled interconnects increases along with applied strain, and the influence of the signal in Port 1 on that in Port 4 becomes stronger, that is, S_{41} becomes larger when P_4 becomes larger. As shown in Figure 10, the applied strain increases from 0% to 100%. S_{41} varies from −33.5 to −28.3 dB at 10 GHz, increasing by 4.2 dB.

(3) Time-domain performance of coupled stretchable interconnects. A simulation circuit of coupled stretchable interconnects is shown in Figure 10. These interconnects can be seen as two-port networks. In addition, since the impendent of coupled stretchable interconnects is too low, a proper resistance is selected for impedance matching. A series resistance of 50 Ω is used in this study.

The crosstalk between coupled stretchable interconnects at a frequency of 10 MHz is shown in Figure 11(a). At 10 MHz, the maximum amplitude of the near-end crosstalk voltage measured at Port 3 is only 192 μV. The maximum amplitude of the far-end crosstalk voltage measured at Port 4 is only 151 μV. Crosstalk noise is very small. However, as shown in Figure 11(b), at 10 GHz, the maximum

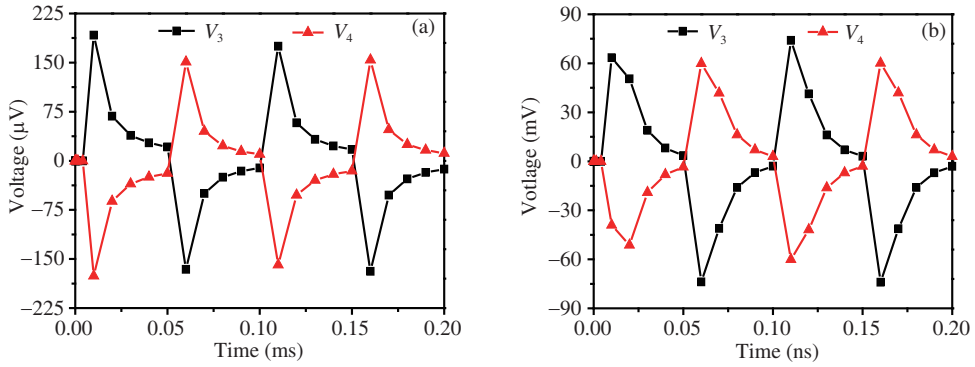

Figure 11 (Color online) Crosstalk of coupled stretchable interconnects at different frequencies. (a) f = 10 MHz; (b) f = 10 GHz.

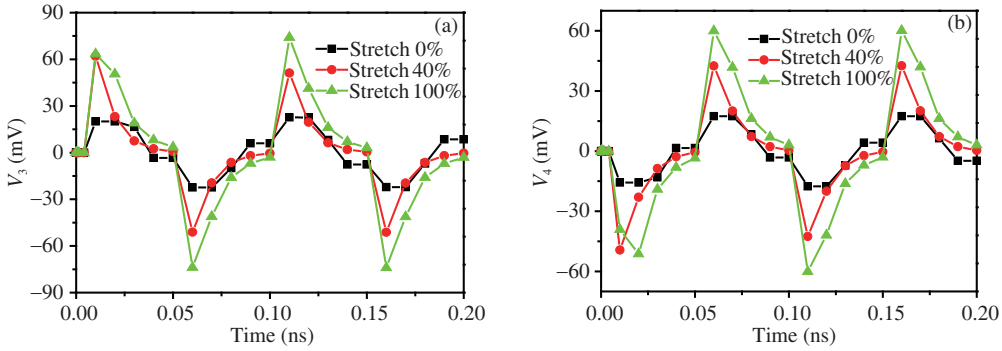

Figure 12 (Color online) Crosstalk of coupled stretchable interconnects with different applied strains. (a) Near-end crosstalk; (b) far-end crosstalk.

amplitude of the near-end crosstalk voltage measured at Port 3 is 74 mV; that of the far-end crosstalk voltage measured at Port 4 is 59 mV. Crosstalk becomes more significant with increasing frequency. In Figure 12, the results indicate that V_3 is slightly larger than V_4. Since the length of the selected wire is shorter, crosstalk at Port 3 is greater than that at Port 4.

The crosstalk between coupled stretchable interconnects with different applied strains is shown in Figure 12. At 10 GHz, obvious crosstalk occurs at Ports 3 and 4. When the applied strain ranges from 0% to 100%, the maximum amplitude of the near-end crosstalk voltage measured at Port 3 increases from 22.7 to 74 mV, and the maximum amplitude of far-end crosstalk voltage measured at Port 4 increases from 17.4 to 59.9 mV. Therefore, at 10 GHz, the signal at Port 1 has significant effects on those at Ports 3 and 4, and crosstalk between interconnects becomes more obvious as the applied strain grows larger.

In short, at high frequencies, as the extension of the stretchable interconnect changes, both delay and crosstalk obviously occur. These cannot be ignored in flexible-circuit design.

3 Flexible-devices research

Flexible devices play an important role in flexible circuits. It is essential that such devices present normal performance in flexible circuits under different deformations. To explore the performances of flexible devices, we here divide them into passive and active. For flexible passive devices, flexible resistance and capacitance were analyzed. For flexible active devices, we took metal-oxide-semiconductor field-effect transistors (MOSFETs) as an example.

3.1 Flexible passive devices

There has been little study of the electrical properties of flexible passive devices in flexible electronic circuits. In the proposed flexible electronic design platform, the performance of such devices can be

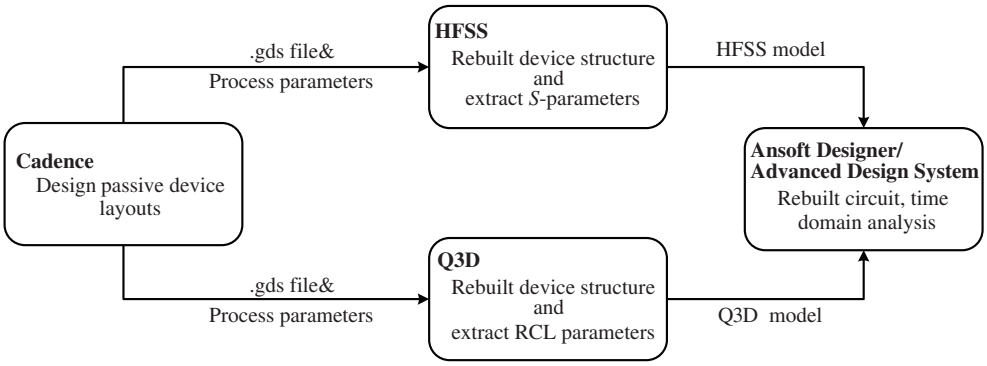

Figure 13 Flexible-passive-device simulation flow.

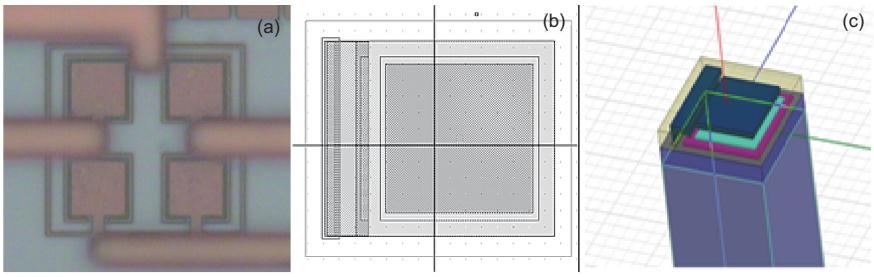

Figure 14 (Color online) Flexible capacitor: (a) capacitor electronic photograph; (b) two-dimensional layer in Cadence; (c) capacitor-reconstruction structure in ANSYS Q3D Extractor.

Table 1 The key capacitor-structure parameters

Device	Effective length (μm)	Effective width (μm)	Effective thickness (μm)	Effective spacing (μm)	Thickness (mm)
10 μm × 10 μm	10	10	0.048	0.048	1
20 μm × 20 μm	20	20	0.048	0.048	1
30 μm × 30 μm	30	30	0.048	0.048	1

obtained.

The simulation flow of a flexible passive device is shown in Figure 13. First, the flexible-passive-device structure can be established using existing multi-physical-field analysis software. Secondly, the various mechanical properties can be extracted. Finally, we can analyze the influence of the signal frequency upon flexible passive devices.

Capacitors are indispensable components of integrated-circuit systems and are widely used in DC, bypass-decoupling, filtering, coupling, tuning, and rectification circuits [19]. A real Capmip capacitor from the Huahong NEC CD350G-60V80V process library is shown in Figure 14(a). In addition, Figure 14(b) shows the layout of the capacitors in Cadence. In this paper, capacitors with areas of 10 μm × 10 μm, 20 μm × 20 μm, and 30 μm × 30 μm were selected. These had capacitance values of 69.2 fF, 274.4 fF, and 615.6 fF, respectively. The three-dimensional structure of flexible capacitance in the ANSYS Q3D Extractor is shown in Figure 14(c). The key structural parameters of flexible capacitor are shown in Table 1.

The simulation results for a flexible capacitor are shown in Table 2. It is clear that the capacitance values are 70.843 fF, 283.361 fF, and 627.573 fF, respectively. The flexible capacitance values do not change much compared with the capmip in Huahong NEC CD350G-60V80V. Eq. (4) presents the capacitance:

$$C = \frac{\varepsilon S}{d}, \tag{4}$$

where ε is the relative permittivity, S is the plate area, and d is the spacing between plates. It is clear that capacitance is mainly governed by the device structure and dielectric material. The integrated

Table 2 Flexible-capacitor-simulation results

Device specification	Huahong NEC CD350G-60V80V capmip (fF)	Capacitance in the paper (fF)
10 μm × 10 μm	69.2	70.843
20 μm × 20 μm	274.4	283.361
30 μm × 30 μm	615.6	627.573

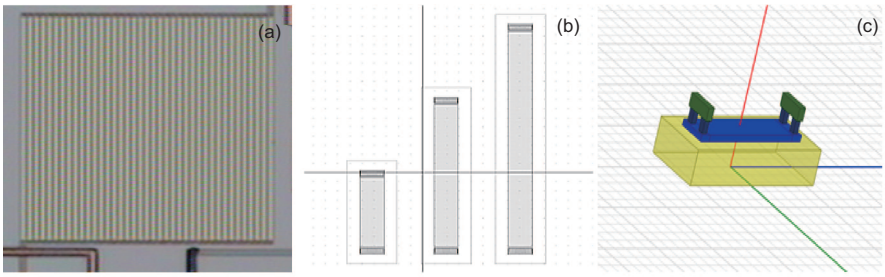

Figure 15 (Color online) Flexible resistance. (a) Resistor electronic photographs; (b) two-dimensional layers in Cadence; (c) resistor reconstruction in the ANSYS Q3D Extractor.

Table 3 Flexible-resistor-simulation results

Device specification (μm)	Huahong NEC CD350G-60V80V rplcd (Ω)	Resistance in the paper (Ω)
$L = 9.2$	41.2371	41.7918
$L = 17.2$	82.4742	83.02892
$L = 25.2$	123.111	124.342

capacitor is made in the surface of the silicon substrate. The capacitor's structure is unaffected by the transfer-printing process; therefore, the capacitance values do not change afterward.

As shown in Figure 15(a), for the real resistor resistor from the Huahong NEC CD350G-60V80V process library, the resistance width is set to 2 μm and the lengths are set to 9.2, 17.2, and 25.2 μm; the corresponding resistance values are 41.2371, 82.4742, and 123.111 Ω, respectively. The layout of the resistor is shown in Figure 15(b). We import the layout file from Cadence into the ANSYS Q3D Extractor and start rebuilding the flexible resistance. Figure 15(c) presents a three-dimensional resistance reconstruction.

From Table 3, at 0 GHz, the simulation results show that the resistance values are 41.7918 Ω, 83.02892 Ω, and 124.342 Ω, respectively. Therefore, the resistance values do not change after transfer printing. Eq. (5) presents the resistance:

$$R = \rho \frac{l}{S}, \tag{5}$$

where ρ is the resistivity of the material, l represents the length of the conductor, and S is the cross-sectional area of the wire. It is clear that resistance is related mainly to the device structure and the material. The structure of the resistor is not affected by the transfer-printing process; therefore, it is clear that the resistance values do not change after transfer printing.

In short, the performance of the passive components after transfer printing has not changed, so they can be directly used in flexible-circuit design.

3.2 Flexible active devices

Flexible active devices are the core of electronic circuits. All oscillations, amplification, adjustment, and demodulation cannot be separated from active devices. In flexible-electronic-circuit systems, the electrical performance of flexible active devices is a hot research topic.

The simulation flow of flexible active devices in the proposed flexible electronic platform is shown in Figure 16. Firstly, based on the characteristics of transfer printing, a flexible active device structure can be determined using the existing semiconductor process and device-simulation software, as well as the

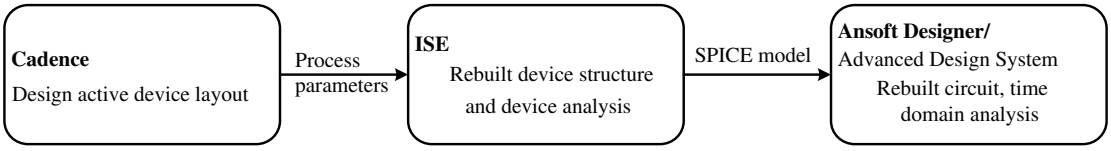

Figure 16 Flexible-active-device-simulation flow.

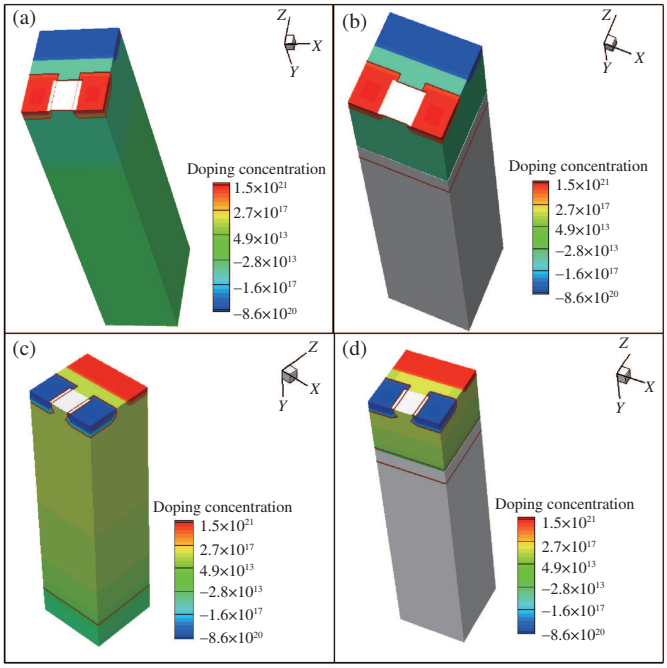

Figure 17 (Color online) NMOSFET device: (a) silicon structure, (b) PDMS substrate. PMOSFET device: (c) silicon structure, (d) PDMS substrate.

size, materials, doping concentration, and other device parameters provided by the foundry. Secondly, we should rebui debives structure and simulate the new flexible active device. Thirdly, the operating frequency, output voltage, threshold voltage, gain, I-V characteristics, and C-V characteristics of flexible active devices with different applied strains are analyzed.

In this paper, the NMOSFET and PMOSFET devices are selected from the Huahong NEC CD350G-60V80V process library; the gate length and gate width of both devices are each 1 μm. According to device-layout-layer information from Cadence, the MOSFET-device structure is established in ISE TCAD. The three-dimensional MOSFET structure constructed in ISE TCAD is shown in Figure 17.

As shown in Figure 18(a), the threshold voltage $V_{\rm th}$, transconductance G_m, and input resistance $R_{\rm on}$ of the device do not change after transfer printing. Since the structure of the MOS is not affected in the transfer-printing process, device-conduction performance is unaffected.

In Figure 18(b), in the cut-off area, the gate capacitance of the MOSFET with PDMS substrate is smaller than that of the MOS with silicon substrate. When the device operates in the linear or saturation areas, the gate capacitance will not change anymore. As shown in Figure 19, the gate capacitance in the cut-off area is a series connection of the channel and substrate capacitances. In addition, the dielectric constant of the substrate becomes smaller after transfer printing, meaning that the substrate capacitance becomes smaller. Therefore, the gate capacitance decreases after transfer printing at the cut-off area. In addition, as the device work in the linear and saturation regions, the gate capacitance presents channel and overlap capacitances, which are only related to the device's surface structure.

$$C_s = \frac{\varepsilon_{rs}\varepsilon_0}{\sqrt{2}L_D}\exp\left(-\frac{qV_s}{2k_0T}\right). \tag{6}$$

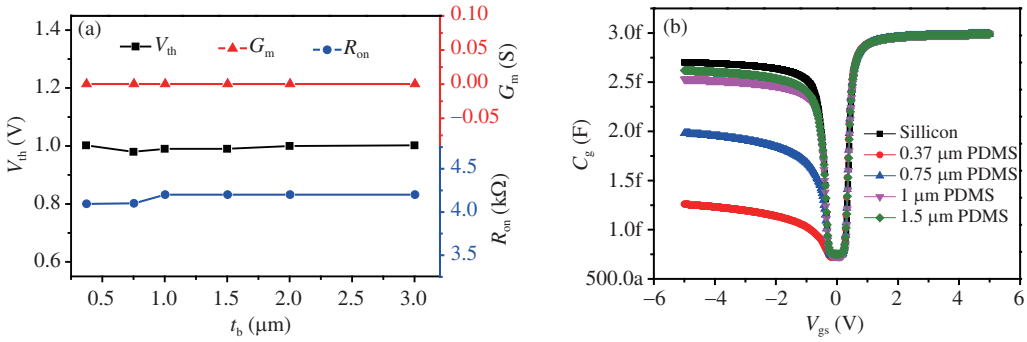

Figure 18 (Color online) (a) The variation of threshold voltage $V_{\rm th}$, transconductance G_m, and on-resistance $R_{\rm on}$ with substrate thickness; (b) the relationship between gate capacitance and gate voltage.

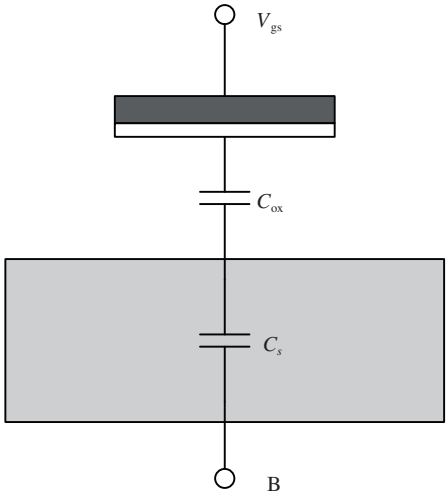

Figure 19 Gate capacitance at the cut-off area.

In short, the performance of active components after transfer printing has not changed in the linear or saturation areas, so active devices can be directly used in flexible-circuit design there. However, in the cut-off area, the changed gate capacitor should be taken into the consideration in flexible-circuit design.

4 Flexible-circuit research

Flexible electronic circuits overcome the brittleness of traditional inorganic electronic products, maintaining excellent electrical properties and ductility. A flexible circuit can be designed in the proposed flexible electronic design platform. Firstly, based on the characteristics of the transfer-process technology, a flexible wire-interconnect model, flexible interconnect layout and routing rules, flexible passive-device model, and flexible active-device model are established. Secondly, the signal integrity of the flexible electronic-circuit system under different deformations is analyzed. At the same time, some signal problems including delay, crosstalk, overshooting, and jitter of flexible-electronic-circuit systems are studied. Finally, by simulating a flexible electronic system, the optimized device, interconnection layout, and wiring are obtained. The simulation process is shown in Figure 20.

The comparator has a high sensitivity. The flexible circuit has a large impact upon the input signal, and the variable input voltage significantly affects the comparator. In this paper, a comparator circuit is designed for verification, for which the circuit diagram is shown in Figure 21(a). The verification circuit built in the Advanced Design System software is shown in Figure 21(b). PMOS and NMOS devices are SPICE models obtained from ISE TCAD and the device size corresponds to the actual situation; W is the outer ring of the device and the aluminum cable; L_1–L_5 is presented as a flexible interconnect.

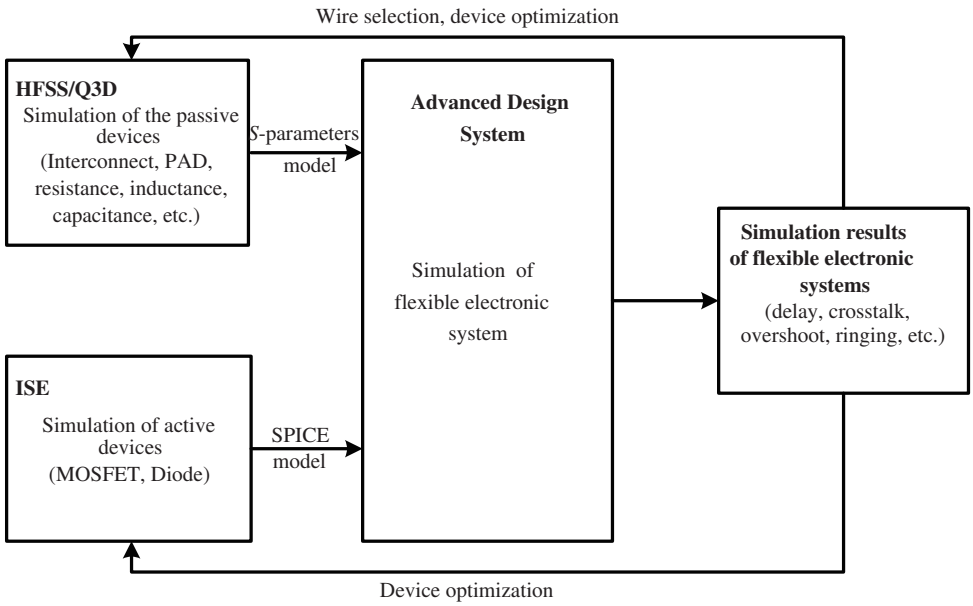

Figure 20 Flexible-electronic-system simulation flow.

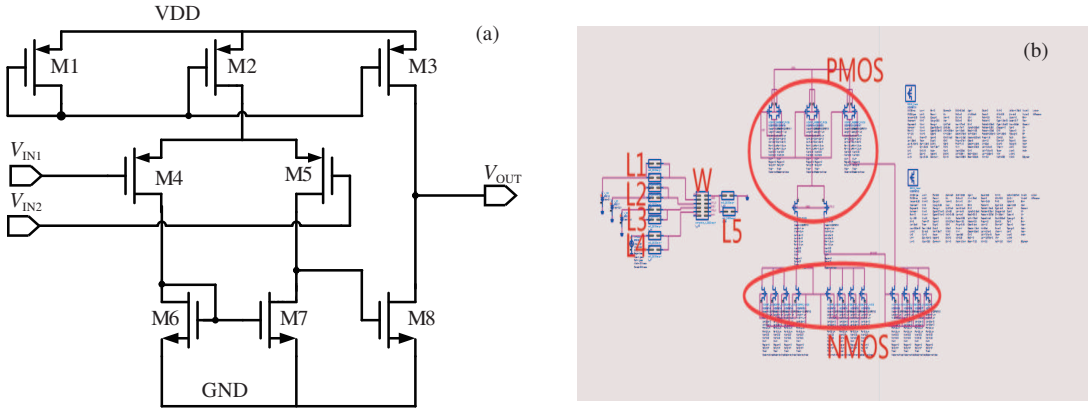

Figure 21 (Color online) (a) Latch-comparator circuit; (b) comparator verification circuit in the advanced design system.

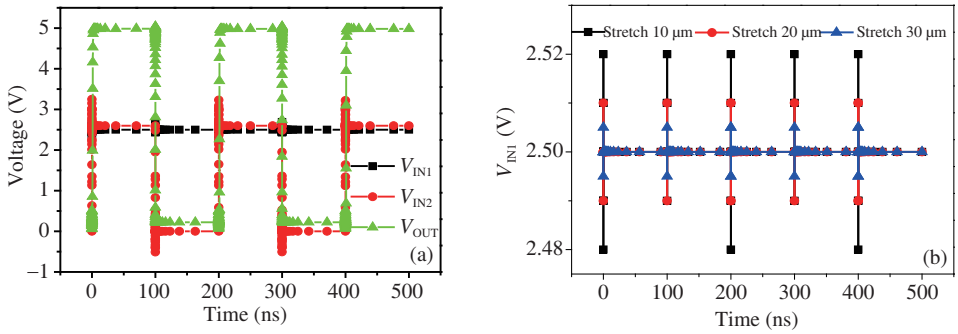

Figure 22 (Color online) (a) Flexible-comparator-simulation results; (b) comparator circuit produces glitches.

Figure 22(a) shows the results of the flexible-comparator simulation. The positive input V_{IN1} is constant at 2.5 V and the negative input V_{IN2} input 2.6 V up and down square wave signal. It is clear that the output V_{OUT} is a 0 to 5 V transition square-wave signal, which may indicate that the comparator can achieve the comparison function. However, the signal passing through module W before and after will produce glitches that are more serious; this phenomenon is shown in Figure 22(b), and can be modified

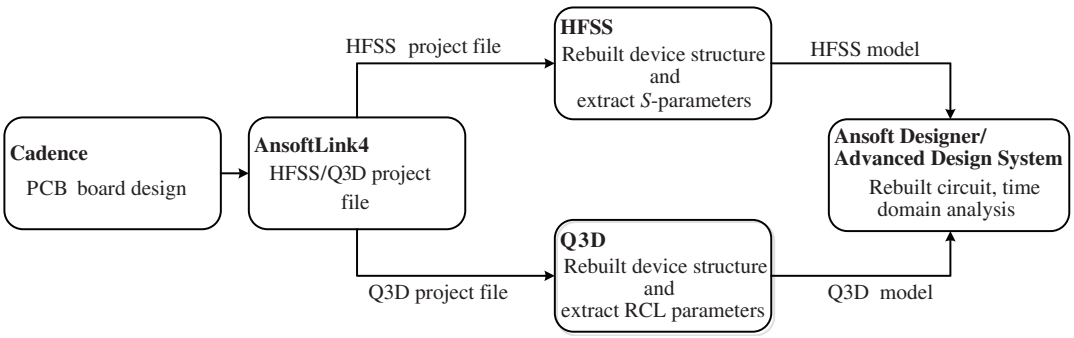

Figure 23 Flexible-circuit-layout-wiring-simulation flow.

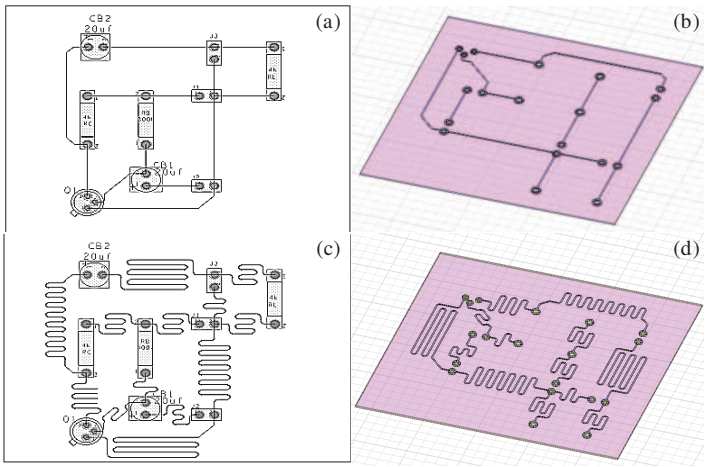

Figure 24 (Color online) The amplifier circuit's layout and wiring: the straight layout wiring diagram (a) in Cadence and (b) in the ANSYS Q3D Extractor; the stretchable-layout-wiring diagram (c) in Cadence and (d) in the ANSYS Q3D Extractor.

by extending the stretchable interconnect to be optimized. This situation must be the subject of further research in future flexible-circuit design.

5 Flexible-circuit-layout-wiring research

In flexible-electronic design, we must first consider the size of the circuit. Second, it is necessary to determine the locations of the special components. Finally, according to the functional unit of the circuit, all components are laid out. Wiring is an important step in completing circuit design. In the wiring process, the reflection interference generated by the parallel input and output trace line should be avoided. The simulation flow of flexible-circuit-layout-wiring is shown in Figure 23.

In the paper, the basic amplifier is chosen as the verification circuit in the proposed flexible-electronic-design platform. The layout of the amplifier circuit in Cadence is shown in Figure 24(a) and (c). The rebuilt layout in the ANSYS Q3D Extractor is shown in Figure 24(b) and (d). Finally, the basic amplifier circuit is built in the advanced design system.

As shown in Figure 25, the simulation analysis is carried out in the Advanced Design System. The input signal is a sine wave with a frequency of 1 MHz and a peak value of 50 mV. The output-voltage amplitudes of the straight wire and the stretchable-flexible-interconnect-amplifier circuit are all 123.5 mV. The amplifier circuit is working properly. The input signal is a sine wave with a frequency of 100 MHz and a peak value of 50 mV. The straight-wire-amplifier circuit work, but its output waveforms are distorted. The main reason for this is that the impedance of stretchable layout wiring cannot be ignored.

As shown in Figure 26, as the applied strain ranges from 0% to 100% the output waveforms of the

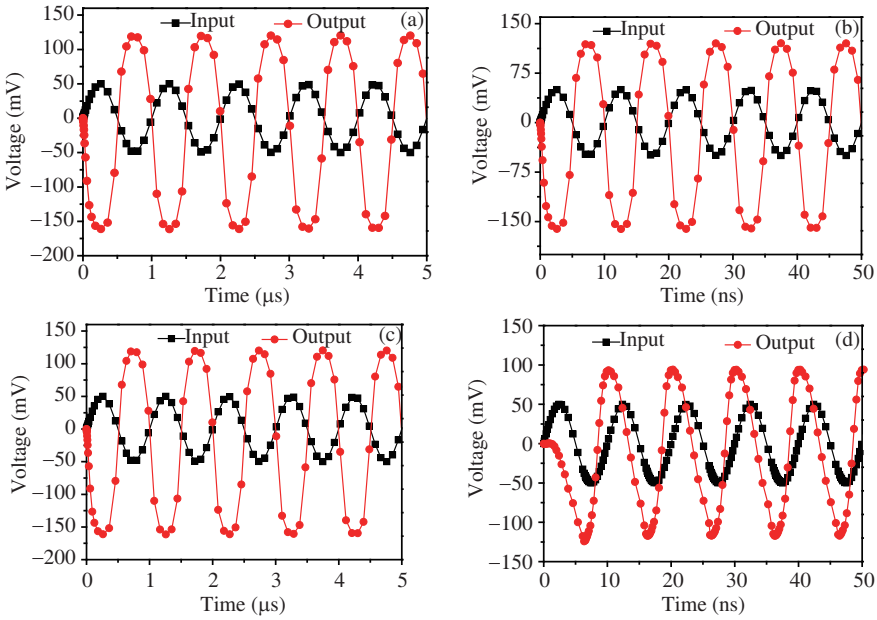

Figure 25 (Color online) Amplifier input and output waveforms (a) at 10 MHz and (b) at 100 MHz for the straight-wire-amplifier circuit; (c) at 10 MHz and (d) at 100 MHz for the stretchable-flexible-interconnect-amplifier circuit.

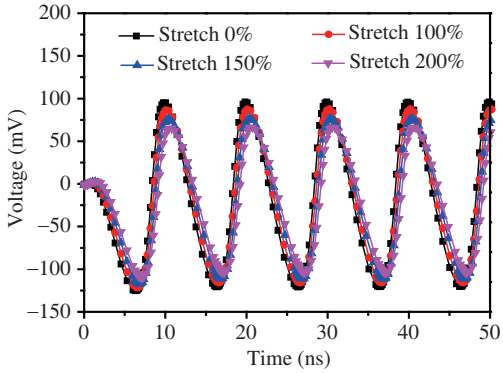

Figure 26 (Color online) Output waveform of the stretchable flexible interconnect amplifier under various applied strains.

stretchable wire-amplifier circuit are distorted. The maximum amplitude of output voltage measured increases from 94 to 64 mV, leading to a certain delay. The main reason for this is that the impedance of stretchable layout wiring becomes large and the transmission performance worsens with increasing applied strain. Therefore, it is very important to establish a set of layout rules for flexible-circuit design.

6 Conclusion

A flexible electronic-design platform is newly presented in this paper. Using this platform, some guiding results can be obtained for the design of a stretchable flexible electronic circuit. At the same time, the following conclusions can be obtained: (1) with increasing applied strain, the inductance of a stretchable interconnect will increase and the delay and crosstalk will become non-negligible; (2) although the performances of flexible passive devices do not change after transfer printing, the gate capacitor of the MOS did decrease in the cut-off area; (3) taking a flexible comparator as an example, the function and electrical performance of a flexible circuit are verified; (4) taking a flexible amplifier circuit as an example, the flexible interconnection layout and wiring are simulated and verified.

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