SCIENCE CHINA
Information Sciences

• LETTER •

December 2017, Vol. 60 129402:1–129402:3
doi: 10.1007/s11432-016-9001-9

Modeling the impact of process and operation variations on the soft error rate of digital circuits

Ruiqiang SONG, Shuming CHEN*, Bin LIANG, Yaqing CHI & Jianjun CHEN

College of Computer, National University of Defense Technology, Changsha 410073*, China*

Received November 21, 2016; accepted January 3, 2017; published online February 24, 2017

Citation Song R Q, Chen S M, Liang B, et al. Modeling the impact of process and operation variations on the soft error rate of digital circuits. Sci China Inf Sci, 2017, 60(12): 129402, doi: 10.1007/s11432-016-9001-9

Dear editor,

Process or operation variations are important factors in the soft error rate (SER) of integrated circuits [1, 2]. During manufacturing or other operations, inevitable process or operation variations lead to changes in the electrical parameters of transistors, which can result in sizeable shifts in the SER of integrated circuits [3]. Some studies have reported that the hardness of test chips can vary by more than 20% as a result of process or operation variations [4]. Therefore, it is vital to account for process and operation variations when evaluating the circuit sensitivity and predicting the SER in advanced CMOS technology.

In previous research, some models for evaluating the circuit sensitivity caused by process or operation variations have been derived. For instance, Mostafa et al. [5] proposed a critical charge model to evaluate the single-event upset (SEU) sensitivity of static random access memorys (SRAMs) and flip-flops. Based on this model, the critical charge was determined by the driving current of the transistors. Process or operation variations affected this driving current, leading to changes in the calculated critical charge. Recently, Monte Carlo simulation approach has been used to evaluate the circuit sensitivity [6]. This approach shifts the device parameters to model process or operation variations. A current source, which is represented as the ion induced transient current, was implemented in the circuit node. The circuit response was simulated by circuit-level simulation tools based on the variational device parameters.

Although these models or approaches have been used to evaluate the circuit sensitivity caused by process or operation variations, they still have some limitations. For instance, the critical charge model is strongly dependent on the circuit topology. Different circuit topologies result in different equations to calculate the critical charge. Moreover, some process parameters, such as mobility, affect the driving current slightly. However, they have a significant effect on the collected charge of sensitive transistors. Although the calculated critical charge does not change, these process parameters also affect the circuit sensitivity and lead to SER variations.

Therefore, we propose a circuit-level simulation approach to evaluate process- or operation-induced SER variations, as shown in Figure 1. Our approach consists of three interacting components. The first component uses a Monte Carlo simulation to determine ion transportation and calculate the ionized charge in the semiconductor. In the second component, circuit-level charge collection models calculate transient currents after ion strikes. In this component, a novel model is used to determine the parameters affected by process or

* Corresponding author (email: smchen@nudt.edu.cn)

The authors declare that they have no conflict of interest.

© Science China Press and Springer-Verlag Berlin Heidelberg 2017

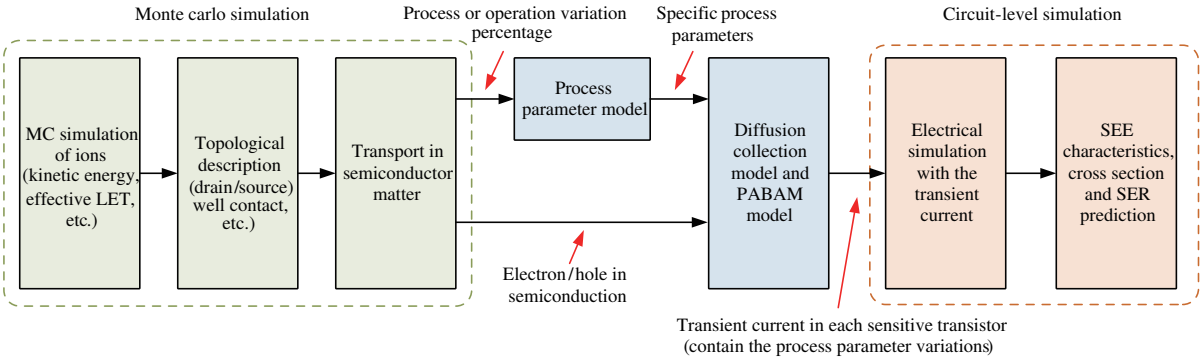

Figure 1 (Color online) Process to implement the proposed simulation approach.

operation variations. Based on the specific process parameters, charge collection models are used to calculate the collected charge and transient current of each sensitive transistor. Finally, the third component evaluates the sensitivity by simulating the circuit response. This enables the circuit sensitivity and SER to be determined.

Unlike conventional approaches, the proposed approach does not use the driving current to take into account process or operation variations. Therefore, it is independent of the circuit topology and can be used to evaluate the SER for many circuit types. Moreover, because the process parameter model consists of a series of look-up tables to define the relationship between process or operation variations and the process parameter values, many parameters can be investigated during SER evaluations. Therefore, the proposed approach overcomes the limitations of existing models or approaches. It is suitable for evaluating process- or operation-induced SER variations.

Determining the process parameter model. In our previous studies, the technology computer aided design (TCAD) simulation tool was employed to investigate the physical mechanism of transistors [7,8]. Therefore, we use the TCAD simulation tool to determine the process parameter model. PMOS and NMOS transistors are represented as TCAD models. These models are first calibrated to match the electrical characteristics of standard compact models. If the electrical characteristics match, the basic process parameters can be determined. Then, TCAD simulations are performed under varying process or operation conditions. Based on the simulation results, the specific parameter values can be obtained and the process parameter model can be determined.

For instance, after calibrating the TCAD model, the peak value of N-well doping is determined. Then, we change the peak value of N-well doping from 80% to 120% and use the TCAD simulation tool to obtain the process parameters. Based on the simulation results, the relationship between the carrier mobility/velocity and the N-well doping variation can be determined in the process parameter model. Similar methods can be used to determine the relationship between the parameters and other process or operation variations. Based on these look-up tables, the process parameter model can conveniently determine the specific parameters with different process or operation conditions.

Simulating circuit responses with specific process parameters. After determining the process parameter model, charge collection models are used to calculate the collected charge and transient current of each sensitive transistor. In our proposed simulation approach, the diffusion collection model [9] and the PABAM model [10] are used to calculate the diffusion current and the parasitic bipolar amplification current. However, unlike the conventional diffusion collection model, process parameters used in this model are not fixed. Instead, they are determined by the process parameter model and they have alterable values if process or operation conditions change. Similarly, the parameter values in the PABAM model are determined by the process parameter model. Therefore, the charge collection models can calculate different results according to process or operation variations. The circuit-level simulation is performed in the last component. Based on the calculated transient current, the circuit response is simulated by the circuit-level tools. The single-event effect (SEE) characteristics, cross section, and SER variation of the circuits are then quantified. Because of the different transient currents, the circuit-level simulation will obtain different SEE characteristics. Therefore, the proposed simulation approach can evaluate changes in the SER under process or operation variations.

Confirming the capability of the proposed simulation approach. We use the proposed approach and TCAD simulation tool to investigate the collected charge of transistors. Variations in the

well doping, gate oxide thickness, threshold voltage doping, transistor size, operation voltage, and temperature are considered. We assume each process or operation condition has approximately ±20% variation. Two simulation results are compared to confirm the capability of the proposed approach.

For instance, variations in the operation voltage significantly affect the collected charge in the TCAD simulation. A higher voltage can increase the collected change of the PMOS transistor by up to 36% and that of the NMOS transitory by up to 32%. Similarly, the collected charge obtained by the proposed simulation approach also varies with the operation voltage. The PMOS and NMOS transistors increase their collected charge by up to 34% and 33%, respectively. Similar simulation results are observed when the other process or operation conditions change.

It is noteworthy that the variation trends obtained by the proposed simulation approach are consistent with the TCAD simulation. For instance, a −20% variation in the gate oxide thickness increases the collected charge of the transistors, whereas the same variation in the operation voltage acts to decrease the collected charge of the transistors in both the TCAD simulation and the proposed approach. The simulation results confirm the capability of the proposed approach. They indicate the proposed approach is able to determine the collected charge variations caused by process or operation variations.

Evaluating SER variations using the proposed simulation approach. The proposed simulation approach was used to evaluate SEU and single-event transient (SET) characteristics caused by process or operation variations. Two test chips were designed and fabricated by the commercial 65 nm CMOS technology. These chips were irradiated by heavy ions. The simulated SEU and SET cross sections are compared with experimental results. They are consistent with experimental results although the process and operation conditions change. Detailed experimental and simulation results are described in the supplementary file. The experimental results also confirm the capability of the proposed simulation approach. The proposed approach is suitable for evaluating the SER of integrated circuits with different process and operation conditions.

Acknowledgements This work was supported by National Natural Science Foundation of China (Grant Nos. 61376109, 61434007). The authors would like to thank the HI-13 team and the HIRFL team for heavy ion experiment support.

Supporting information The supporting information is available online at info.scichina.com and link.springer.com. The supporting materials are published as submitted, without typesetting or editing. The responsibility for scientific accuracy and content remains entirely with the authors.

References

1 Loveless T D, Alles M L, Ball D R, et al. Parametric variability affecting 45 nm SOI SRAM single event upset cross-section. IEEE Trans Nucl Sci, 2010, 57: 3228–3233
2 Kauppila A V, Bhuva B L, Kauppila J S, et al. Impact of process variations on SRAM single event upsets. IEEE Trans Nucl Sci, 2011, 58: 834–839
3 Peng H K, Wen C, Bhadra J. On soft error rate analysis of scaled CMOS designs: a statistical perspective. In: Proceedings of IEEE/ACM International Conference on Computer-Aided Design, San Jose, 2009. 157–163
4 Gasiot G, Castelnovo A, Glorieux M, et al, Process variability effect on soft error rate by characterization of large number of samples. IEEE Trans Nucl Sci, 2012, 59: 2914–2919
5 Mostafa H, Anis M, Elmasry M, et al. A design-oriented soft error rate variation model accounting for both die-to-die and within-die variations in submicrometer CMOS SRAM cells. IEEE Trans Cric Syst, 2010, 57: 1298–1311
6 Kauppila A V, Bhuva B L, Massengill L W, et al. Impact of process variations and charge sharing on the single event upset response of flip-flops. IEEE Trans Nucl Sci, 2011, 58: 2658–2663
7 Liang B, Song R Q. Analyzing and mitigating the internal single-event transient in radiation hardened flip-flops at circuit-level. Sci China Tech Sci, 2014, 57: 1–6
8 Song R Q, Chen S M, He Y B, et al. Flip-flops soft error rate evaluation approach considering internal single-event transient. Sci China Inf Sci, 2015, 58: 062403
9 Artola L, Hubert G, Warren K M, et al. SEU prediction from SET model using multi-node collection in Bulk transistors and SRAMs down to the 65 nm technology node. IEEE Trans Nucl Sci, 2011, 58: 1338–1346
10 Song R Q, Chen S M, Huang P C, et al. PABAM: a physics-based analytical model to estimate bipolar amplification effect induced collected charge at circuit level. IEEE Trans Device Mater Rel, 2015, 15: 595–603