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• **Supplementary File** •

Modeling the impact of process and operation variations on the soft error rate of digital circuits

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Appendix A Confirming the capability of the proposed simulation approach

Appendix A.1 Simulation setup

To confirm the capability of the proposed simulation approach, we use the proposed approach and TCAD simulation tool to investigate the collected charge of transistors. The PMOS and NMOS transistors are represented as TCAD models, as shown in Figure A1. The variations of the well doping, the gate oxide thickness, the threshold voltage doping, the W/L rate, the voltage and the temperature are considered. We assume each process or operation conditions have about ±20% variation. The incident ion location is set to the center of the drain depletion region. The linear energy transfer (LET) is set to 30 MeV·cm^2/mg. The collected charge of PMOS and NMOS transistors is determined by TCAD simulation and the proposed simulation approach. Two simulation results are compared to confirm the capability of the proposed approach.

Physical models used in TCAD simulation included Fermi-Dirac statistics, band-gap narrowing effect, Auger recombination, and doping dependent, electric field dependent, and carrier-carrier scattering mobility models. Unless otherwise specified, the default models and parameters were provided by Sentaurus TCAD vH-2013.03.

Appendix A.2 Simulation results

Figure A2 shows the simulated collected charge of transistors with voltage and gate oxide thickness variations. Simulation results show a significant change when the process or operation conditions change. For TCAD simulation, the variation of the voltage significantly increases the collected charge. The change of PMOS transistor is about 36% and the change of NMOS transistor is about 32%. Similar with TCAD simulation results, the collected charge obtained by the proposed simulation approach also increases with the variation of the operation voltage. The change of PMOS transistor is about 34% and the change of NMOS transistor is about 33%. Similar simulation results are also observed when the other process or operation factors change.

It is noteworthy that the variation trends obtained by the proposed simulation approach are also consistent with TCAD simulation. For instance, the gate oxide thickness with -20% variation increases the collected charge of transistors while the voltage with the same variation decrease the collected charge of transistors in both TCAD results and the proposed approach. Simulation results confirm the capability of the proposed approach. They indicate the proposed approach is able to determine the collected charge variations caused by process or operation variations.

Appendix B Evaluating SER variations using the proposed simulation approach

Appendix B.1 Test chip design and experimental setup

To clearly show the advantage of the proposed simulation approach, we use the proposed simulation approach to evaluate SER variations of integrated circuits. Two test chips were designed and fabricated by the commercial 65 nm CMOS technology. The design details of two chips are shown in Table B1. Test-A was constructed by the conventional D flip-flop and DICE flip-flop. It was used to investigate SEU characteristics of the sequential circuit cells. Test-B was constructed

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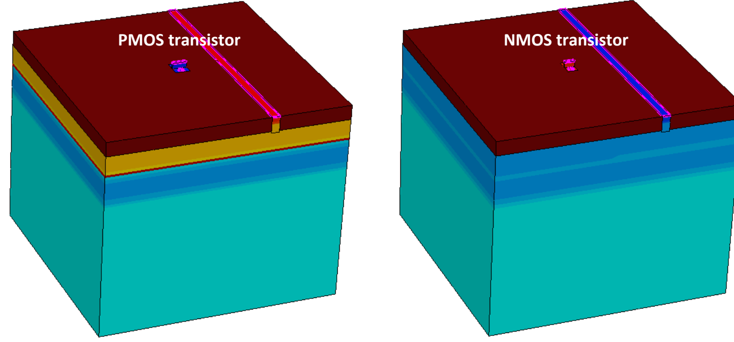

Figure A1 PMOS and NMOS transistor are represented as TCAD models.

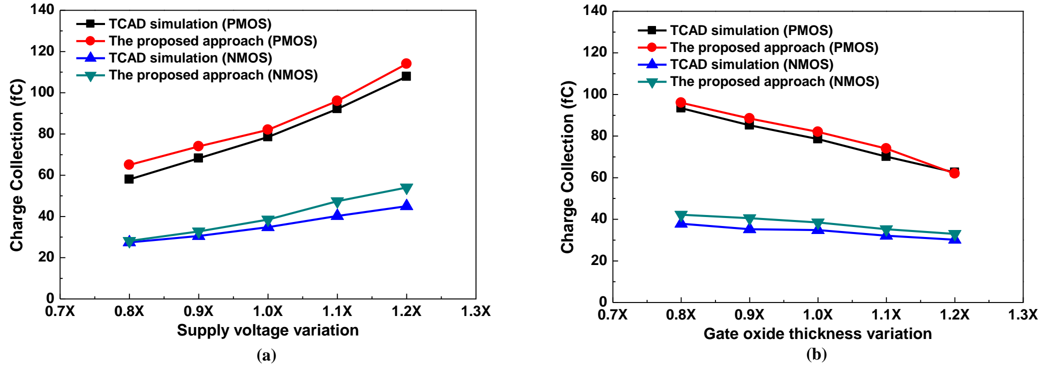

Figure A2 The collected charge of transistors with (a) voltage and (b) gate oxide thickness variations.

Table B1 Test chips used in the experiment

Test no.	Circuit cell	Core voltage	Other feature
Test-A	D flip-flop	1.2V	Dual-well
	D flip-flop	1.2V	Dual-well, Low Vth
	DICE flip-flop	1.2V	Dual-well
Test-B	Inverter chain	1.2V	Dual-well
	Inverter chain	1.2V	Triple-well

by the inverter chain. It was used to investigate SET characteristics of the combinational circuit cells. The simple circuit schemes of Test-A and Test-B are shown in Figure B1. The detailed designs have been described in our previous works [1,2].

To investigate process or operation variations affect the circuit sensitivity, we designed the extra circuit cells in the test chips and set different test conditions during heavy ion experiments. For instance, the conventional D flip-flop with low threshold voltage was designed in Test-A. It was used to investigate the circuit sensitivity with different threshold voltages. The inverter chains were designed in the dual- and triple-well to investigate the circuit sensitivity with different well structures. The core voltage was set from 1.0V to 1.2V and the temperature was set from 300K to 350K during the experiments. They were used to investigate the circuit sensitivity with different operation conditions.

Heavy ion experiments were conducted at the HI-13 Tandem Accelerator in China Institute of Atomic Energy and the Heavy Ion Research Facility in Lanzhou (HIRFL) cyclotrons in Institute of Modern Physics, Chinese Academy of Sciences. The characteristics of the ions used in the experiment are listed in Table B2. The incident ion dose rate was $1 \times 10^4 ions/cm^2 \cdot s$ and the fluence in each incident ion was $1 \times 10^7 ions/cm^2$. All signal (input, output and clock) pins of each test chip were connected to FPGA. Error detection was implemented by FPGA and error counts were exported to the computer by the serial interface during the experiments.

Appendix B.2 Simulation setup

The proposed simulation approach is used to evaluate SEU and SET characteristics caused by process or operations variations. Monte Carlo simulation tool Geant4.9.5 was performed to simulate the particle transportation in the first component. The simulated ion energy, equivalent LET, the ion dose and the fluence were satisfied with the experiment setup. The simulation structure for Monte Carlo simulation contained all active junctions (drains, sources and well contacts). The transistor size and spacing were consistent with the layout topology.

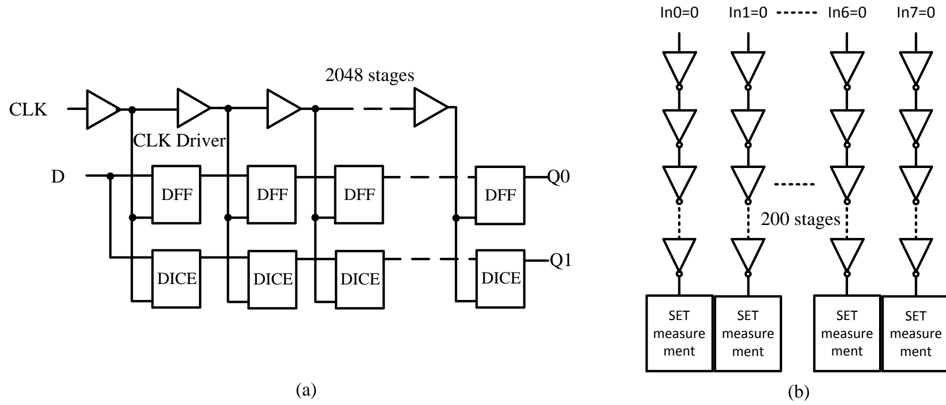

Figure B1 The simple circuit schemes of (a) Test-A and (b) Test-B.

Table B2 Heavy ions used in the experiment

Ion	Energy at the silicon surface (MeV)	Effective LET (MeV·cm^2/mg)	Range (μm)
O	100	3.1	95.2
Cl	165	11.3	51.8
Ti	185	21.2	37.9
Ge	205	37.1	35.5
Bi	923.2	99.8	53.7

Two different model groups were implemented in the second component. The first model group only contained the diffusion collection model and the PABAM model which was represented as the conventional SER evaluation approach. The second model group added the process parameter model which was satisfied with the proposed simulation approach. Based on the calculated transient currents, the circuit responses were simulated and SEE cross sections were determined by HSPICE simulation tool.

Appendix B.3 Evaluating SEU variations of the sequential circuit cells

The comparison between the measurement results and the simulation results are shown in Figure B2. The measured SEU cross sections show obvious discrepancies with difference process or operation conditions. For instance, the SEU cross section of the D flip-flop with low threshold voltage shows about 1.18X than that with normal threshold voltage. The SEU cross section of the DICE flip-flop with low core voltage shows about 3.11X than that with normal operation voltage. These measurement results indicate process and operation variations significantly affect the circuit sensitivity of flip-flops. The simulated results obtained by two simulation approaches show different SEU characteristics. The simulated SEU cross section obtained by the conventional approach shows a certain value. Although it shows a good agreement with the measurement results, the simulated SEU cross section does not reveal the SEU variations caused by different process or operation conditions.

Different from the conventional simulation results, the simulated SEU cross section with the proposed simulation approach does not have a certain value but show a variable value within specific ranges. The Y error bars are represented as the range

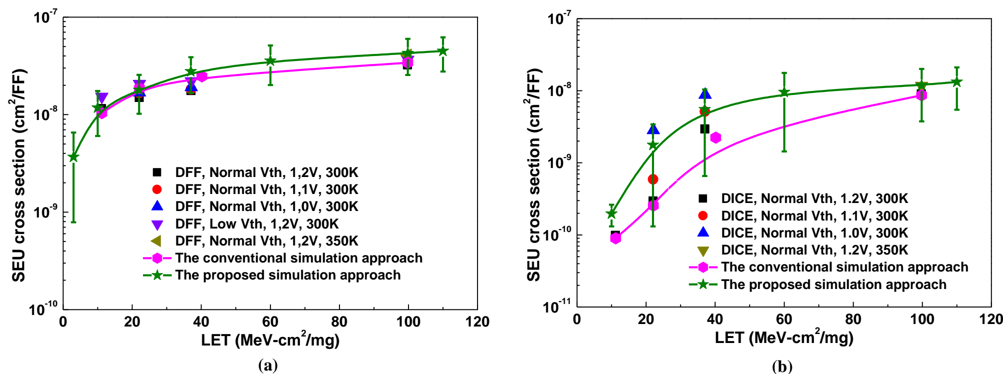

Figure B2 Comparison between the simulated and measured SEU cross sections of (a) D and (b) DICE flip-flop.

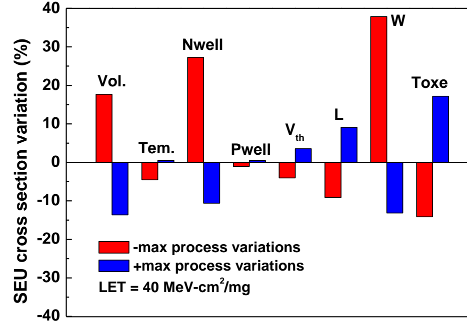

Figure B3 The simulated SEU cross section variations with different process and operation conditions.

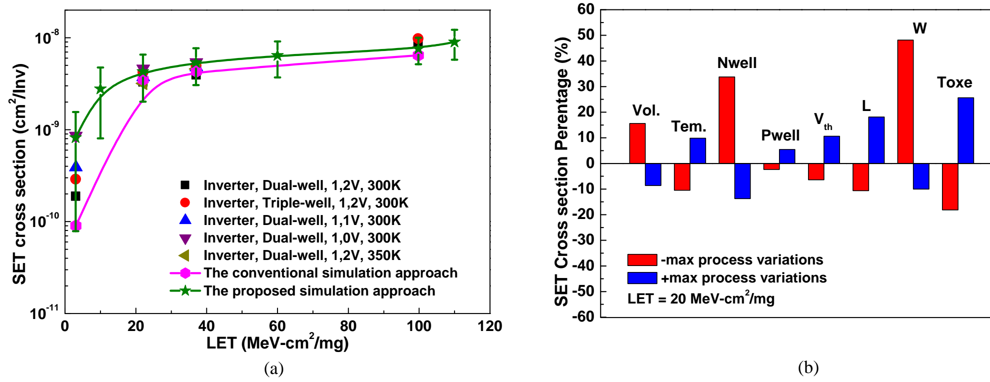

Figure B4 (a) Comparison between the simulated and experimental SET cross sections. (b) The simulated SET cross section variations with different process and operation conditions.

of SEU variations and the point is represented as the average value. When process or operation conditions change, the simulated cross section can still reveal the SEU variations. The simulation results are also satisfied with the measurement results.

It is noteworthy that the proposed simulation approach can also help to investigate the SEU cross section variations caused by each process and operations conditions. Figure B3 shows the SEU cross section variation of D flip-flops with each process and operation conditions. Based on the simulation results, the circuit sensitivity of D flip-flops is significantly influenced by the variation of the operation voltage, the N-well doping, the gate width and the gate oxide thickness. The operation voltage, the gate width and the gate oxide thickness affect the driving current of transistors. They change the critical charge and affect the SEU characteristic of D flip-flops. The N-well doping variation significantly affects the carrier diffusion and the bipolar amplification effect. Therefore, it affects the charge collection and finally affect the SEU characteristics of flip-flop.

Appendix B.4 Evaluating SET variations of the combinational circuit cells

The proposed simulation approach is also performed to evaluate SET characteristics caused by process or operation variations. The measurement and simulation results are shown in Figure B4(a). Similar with SEU results, the measured SET cross sections change obviously with different process and operation conditions, especially for low LET value. Compared with the measurement results, the simulation results obtained by the conventional approach have obvious discrepancies because it is hard to evaluate the SER variations if process or operation conditions change. For the proposed simulation approach, the simulated SET cross sections are similar with the measurement results although process and operation conditions change. The proposed approach can also help to investigate the SET cross section variations caused by each process and operations conditions, as shown in Figure B4(b). Simulation results indicate the capability of the proposed simulation approach. It is suited for evaluating the SEU or SET characteristics with different process and operation conditions.

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