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A four-channel time-interleaved 30-GS/s 6-bit ADC in 0.18 μm SiGe BiCMOS technology

Xiaoge ZHU[1,2], Danyu WU[1], Lei ZHOU[1], Yinkun HUANG[1], Jin WU[1] & Xinyu LIU[1*]

[1]*Insititute of Microelectronics, Chinese Academy of Sciences, Beijing* 100029*, China;*
[2]*University of Chinese Academy of Sciences, Beijing* 100049*, China*

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Dear editor,

Analog-to-digital converters (ADCs) with GHz bandwidth have widely been used in wideband communication systems, data acquisition systems and test and measurement instruments. As key elements of these systems, wideband high speed ADCs in multi-GHz range are in increasing demands. Folding and interpolating ADCs are perfectly suitable to these performance because of its direct conversion mode with limited hardware consumption [1]. Recently, the time-interleaved successive-approximate-register (TI SAR) ADCs have become an attractive architecture for high speed and moderate speed application in advanced nanometer CMOS technology for its small area and power efficiency [2]. They are very suitable for high volume system-on-chip (SOC) application. However, the production cost in the advanced silicon process is unbearable for the limited quantitive products. Compared with CMOS technology, SiGe BiCMOS technology has advantages of high speed, low 1/f noise, low mismatch and high reliability with low cost, which make it very suitable to built low volume high speed ADCs [3]. Additional, time-interleaving technique increases the conversion rate of a data converter by using a number of converters working in parallel for a simultaneous quantization of input samples. It can also reduce the die size and relax the requirements on fabrication process at the same time [4]. Hence, a four-channel time-interleaved folding and interpolating (F&I) ADC was designed to achieve the target of 30-GHz sampling rate and 6-bit resolution.

Proposed ADC design. Figure 1(a) presents the system architecture of the 30-GS/s 6-bit four-channel TI ADC. The analog input is fed into a wideband input buffer. Then the signal is fed into four sub-ADCs, each consists of a track-and-hold amplifier (THA), a reference generator and a 6-bit ADC core based on F&I architecture. A base-4 F&I configuration with analog pre-processing circuits is adopted to realize the 6-bit sub-ADC. Each sub-ADC is made up of F&I circuits, analog pre-processing circuits, comparators, coarse encoder and fine encoder that is similar with [5]. Some intermediate signals of the F&I stage are selected to fed into the analog pre-processing circuits to form the most-significant-bits (MSB) signals. They are also used to avoid the glitch code of the ADC outputs. The outputs of the four sub-ADCs are fed into 24-lane full rate high speed data interface for measurement. A foreground calibration method was ultilized to correct time-skew, gain and offset mismatches between channels. The ADC also integrates a CMOS controller circuit with 4-wire SPI interface which enables the ADC to be configured

* Corresponding author (email: xyliu@ime.ac.cn)

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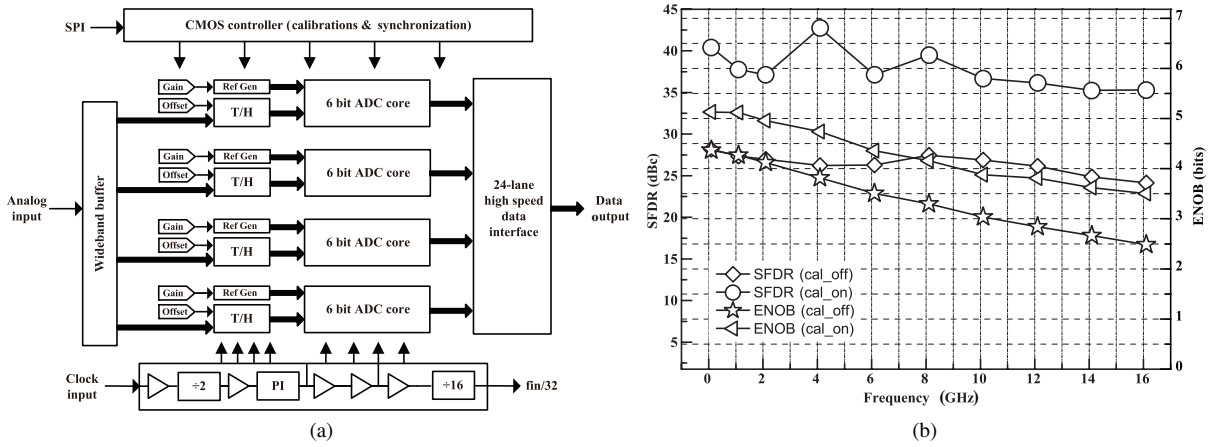

Figure 1 The overall architecture and measured results of the proposed ADC. (a) The overall architecture of the proposed ADC; (b) SFDR and ENOB versus input frequency.

and calibrated conveniently.

The wideband input buffer provides constant input impedence and reduces kickback noise from sub-channels for better input signal quality. But the big parasitics from long routing limits the signal bandwidth. Bandwidth boosting and cascade structure is adopted to overcome this problem. The bandwidth boosting skill gives peaking at high frequency. Meanwhile, cascade structure offers reduced signal swing and small equivalent resistance. All these techniques push the signal bandwidth about 5 GHz. Additional, all of the components within the input path including the PCB-to-SMA connector, PCB traces, bond wires and input pads have a negative effect on bandwidth. 3-D electromagnetic simulation is performed to model and optimize the performance of the whole input path. The simulation shows the proposed input buffer has a very flat frequency response with DC$\sim$16 GHz and has a excellent -3 dB bandwidth beyond 25 GHz without de-embedded.

The THA in each channel adopts master-slave type to achive required linearity and bandwidth [6]. The master is optimized in order to obtain a good linearity with a large bandwidth to sample high frequency signals and the slave to achieve a high isolation to maintain the sample before digitalization. Additional, the holding time is almost doubled in the proposed architecture which relaxs the folding bandwidth requirment by $2\times$ for a given sample rate. The switched emitters follower (SEF) is well known for its robustness [7]. However, in high frequency application, the unbalenced charge-discharge current and feedthrough effect weaken the linearity which were alleviated by a inserted resister and capacitanve, seperately [5].

With the continual increase of speed in high speed ADC, the output data-rate for digital I/O block has increased aggressively. Traditional digital logic such as LVCMOS and LVDS cannot satisfy the I/O speed requirement of this high speed ADCs. Instead, the current-mode-logic (CML) output buffer is adopted in the data interface which can reach 28 Gbps in [8]. Fortunately, an Xilinx Virtex Ultrascale FPGA XCVU190 has as much as 120 alternating-current couping transceivers that are capable of supporting 2.8-Tb/s data transfer. It only needs 24 high speed serial lanes to achieve 180 Gbps data rate at 7.5 Gbps per lane. For achieving good signal integrity, the DC voltage balence and enough transitions over a period of time are necessary for high speed serial interface. In this ADC, a pseudo random binary sequence (PRBS) generator is ultilized to insert transitions to the ADC data as a scrambler. Meanwhile, the probability of 1 and 0 in the scrambled datas are almost balenced. Additional, the proposed interface can be configured between pure PRBS-7 pattern mode and scrambing data mode. The pure PRBS-7 pattern mode can also be used to synchronous the output datas of the 24 lanes which can also realize multi-device synchronization.

The operating speed of the TI ADC can linear grow by increasing the number of parallel ADC channels. However, in reality, mismatches between channels introduce additional errors which degrade the performance of the TI-ADC, such as timing, gain and offset mismatches. Those mismatches must be calibrated to achieve satisfactory performance in the design of TI-ADCs [9]. For 6-bit resolution and 16-GHz input frequency, the σ_t between channels must be low than 142 fs with 3 dB penalty. The calibration of the timing mismatches between different channels is accomplished by using phase interpolator. The maximum adjustment range is determined by time interval between the clock signal and its delayed replica. A 8-bit dif-

ferential current DAC is used to implement phase tuning with 80 fs/step. In the sub-ADC, the folding signals are derived from the reference signals and the input sampling signals. The range of reference signals can be adjusted to match the differential range input signals so that to avoid the errors induced by gain mismatches between channels. A 6-bit current DAC is used to adjust the reference range to be less 1%. The offset calibration is inserted in the output buffer of the track and hold amplifier. Adjusting the current passes through NPN differential pair, the output offset voltage is calibrated. The offset calibration can get a range of ±8 LSB with a step of 0.25 LSB through the 6-bit current-type DAC.

A kind of foreground calibration module was built in the FPGA to eliminate all the 3 kinds of differences automatically. The calibration flow is as follows: At first, we send a sine wave to the ADC input, all the data are transmitted to the FPGA through high speed data interface, then we have used a simple algorithm in the FPGA to calculate and accumulate the error between the sub ADCs. Then, the accumulated error has been converted and sent to the ADC by the SPI interface. It includes 3 independent close loops which performs dynamic fine tuning of all the 4 sub-ADCs gain, offset and clock delay. After the tuning loop became stable, we make the gain, offset and delay control registers fixed, then the ADC can be used to capture any kind of signals. Because of the calibration architecture only needs adder and subtractor, it only needs several consecutive data frames (it means that it does not need to deal with all the ADC data), which makes it suitable for on-chip implementation, consuming only a few amount of power and die area.

Measurement results. The test chip is fabricated using 0.18-μm 1P6M SiGe BiCMOS technology. All of measurement results are reported at a sampling rate of 30 GHz. The measured ENOB and SFDR versus input frequency are shown in Figure 1(b). The ADC achieves the SNDR of 32.64 dB at low frequencie and maintains the SNDR higher than 22.83 dB up to 16 GHz. The SFDR stays above 35 dB up to 16 GHz. The measured static performance shows that the DNL is within +0.2/−0.2 LSB and the INL is within +0.4/−0.4 LSB. The core ADC consumes 8.5 W from the supplies of 4.5 V and 3.3 V (6.5 W excluding the data interface). The standard figure-of-merits (FOM) is 18.9 pJ/conversion-step with low frequency ENOB.

Conclusion. A four-channel time-interleaved 30-GS/s 6-bit ADC with full data rate interface has been demonstrated. The ADC has a measured analog bandwidth of above 18 GHz and ENOB above 5 bits. It can transmit all of the ADC output data to an commercial FPGA in real-time. The whole chip including high speed data interface consumes 8.5 W of power and has a die size of 4.0 mm × 3.4 mm (including pads).

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