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A low power V-band LC VCO with high Q varactor technique in 40 nm CMOS process

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Dear editor,

Demand for higher data transmission rate, particularly in the modern communication systems, has been increasing over the years. For example, the IEEE standard 802.15.3c specifies more than 2 Gbps data transmission rate, which pushes the frequency band up to 60 GHz. In the transceiver, the working frequency of VCO is in 60 GHz, and that has attracted many people to study it [1, 2]. However, implementing high speed voltage-controlled oscillator (VCO) through CMOS technology can be extremely challenging because of the intrinsic cut-off frequency limitation of CMOS devices. The LC-tank VCO structure can be used to address this issue [3], but its phase noise is poor and the power consumption is high [4, 5]. In the previous studies, the researchers use the intrinsic-tuned technique and capacitance-splitting technique to improve VCO performance, but they are complicated [6].

When the frequency increases, the power consumption of VCO will also increase significantly because the circuit nodes switch faster in different states. The Q factor of varactor will also deteriorate rapidly and cause deterioration of the VCO phase noise at a higher frequency. For example, when the working frequency changes from 2.4 GHz to 60 GHz, the Q factor of the varactor will deteriorate from 137.8 to 5.58. Therefore, determining how to improve the varactor performance is crucial for the millimeter wave VCO design.

To overcome the technique difficulties, the new VCO architectures have to be explored in addition to leveraging on the traditional approaches. In this letter, we adopted the novel VCO architectures to better trade off among the performance, power and area. In order to improve the phase noise and reduce the power consumption, the low power technique is adopted in the LC tank, which can improve the Q factor of varactor. Measurement results show the novel VCO demonstrates the better figure-of-merit (FOM) compared to the traditional VCO structure.

Circuit architecture. In traditional approach of VCO, two NMOS transistors constitute the negative resistance mechanism to maintain the resonator operation and two varactors are used to tune the frequency of VCO. This structure is simple but its performance and power consumption are not good enough for the high frequency applications. The main reason is the sharp deterioration of the varactor Q factor. In this let-

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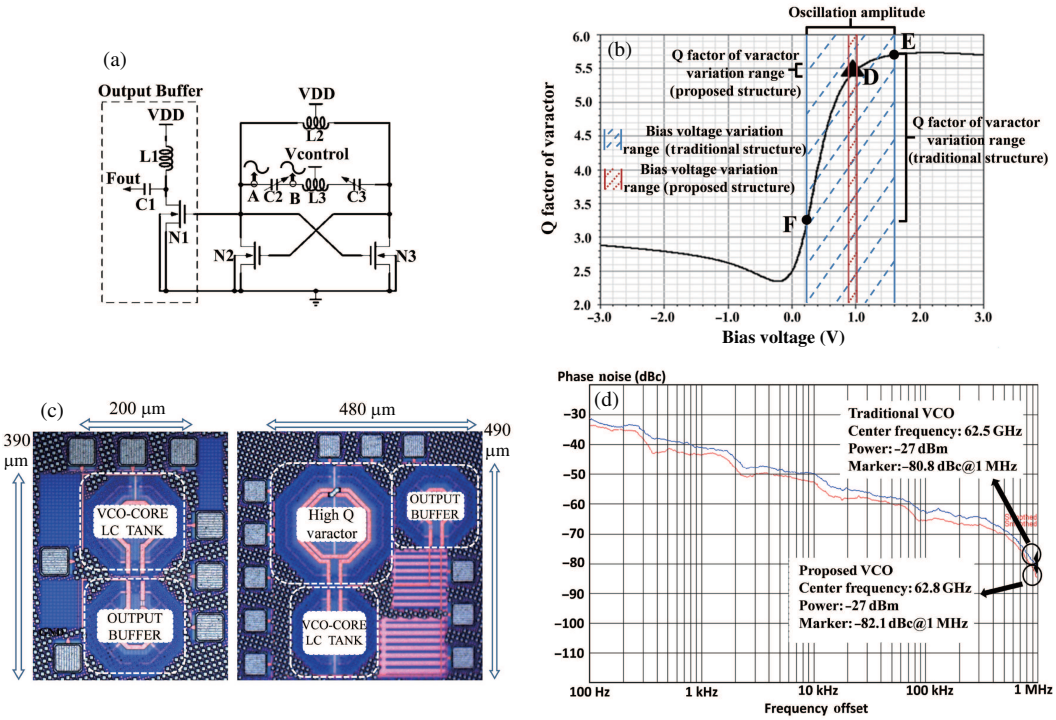

Figure 1 (Color online) (a) Proposed VCO structure; (b) the varactor's Q factor working ranging of two structures; (c) traditional VCO micrograph and proposed VCO micrograph; (d) the measured phase noise of the two VCO dies.

ter, we present a novel low power LC-VCO structure as illustrated in Figure 1(a). In this novel architecture, an inductor is inserted in between varactors C2 and C3. The waveform of varactor's node is oscillating instead of a fixed voltage level.

Figure 1(b) shows the correlation between the Q factor and the bias voltage of the varactor when the operating frequency reaches 60 GHz. To obtain a better Q factor, we need to set the bias voltage in black triangular region D, which can achieve the lowest power consumption and high performance. The low Q factor states of varactors obtained through traditional approaches will appear in each oscillation cycle because the voltage of varactor is fixed at one end and fluctuates at the other end. These low Q factor states will increase power consumption and cause deterioration in the performance. In this letter, we propose a low-power design, in which an inductor L3 is inserted in between two varactors. Although the voltage of node B is no longer fixed, the varactors always work in the area of high Q factor throughout the entire oscillation period.

In the design consideration, the inserted inductor is working in the capacitance region. In this condition, the voltages of two ends of varactor have the same phase. In the traditional structure, the voltage difference is equals to oscillating voltage minus the control voltage. In the proposed structure, the voltage difference is equals to one end of varactor voltage minus another end of varactor voltage. The voltages of two ends of varactor have the same phase, so the voltage difference is degraded. With a smaller voltage difference, the average Q factor of varactor is improved. In this way, it can improve performance and reduce power consumption.

Ploss (power consumption) of VCO depends on QC (Q factor of varactor) and QL (Q factor of inductor). When the operating frequency is relatively low, for example 2.4 GHz, QC is much larger than QL, the Ploss depends on QL. But in the V-band, the QC decays quickly and is less than the QL. Therefore, Ploss depends on QC. With the low power structure, the VCO power consumption is smaller than the traditional one. The simulation results show that the power consumption can be reduced by 20%. Moreover, based on Lesson's noise model, phase noise depends on the quality factor of the resonant circuit. With increasing Q factor of varactor, the quality factor of the resonant circuit will also increase, and then phase noise can be improved.

Experimental results. The prototype of the VCO is implemented by the 40 nm CMOS process. The output signal is captured by Agilent E9030A spectrum analyzer. Since the spectrum analyzer

E9030A has its measurement limit up to 26.5 GHz, another 50–90 GHz Spread Spectrum instrument (Agilent M1917E) is used to down-convert the frequency of the VCO output signal. The input voltage signal is provided by Agilent 4156C DC power.

The prototype of the VCO is implemented by the 40 nm CMOS process. Its microphotograph is illustrated by Figure 1(c). The proposed VCO consumes 10.4 mW power dissipation when the power supply is 1.2 V and the operating frequency is 62.8 GHz. Under the same power supply conditions, the traditional VCO consumes 13.6 mW while operating at 62.5 GHz. Figure 1(d) shows the phase noise of two VCO structures. The traditional VCO structure achieves −81 dBc/Hz @1MHz phase noise and FOM is −166. However, an excellent phase noise is achieved by low power technique. The proposed VCO achieves −82 dBc/Hz@1MHz phase noise and FOM is −168. Compared with the traditional design, its power consumption is reduced by 23.5%. Moreover, compared to the previous designs (reported by [4, 5, 7, 8]), the proposed VCO can improve the FOM by 1–17.

Conclusion. A V-band LC VCO was implemented by domestic 40 nm CMOS Process. Using low power techniques, the proposed V-band VCO achieved the phase noise of −82 dBc/Hz@1MHz, and power consumption of 10.4 mW (including output buffer), all under 1.2 V power supplies. Compared with the traditional VCOs, the measured FOM of proposed VCO was optimized from −166 to −168, and its power consumption was reduced by 23.5%, and this is the first 60 GHz CMOS VCO in domestic 40 nm technology.

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References

1 Yi X, Boon C C, Liu H. A 57.9-to-68.3 GHz 24.6 mW frequency synthesizer with in-phase injection-coupled QVCO in 65 nm CMOS technology. IEEE J Solid-State Circ, 2014, 49: 347–359
2 Luo J, Zhang L, Zhang L, et al. A 24 GHz low power and low phase noise PLL frequency synthesizer with constant KVCO for 60 GHz wireless applications. In: Proceedings of IEEE International Symposium on Circuits and Systems (ISCAS), Lisbon, 2015
3 Chen Y M, Wang H, Yan S C, et al. A 10 GHz multi-phase LC VCO with a ring capacitive coupling structure. Sci China Inf Sci, 2012, 55: 2656–2662
4 Chang Y-H, Chiang Y-C, Yang C-Y. A V-band push-push VCO with wide tuning range using 0.18 μm CMOS process. IEEE Microw Wirel Comp Lett, 2015, 25: 115–117
5 Fei W, Yu H, Fu H, et al. Design and analysis of wide frequency-tuning-range CMOS 60 GHz VCO by switching inductor loaded transformer. IEEE Trans Circ Syst I: Regular Papers, 2014, 61: 699–711
6 Li L, Reynaert P, Steyaert M. A 60 GHz CMOS VCO using capacitance-splitting and gate-drain impedance-balancing technique. IEEE Trans Microw Theory Tech, 2011, 59: 406–413
7 Weber R, Schwantuschke D, Brückner P, et al. A 67 GHz GaN voltage controlled oscillator MMIC with high output power. IEEE Microw Wirel Comp Lett, 2013, 23: 374–376
8 Trivedi V P, Kun-Hin T, Huang W M. A 77 GHz CMOS VCO with 11.3 GHz tuning range, 6 dBm output power, and competitive phase noise in 65 nm bulk CMOS. In: Proceedings of IEEE in Radio Frequency Integrated Circuits Symposium (RFIC), Baltimore, 2011. 1–4