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Design of low power 4×40 Gb/s laser diode driver for parallel optical transmission systems

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Compared with conventional electrical interconnection technology, optical interconnection has the merits of anti-interference, small signal loss, long transmission distance and so on. Furthermore, parallel optical interconnects become the crucial technique to solve the problem of large capacity data transmission in high-speed transmission systems. The parallel mode can decrease transmit rate of every optical fiber, reduce the demands for optical devices and decrease the cost of optical interconnects [1–3].

Optical transmitter chip which consists of a multiplexer and a laser diode driver (LDD), is the crucial module for the optical fiber communication system. The LDD is used to amplify the output signal of multiplexer and turn the electrical signal into optical one.

The bipolar transistor of SiGe BiCMOS technology has higher operating frequency and superior driving ability, so many high-speed LDDs are designed in SiGe BiCMOS [4, 5]. Ref. [4] has relatively large output swing, but it consumes more power of 3600 mW. The large power consumption is not suitable for high-density optical interconnects. Using low-power bandwidth enhancement techniques, a 40 Gb/s VCSEL driver IC is successfully developed in 180-GHz SiGe BiCMOS technology in [5]. But the passive peaking inductors in output stage occupy large chip area, which cannot retain 250 μm channel space for parallel optical transmission.

A 4-channel 40 Gb/s parallel VCSEL driver array in GF 0.13 μm SiGe BiCMOS technology is proposed in this article. The pre-emphasis technique of RC parallel negative feedback makes it acquire high operating rate and occupy small chip area.

Circuit design. The function of VCSEL driver is to convert the electrical signal to optical one. Due to the driving signal of voltage or current, the VCSEL driver can be divided into current type driver and voltage type driver. This article proposed the voltage type driver because it is suitable for driving common-cathode type VCSEL.

The structure of the 40 Gb/s laser diode driver consists of input buffer stage, pre-amplifier stage and output driver stage.

The input buffer stage has three functions of impedance matching, DC bias, and voltage level shift. The 50 Ω impedance matching is designed to reduce the high frequency reflection of the signal, which goes through transmission line to the pads of chip.

Pre-amplifier stage is located between the input buffer stage and the output driver stage, amplifying the signal to a large swing for the latter

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output driver stage. Due to the large modulation current by the VCSEL, large size devices should be adopted which leading large parasitic capacitance. The large capacitance will limit the bandwidth, especially in the design of high-speed circuit. Therefore, the bandwidth expanding technique should be exploited in this 40 Gb/s LDD circuit. Shunt peaking inductors are used to expand the bandwidth in most high-speed laser driver designs, while it is not suitable for the high-density parallel optical transmission systems. The preamplifier stage in this article adopts emitter series resistance structure constituting negative feedback to extend bandwidth and stabilize gain.

Because the VCSEL is a single terminal device, the LDD driver should have the function of turning differential input signal to single-ended output signal. Figure 1(a) presents one kind of common-cathode LDD driver stage circuit, but it is inappropriate for the supply voltage requirements. The emitter follower in Figure 1(a) leads a $V_{\mathrm{BE,ON}}$ voltage; adding another 2.8 V forward operating voltage of VCSEL. The 3.3 V voltage supply is not sufficient to produce large output swing.

The schematic of the proposed driver stage for common-cathode structure LDD is shown in Figure 1(b), in which the resistor of R_{out} sources current into VCSEL. The modulation voltage V_{mod} controls the modulation current amplitude, and the bias current of VCSEL depends on the bias voltage V_{bias}.

To expand the bandwidth, the pre-emphasis technique of RC parallel negative feedback is introduced in the driver stage. The equivalent transconductance G_{m} of the driver stage is

$$G_{\mathrm{m}} = \frac{g_{\mathrm{m}}}{1 + g_{\mathrm{m}}\left(\frac{R_{\mathrm{e}}}{2}||\frac{1}{2sC_{\mathrm{e}}}\right)} = \frac{g_{\mathrm{m}}(sR_{\mathrm{e}}C_{\mathrm{e}}+1)}{sR_{\mathrm{e}}C_{\mathrm{e}}+1+\frac{g_{\mathrm{m}}R_{\mathrm{e}}}{2}}, \tag{1}$$

where g_{m} is the transconductance of Q_1, and $R_{\mathrm{e}}/2||1/(2sC_{\mathrm{e}})$ is the parallel impedance of the feedback circuit of R_{e} and C_{e}. One pole and one zero contained in the equivalent transconductance G_{m} are

$$p_1 = \frac{1+\frac{g_{\mathrm{m}}R_{\mathrm{e}}}{2}}{R_{\mathrm{e}}C_{\mathrm{e}}}, \tag{2}$$

$$z_1 = \frac{1}{R_{\mathrm{e}}C_{\mathrm{e}}}. \tag{3}$$

If the load resistor and load capacitance at the output node of the VCSEL are expressed as R_{L} and C_{L} respectively, the pole frequency produced by the output node is $1/(R_{\mathrm{L}}C_{\mathrm{L}})$.

When $R_{\mathrm{e}}C_{\mathrm{e}} = R_{\mathrm{L}}C_{\mathrm{L}}$, the pole at the output node can be offset by z_1 in (3). Therefore, p_1 in (2) becomes the dominant pole. The p_1 in (2) can be substituted as

$$p_1 = \frac{1+\frac{g_{\mathrm{m}}R_{\mathrm{e}}}{2}}{R_{\mathrm{e}}C_{\mathrm{e}}} = \frac{1+\frac{g_{\mathrm{m}}R_{\mathrm{e}}}{2}}{R_{\mathrm{L}}C_{\mathrm{L}}}. \tag{4}$$

It can be seen that the bandwidth of the output stage is expanded $(1 + g_{\mathrm{m}}R_{\mathrm{e}}/2)$ times larger. Although the gain of the output stage is restricted to a lower value due to bandwidth expanding, it is sufficient for the LDD.

Experimental results. The 4×40 Gb/s VCSEL driver occupies an area of 0.58 mm×1.2 mm about 0.7 mm^2. The core area of each channel is only 0.05 mm^2. Without peaking inductors, the channel space can be constricted to 250 μm which is exactly appropriate to commercial parallel VCSEL array. The whole current drawing from the 3.3 V supply voltage is 236 mA, hence the power consumption of each channel is about 195 mW.

The large signal performance was measured by applying a differential pseudo random bit sequence (PRBS $2^{31}-1$) data, and the output signal was captured by Agilent DCA 86100A oscilloscope. The eye diagram of the output signal working at 25 Gb/s rate is clear and wide-open, and the output amplitude is about 476 mV corresponding to 9.5 mA current. The eye diagram of 38.5 Gb/s data is shown in Figure 1(c), and it has the output amplitude of 350 mV corresponding to 7 mA modulation current.

The specifications of the 4-channel 40 Gb/s parallel LDD chip in 0.13 μm SiGe BiCMOS technology are compared with other published works [5–7]. Ref. [5] has the least power consumption per data rate, but it has minimum output modulation current. The proposed parallel 4× 40 Gb/s LDD chip features minor power consumption per data rate 4.9 mW/(Gb/s) and least area. The power per data rate achieved is much less than the power budget of 10 mW/(Gb/s) of future high-density optical interconnects.

Conclusion. The low power 4×40 Gb/s parallel VCSEL voltage driver array was successfully implemented in 0.13 μm SiGe BiCMOS technology. The pre-emphasis technique of RC parallel negative feedback is employed in the output driver stage to acquire high bandwidth and large output amplitude. The modulation current swing is more than 7 mA, and the bias current is about 2 mA. The power consumption of single channel is only 195 mW for a single 3.3 V supply. The power efficiency of 4.9 mW/(Gb/s) is successful for high-density parallel optical interconnects.

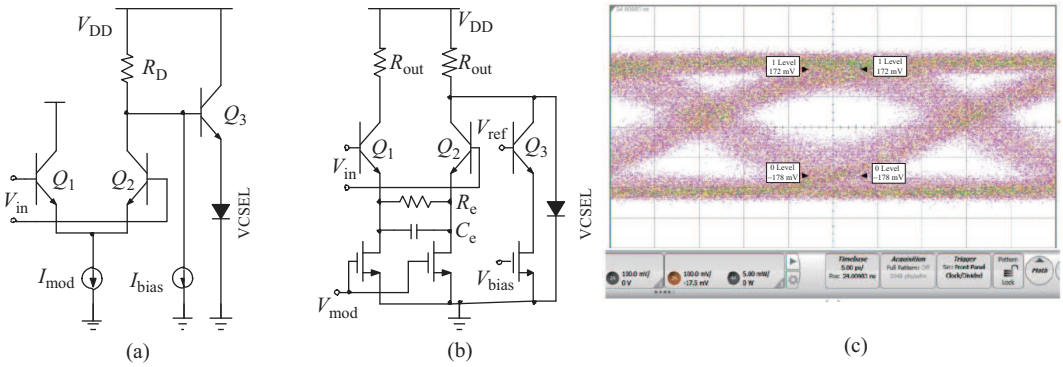

Figure 1 (Color online) Schematic and experimental results. (a) Driver stage with emitter follower; (b) proposed driver stage; (c) eye diagram of 38.5 Gb/s output data.

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References

1 Kromer C, Sialm G, Morf T, et al. A 100 mW 4×10 Gb/s transceiver in 80 nm CMOS for high-density optical interconnects. IEEE J Solid-State Circ, 2005, 40: 2667–2679
2 Schow C L, Doany F E, Chen C, et al. Low-power 16×10 Gb/s bi-directional single chip CMOS optical transceivers operating at $<$ 5 mW/Gb/s/link. IEEE J Solid-State Circ, 2009, 44: 301–313
3 Chen Y M, Zhu L, Zhang L, et al. 4-channel, 40 Gb/s front-end amplifier for parallel optical receiver in 0.18 μm CMOS. Sci China Inf Sci, 2013, 56: 042402
4 Aroca R A, Voinigescu S P. A large swing, 40-Gb/s SiGe BiCMOS driver with adjustable pre-emphasis for data transmission over 75-ohm coaxial cable. In: Proceedings of IEEE Compound Semiconductor Integrated Circuit Symposium, Portland, 2007. 1–4
5 Sedighi B, Scheytt J C. 40 Gb/s VCSEL driver IC with a new output current and pre-emphasis adjustment method. In: Proceedings of Digest of IEEE/MTT-S International Microwave Symposium, Montreal, 2012. 1–3
6 Kucharski D, Kwark Y, Kuchta D, et al. A 20 Gb/s VCSEL driver with pre-emphasis and regulated output impedance in 0.13 μm CMOS. In: Proceedings of Digest of IEEE International Solid-State Circuits Conf, San Francisco, 2005. 222–223
7 Schick C, Feger T, Sonmez E, et al. Broadband SiGe HBT amplifier concepts for 40 Gbit/s fiber-optic communication systems. In: Proceedings of European Microwave Conference, Paris, 2005. 113–116