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Special Focus on Millimeter Wave Communications Techniques and Devices for 5G

An 80–83 GHz CMOS DCO based on DiCAD technique for size, linearity and noise optimization

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Dear editor,

It becomes practical to implement competitive mm-wave circuits in advanced deep-submicron CMOS process, with the scaling CMOS technology and innovative circuit techniques. Among various mm-wave circuit blocks, the oscillator draws special attention since mm-wave signal sources are demanded in almost all mm-wave electrical systems. However, big challenges still exist to implement a high performance mm-wave oscillator with the traditional approach. Varactors and switched capacitor arrays or switchable coupled tanks are usually used to realize the frequency tuning in LC oscillator at low frequency band below 10 GHz. However, the Q-factor of these frequency tuning components becomes very low and significantly deteriorates the phase noise performance of the oscillator.

Digitally-controlled oscillator (DCO) techniques are proposed to overcome the shortcomings of the traditional oscillator approach [1–4]. However, the fine frequency tuning is difficult to realize since any direct switching in the tank would introduce much loss and parasitic capacitance at mm-wave. Floating metal strip slow-wave structure underneath the transmission line, coplanar waveguide and inductor has been proposed to realize the fine frequency tuning in the frequency up to mm-wave [5–8]. This approach can reduce the substrate loss, improve the quality factor and configure a large range of effective permittivity, making it a promising method to overcome the problems mentioned above.

In this letter, the digital control artificial dielectric (DiCAD) technique is used to realize the fine frequency tuning in the mm-wave DCO. The quality factor of the formed tank is not deteriorated by avoiding the direct switching in the tank. With this approach, an 80–83 GHz digitally-controlled oscillator (DCO) has been implemented in 65 nm CMOS and the measured results show that the DCO achieves a tuning range of 2.8 GHz with <-110 dBc/Hz phase noise at 10-MHz offset over the tuning range. Compared with [2–4], the DCO in this work achieves more superior FOM of -184.0 dBc/Hz, even with much higher oscillation frequency.

DiCAD differential transmission line. The DCO in this work uses the traditional LC-tank-based oscillator core with one cross-coupled pair to compensate the loss of the LC tank. The LC tank in the DCO is segmented into three sections, including coarse tuning bank, medium tuning bank and fine tuning bank. The coarse tuning bank provides a coarse tuning frequency step and aims to widen the tuning range while maintaining high quality factor, the fine tuning bank provides a fine tuning frequency step and aims to achieve the fine frequency resolution, and the medium tuning bank bridges the frequency gap between coarse tuning

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and fine tuning with a medium tuning frequency step. The coarse/medium and fine tuning banks tune the capacitance C and the inductance L in the LC tank to implement the tuned oscillation frequency by utilizing the DiCAD-based differential transmission line technique and the DiCAD-based inductor technique, respectively.

The DiCAD transmission line (TL) was first introduced in [8] to change the effective dielectric constant. Some floating metal strip pairs are inserted into the silicon dioxide underneath the DiCAD differential transmission line (DTL).

The floating metal strip pairs, each of which is connected with the MOS switch, distribute homogeneously along the DTL. The MOS switches control the underneath strip pairs to be shorted or opened and the effective permittivity is changed as a result. The trade-off between Q-factor and the tuning range is totally determined by the size of the MOSFET switches.

The DiCAD DTL can replace the varactors and MIM/MOM-based switched-capacitor arrays used in the conventional oscillators to realize the frequency tuning while maintaining high Q quality factor. It also avoids the interconnections used in the traditional oscillators to connect the capacitors.

DiCAD DTL-based coarse and medium tuning. The DiCAD DTL is used to realize coarse and medium tuning. The effective dielectric constant is completely determined by the metal layers as well as physical parameters of the transmission line and floating metal strips beneath it. This work utilizes the top three metal layers M9 to M7 to implement the 5.855 μm thick DTL for coarse tuning, M6 to form the underlying floating strip pairs. The height space between M6 and M7 is the smallest among the top four metal layers, which leads to a large change in capacitance while maintaining a compact size. The DTL is 41.5 μm long, 18 μm wide with 18 μm space. The coarse tuning is realized with 7 strip pairs whose width and space are 0.6 μm and 0.3 μm, respectively. Only the top metal M9 is used to implement the DTL for medium tuning and the 20 strip pairs beneath it are 1.2 μm wide with 0.3 μm space. The sizes are optimized to achieve the optimum design trade-off among the tuning range, frequency resolution, quality factor and size compactness.

In the final implementation, when the switch control code changes one bit, the coarse tuning introduces 0.49 fF capacitance variation which would result in 430 MHz oscillation frequency step for this 80 GHz DCO. The medium tuning only introduces 0.029 fF capacitance variation instead. The total capacitance variation ratio of the DiCAD DTL (including coarse tuning and medium tuning) is 1.18. The minimum simulated Q-factor is 25.8, which is much higher than the varactors.

DiCAD inductor-based fine tuning. The DiCAD transmission line is not the only structure to obtain the artificial dielectric effect. The similar effect can be achieved by inserting floating metal strip pairs underneath the inductor. But there is a big difference between these two structures. The transmission line based structure is an open-circuited stub while the inductor based structure is a short-circuited stub. Looking into the differential input of these two structures, the change of the artificial dielectric is homogeneous in the DiCAD transmission line while the inductor sees a decreasing capacitive load as the floating metal strip pairs approach to the central tap of the inductor [2–4].

16 equally distributed floating M6 strip pairs with 0.6 μm width and 0.6 μm space are placed beneath the inductor. Smaller resolution can be obtained by putting the tuning pairs closer to the central tap of the inductor. The inductor is implemented with the 10 μm wide top metal M9. With 92 μm × 120 μm dimension, the differential inductance ranges from 93.243 pH to 93.326 pH at 80 GHz. The Q-factor is around 44.

Circuit implementation. The schematic of the proposed DCO is shown in Figure 1(a). The core of the DCO is based on the widely used CMOS cross-coupled oscillator topology. The parallel LC tank is used to determine the desired oscillation frequency. A cross-coupled NMOS differential-pair provides the negative resistance to compensate for the loss in the resonant LC tank. The LC tank has been implemented as discussed in the above, which offers a considerable high Q factor at the resonant frequency. So the size of the cross-coupled NMOS pair can be small, which further reduces the fixed capacitance contribution and widens the tuning range. The cross-coupled pair with $W/L=$ 7 μm/60 nm provides sufficient gain to start-up the oscillation. The loop gain is higher than 2 under various process corners.

A cascode common source buffer with good reverse isolation is added to minimize the noise pathway from other blocks into the DCO and make sure the oscillation frequency will not be disturbed by the subsequent blocks.

Measurement results. The proposed DCO has been implemented in 65-nm CMOS and tested on a high-frequency probing station with the DC pads directly wire-bonded to one printed circuit board (PCB). Figure 1(b) shows the chip microphotograph of the propose DCO. The die size, including the PADs, is 0.7 mm × 0.79 mm, while the size of the DCO core is only 0.13 mm × 0.18 mm. The

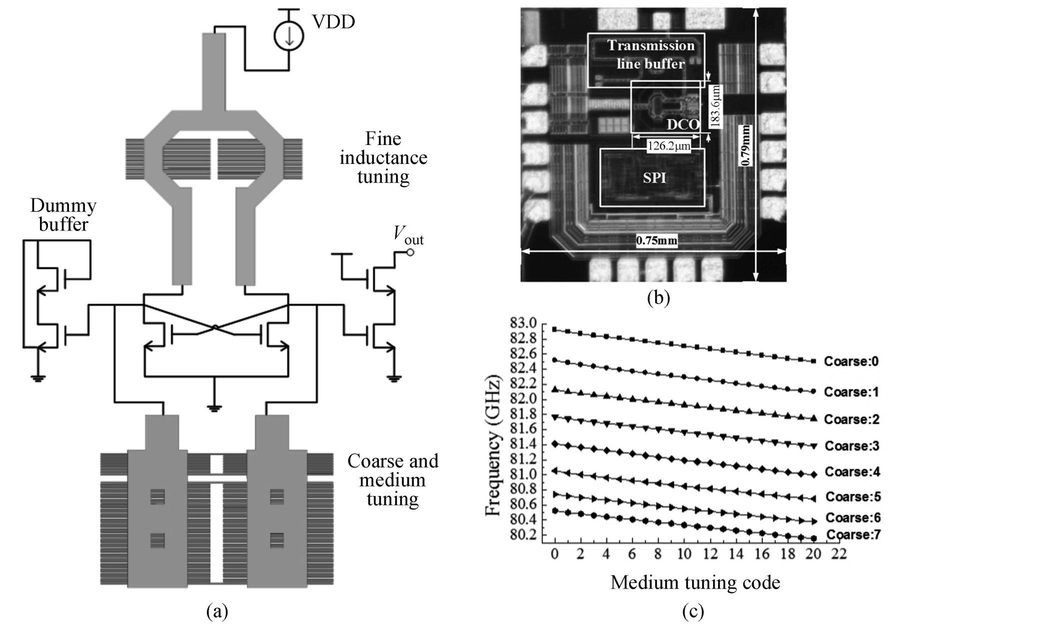

Figure 1 (a) The schematic of the DCO; (b) the microphotograph of the proposed DCO; (c) the measured DCO medium tuning for each coarse tuning bit.

DCO core draws 4 mA current from one 1.0 V power supply.

The DCO has a measured tuning range from 80.2 GHz to 83 GHz, covering about 2.8 GHz tuning range. The measured medium tuning curves at each coarse tuning bit are plotted in Figure 1(c). The medium tuning scheme realizes linear tuning of 20 MHz per bit. Overlap between adjacent frequency tuning curves is essential to guarantee the continuous tuning across the entire tuning range.

Due to the frequency pulling effects, the fine tuning characteristics of the proposed DCO is not available. When the frequency change is less than 1 MHz, the output spectrum does not have obvious response. But half of the fine tuning bits induce the frequency change of less than 1 MHz, and carrier frequency may not be tuned continuously by fine tuning bit across the entire tuning range. This problem could be corrected in the future design by inserting more floating strip pairs.

The measured phase noise of the DCO is −111.8 dBc/Hz at 10-MHz offset (about −90 dBc/Hz at 1-MHz offset) from an 81.16-GHz carrier frequency, corresponding to a FOMT value of −175.3 dBc/Hz and a FOM value of −184.0 dBc/Hz.

Supporting information Appendixes A–D. The supporting information is available online at info.scichina.com and link.springer.com. The supporting materials are published as submitted, without typesetting or editing. The responsibility for scientific accuracy and content remains entirely with the authors.

References

1 Genesi R, de Paola F M, Manstretta D. A 53 GHz DCO for mm-wave WPAN. In: Proceedings of IEEE Custom Integrated Circuits Conference (CICC), San Jose, 2008. 571–574

2 LaRocca T, Liu J, Wang F, et al. CMOS digital controlled oscillator with embedded DiCAD resonator for 58–64 GHz linear frequency tuning and low phase. In: Proceedings of IEEE MTT-S International Microwave Symposium Digest, Boston, 2009. 685–688

3 Wu W H, Long J R, Staszewski R B, et al. High-resolution 60-GHz DCOs with reconfigurable distributed metal capacitors in passive resonators. In: Proceedings of the IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Montreal, 2012. 91–94

4 Wu W H, Long J R, Staszewski R B. High-resolution millimeter-wave digitally controlled oscillators with reconfigurable passive resonators. IEEE J Solid-State Circ, 2012, 48: 2785–2794

5 Huang D, Hant W, Wang N Y, et al. A 60 GHz CMOS VCO using on-chip resonator with embedded artificial dielectric for size, loss and noise reduction. In: Proceedings of IEEE International Solid-State Circuits Conference, Digest of Technical Papers, San Francisco, 2006. 1218–1227

6 Cheung T S D, Long J R, Vaed K, et al. On-chip interconnect for mm-wave applications using an all-copper technology and wavelength reduction. In: Proceedings of IEEE International Solid-State Circuits Conference, Digest of Technical Papers, San Francisco, 2003. 396–501

7 Cheung T S D, Long J R. Shielded passive devices for silicon-based monolithic microwave and millimeter-wave integrated circuits. IEEE J Solid-State Circ, 2006, 41: 1183–1200

8 LaRocca T, Tam S W, Huang D, et al. Millimeter-wave CMOS digital controlled artificial dielectric differential mode transmission lines for reconfigurable ICs. In: Proceedings of IEEE MTT-S International Microwave Symposium Digest, Atlanta, 2008. 181–184