Appendix A

Design Considerations: The DCO in this work uses the traditional LC-tank-based oscillator core with one cross-coupled pair to compensate the loss of the LC tank. The oscillation frequency is given by the equation (1):

$$f_{osc} = \frac{1}{2\pi\sqrt{LC}} \quad (1)$$

where L and C are the inductance and the capacitance in the LC tank, respectively. Here, all the parasitic capacitance is taken into C.

From (1), the oscillation frequency could be varied by tuning L or C. In this work, the LC tank in the DCO is segmented into three sections, including coarse tuning bank, medium tuning bank and fine tuning bank.

Assume that the capacitance of the LC tank is increased by ΔC, the oscillation frequency would be

$$f_{osc1} = f_{osc} - \Delta f = \frac{1}{2\pi\sqrt{L(C+\Delta C)}} \approx \frac{1}{2\pi\sqrt{LC}}(1-\frac{1}{2}\frac{\Delta C}{C}) \quad (2)$$

where it is assumed that ΔC is much smaller than C and Taylor series is used in the approximation. From (2), the oscillation frequency variation induced by the increased ΔC is

$$\Delta f \approx f_{osc} \bullet \frac{1}{2}\frac{\Delta C}{C} \quad (3)$$

Similarly, the oscillation frequency variation induced by the increased ΔL is

$$\Delta f \approx f_{osc} \bullet \frac{1}{2}\frac{\Delta L}{L} \quad (4)$$

It could be seen from the equations (3) and (4), the inductance variation or capacitance variation should be linearly dependent on the tuning bits if high tuning linearity is desired for the DCO, which is an important optimized goal during the implementation of the LC tank.

If the tuning frequency steps of the coarse, medium and fine tuning are Δf_{coa}, Δf_{med} and Δf_{fine}, then the tuning frequency range of the DCO is $\Delta f_{coa} \bullet N_{coa}$, where N_{coa} is the tuning bit number of the coarse tuning, and $\Delta f_{coa} < \Delta f_{med} * N_{med}$ and $\Delta f_{med} < \Delta f_{fine} * N_{fine}$ should be assured to avoid the blind frequency band over the whole tuning frequency range, where N_{med} and N_{fine} are the tuning bit numbers of the medium tuning and fine tuning, respectively. Since Δf_{fine} is also the achievable frequency resolution of the DCO, there is a trade-off between the frequency resolution and the tuning range under the fixed tuning bit numbers. Otherwise, more tuning bit numbers should be used.

The required capacitance/inductance variation step of the coarse, medium and fine tuning could be calculated from the equations (3) and (4) once Δf_{coa}, Δf_{med} and Δf_{fine} are known. Actually, some iterations are needed due to the complicated electrical characteristics of the LC tank and severe parasitics effects in mm-wave band.

Furthermore, the LC tank should maintain a high quality factor over the whole tuning range to keep good phase noise performance, based on Leeson phase noise model. In this work, the LC tank includes a lot of digitally-controlled switches to implement the tuning function. These switches should be optimized to minimize the effects of the digitally-controlled switches on the quality factor of the LC tank.

Appendix B

DiCAD Differential Transmission Line: The DiCAD transmission line (TL) was first introduced in [8] to change the effective dielectric constant which can reach a much greater permittivity than that of the silicon dioxide. The operation principle of the DiCAD is briefly explained here. Figure S1 shows the structure and equivalent circuit of the DiCAD differential transmission line (DTL). Some floating metal strip pairs are inserted into the silicon dioxide underneath the DTL.

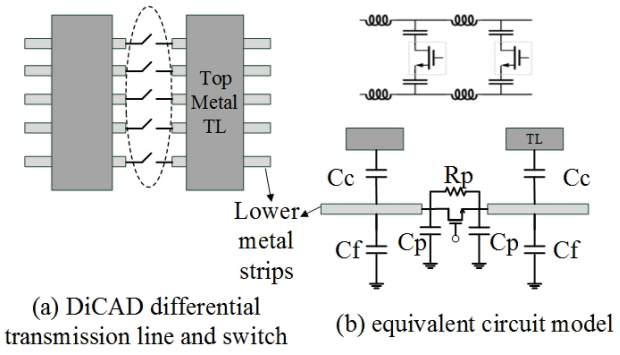

Figure S1 (a) DiCAD differential transmission line; (b) its equivalent circuit.

When the dielectric is placed in an external electric field (E), the electric dipole moment is induced in this dielectric material. The unit volume of the electric dipole moment is called polarization density (P). The polarization density (P) yields both the electric displacement field (D) and effective permittivity (ε_{eff}) via:

$$D = \varepsilon_o E + P = \varepsilon_{eff} E \tag{5}$$

The floating metal strip pairs, each of which is connected with the MOS switch, distribute homogeneously along the DTL. The MOS switches control the underneath strip pairs to be shorted or opened and the effective permittivity is changed as a result. Fig. 1(b) shows its equivalent circuit, where C_c represents the capacitance between the TL and the floating metal strips, C_f is the capacitance between the metal strips and the silicon substrate, C_p and R_p are the switch-off capacitance and switch-on resistance of the switch transistor. When the switch is turned on, the single-ended capacitance of the DiCAD DTL is given by $C_{short} = C_c$ and the quality-factor is given by (6). When the switch is turned off, the single-ended capacitance is given by (7).

$$Q_{short} = \frac{1}{\omega R_p C_c} \tag{6}$$

$$C_{open} = \frac{(C_f + C_p)C_c}{C_f + C_p + C_c} \tag{7}$$

So the tuning factor of the structure is:

$$C_{\max} / C_{\min} = \frac{C_f + C_p + C_c}{C_f + C_p} \tag{8}$$

C_c and C_f are fixed capacitance when the passive structure is settled. The trade-off between Q-factor and the tuning range is totally determined by the size of the MOSFET switches.

Appendix C

Digitally-Controlled Switches: The DiCAD DTL is controlled by the MOS switch network which is located in the midway along the floating metal strip pairs. The size of the MOS switches in the tuning tanks is quite crucial in the frequency up to 80 GHz since there is a trade-off between the tuning range and Q-factor of the DiCAD DTL.

Figure S2 shows two different implementations of the digitally-controlled switch. Three transistors are used in Figure S2(a) and M2 is the main switch while M1 and M3 are used to pull the source/drain nodes of M2 to the ground so that M2 is completely turned on when the control bit is logically high. When the control bit is logically low, the source/drain nodes of M2 are floating, which may affect the switch performance at off mode. One transistor M2 is used as the main switch in Figure S2(b) while two resistors and one inverter avoid the floating source/drain nodes of M2 so that M2 could be completely turned on or off to achieve better switch performance. As a comparison, the post-layout extractions show that the switch-on resistance R_p is 33.9Ω and the switch-off capacitance C_p is 10.9fF for the implementation of Figure S2(a) while the switch-on resistance R_p is 31.2Ω and the switch-off capacitance C_p is 9.0fF for the implementation of Figure S2(b), which shows that the implementation in Figure S2(b) is superior to the implementation in Figure S2(a). In this work, all the digitally-controlled switches use the implementation of Figure S2(b).

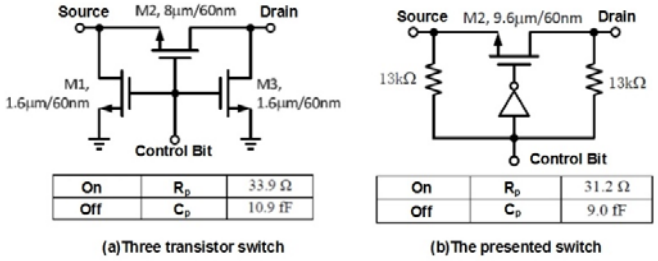

Figure S2 Two implementations of the digitally-controlled switch and extracted parasitics.

Appendix D

Measured Results: As shown in Figure S3, the measured phase noise of the DCO is –111.8dBc/Hz at 10-MHz offset (about -90dBc/Hz at 1-MHz offset) from an 81.16-GHz carrier frequency, corresponding to a FOM_T value of -175.3dBc/Hz and a FOM value of -184.0dBc/Hz, where FOM_T and FOM are given by (9) and (10). The phase noise at 10-MHz offset across the entire coarse tuning range is shown in Figure S4.

$$FOM_T = PN - 20\log_{10}(\frac{F_0}{\Delta f} \times \frac{FTR}{10}) + 10\log_{10}(\frac{P_{DC}}{1mW}) \quad (9)$$

$$FOM = PN - 20\log_{10}(\frac{F_0}{\Delta f}) + 10\log_{10}(\frac{P_{DC}}{1mW}) \quad (10)$$

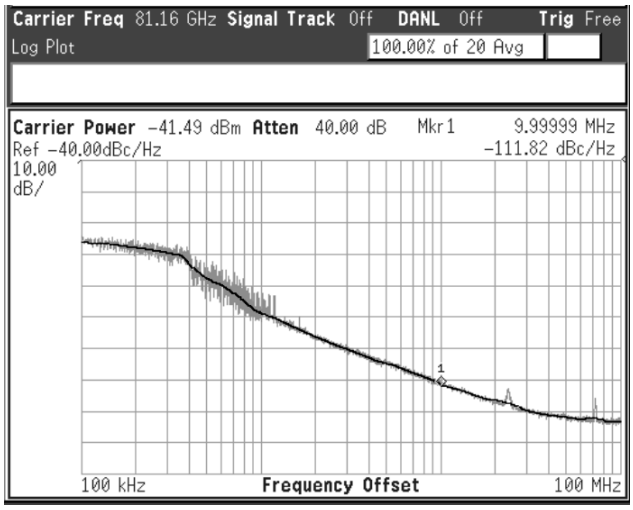

Figure S3 Measured phase noise of the DCO at 81 GHz

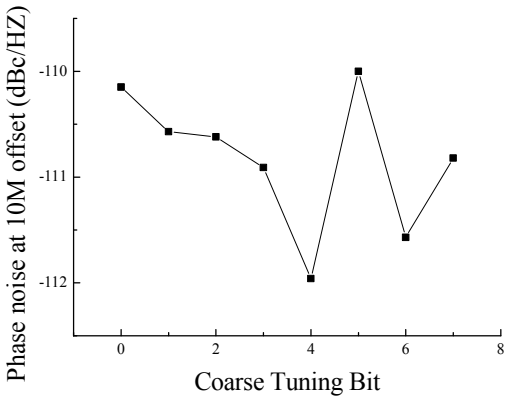

Figure S4 DCO phase noise at 10-MHz offset versus the coarse tuning codes.

The performance of the presented DCO is summarized and compared with the-state-of-the-art in Table I. Compared with others, the DCO in this work achieves a superior FOM of -184.0 dBc/Hz, better than [2] and [3, 4], and the presented DCO achieves the highest oscillation frequency.

TABLE I Performance Comparison of the DCOs above 50GHz

Ref.	F_0 (GHz)	FTR (%)	PN dBc/Hz	P_{DC} (mW)	FOM dBc/Hz	FOM_T dBc/Hz	CMOS
[1]	51.3-53.3	4	-116[1]	2.34	-187.2	−179.2	90 nm
[2]	58.27-63.83	9.3	−90.1	10.6	-175.5	−174.9	90nm
[3, 4]	56.22-62.16	10	−93	12	-177.9	−177.9	90nm
This work	80.23-83.02	3.7	-111.8[1]	4	-184.0	−175.3	65nm

[1] PN @ $\Delta f = 10$ MHz, the rest are at 1 MHz.