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Demonstration of 60 GHz millimeter-wave short-range wireless communication system at 3.5 Gbps over 5 m range

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Abstract Millimeter-wave communication has received considerable attention for use in new-generation broadband wireless communication because of the scarcity of microwave band spectrum resources. The unlicensed frequency band at 60 GHz is suitable for indoor short-range broadband communication. In this paper, we introduce a 60 GHz millimeter-wave short-range wireless communication demo system adhering to the IEEE 802.11ad standard and targeting high-definition video streaming transmission. The system uses single-carrier transmission with frequency-domain equalization. The hardware prototype consists of a 65-nm CMOS radio-frequency front-end and a baseband transceiver for the physical layer functions. Important baseband technologies such as carrier synchronization, phase noise compensation, frequency-domain equalization, and low-density parity-check decoding based on probability calculation are also discussed. The system performance is demonstrated in an experiment on high-definition video transmission, where a data rate of 3.52 Gbps is achieved with a quadrature phase-shift keying signal over a distance of 5.109 m.

Keywords 60 GHz, millimeter-wave, IEEE 802.11ad, SC-FDE, 65-nm CMOS

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1 Introduction

Mobile data traffic is experiencing unprecedented growth due to the increasing popularity of smart phones and other mobile devices such as netbooks and smart tablets [1]. To meet this challenging demand, the capacity of wireless links needs to be enhanced. Although technologies such as cognitive radio and multi-antenna technology are developed to enhance the spectrum efficiency, they may not be sufficient to meet future traffic demand. As a result, increasing the available spectrum is a promising solution.

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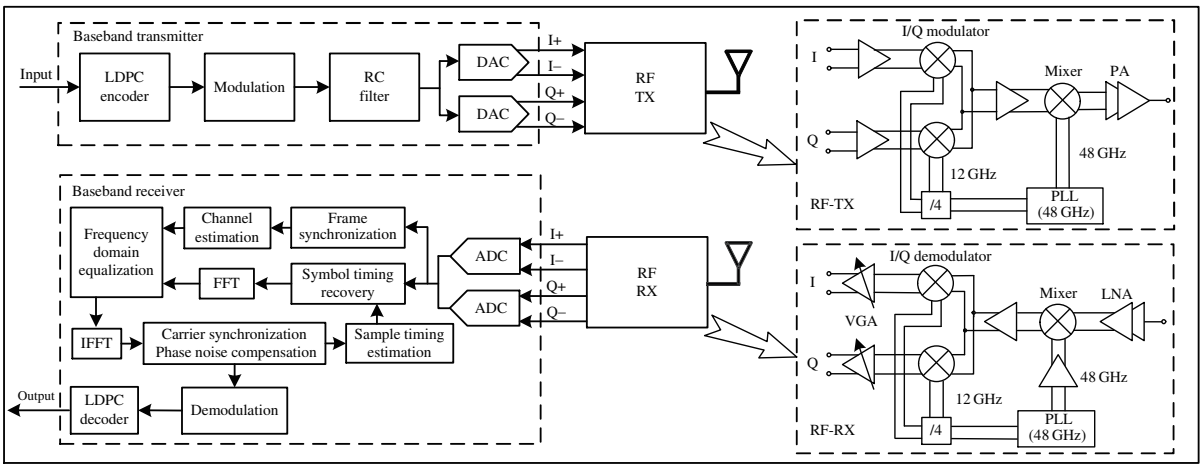


Figure 1 Block diagram of 60 GHz millimeter-wave communication system.

However, the sub-3 GHz microwave band spectrum is becoming increasingly crowded. On the other hand, vast amounts of band resources remain underutilized in the millimeter-wave band (30 to 300 GHz), making it attractive for high-data-rate communication. In particular, the 60 GHz band, where a 5–7 GHz unlicensed band resource is located, is a promising candidate. Compared to the band resources at lower frequencies, the 60 GHz band has higher path loss and oxygen absorption, making it more suitable for short-range broadband communication [2]. Rapid progress in the development of CMOS radio frequency (RF) integrated circuits paves the way to low-cost implementation of millimeter-wave systems. Regarding standardization, several standards have already been developed for indoor wireless personal area networks or wireless local area networks, such as IEEE 802.15.3c [3], ECMA-387 [4], and IEEE 802.11ad [5]. In future 5G mobile communications, millimeter-wave communications will also be an important element in providing multigigabit communication services.

The literature [6–9] report 60 GHz wireless communication systems in different scenarios. A fully integrated 60 GHz CMOS transceiver chipset for mobile communication is reported in [6]. The chipset achieves 1.8 Gbps for transmission up to 40 cm and 1.5 Gbps up to 1 m. A 60 GHz short-range wireless file transfer system supporting 2 Gbps throughput is implemented in [7].

In this paper, a 60 GHz millimeter-wave short-range wireless communication demo system based on the IEEE 802.11ad standard is presented. The single-carrier transmission with the frequency-domain equalization (SC-FDE) scheme is adopted for transmission. The RF front-ends use a dual-conversion architecture implemented in a 65 nm CMOS process. Advanced signal processing technologies such as carrier synchronization, phase noise compensation, overlap-cut fractionally spaced equalization, and low-density parity-check (LDPC) decoding based on probability calculation are developed and implemented in the baseband circuits to enhance the overall system performance.

2 System architecture

Figure 1 shows the system block diagram, including the RF front-ends and baseband transceivers. The RF front-ends employ a dual-conversion architecture. In the RF transmitter (RF-TX), the differential in-phase (I) and quadrature (Q) signals are first up-converted to the 12 GHz intermediate frequency (IF) by the quadrature modulator and then up-converted again by a 48 GHz mixer to the 60 GHz frequency band. The 60 GHz RF signal is amplified by a multistage power amplifier (PA). In the RF receiver (RF-RX), the 60 GHz signal is first amplified by a low-noise amplifier (LNA). The output signal is then down-converted to the 12 GHz IF band and fed to the IF I/Q demodulator. The IF signal is demodulated to a differential I/Q baseband signal, which is later amplified by a variable gain amplifier (VGA).

We adopt the SC frame structure defined by the IEEE 802.11ad standard, which is depicted in Figure 2. In the transmitter baseband, the user data are encoded by the LDPC encoder and then mapped to

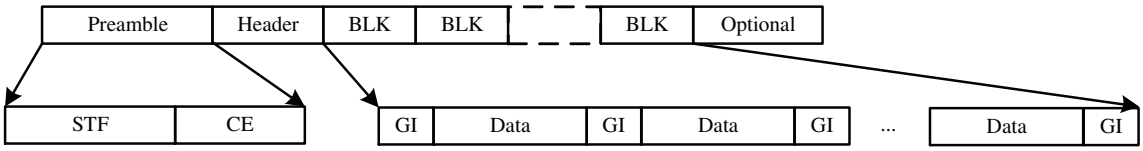


Figure 2 IEEE 802.11ad SC-physical layer (PHY) frame.

Table 1 Summary of the PHY parameters

Parameter	Value or description
Constellation	QPSK
Coding scheme	LDPC (R=1/2)
System rate	1.76 Gbps
Roll-off factor of RC filter	0.23
Bandwidth	2.16 GHz
ADC/DAC sampling	3.52 GHz
Number of FFT points	256

quadrature phase-shift keying (QPSK) symbols. Next, the Golay preamble and the header section are catenated. The signal frame is filtered by a raised cosine (RC) filter with a 2.16 GHz bandwidth spectral mask and split into the in-phase and quadrature branches, which are sent to digital-to-analog converters (DACs) and transmitted by the RF front-end. In the receiver baseband, the differential I/Q analog signals are converted to digital signals by time-interleaved analog-to-digital converters (ADCs). Each ADC consists of four parallel-channel ADCs with an 880 MHz sampling clock. The received signal is then sent to the frame synchronization module to estimate the starting position of the PHY frame by searching for the correlation peak of the Golay sequences. The symbol timing recovery module then compensates for the sampling offset. The overlap-cut fractionally spaced equalizer is used for frequency-domain equalization. The coefficients are estimated using the channel estimation sequences, which consist of Golay sequences that have good auto-correlation. In a conventional receiver, the carrier synchronization is processed after the ADC sampling. However, owing to the high phase noise level in 60 GHz millimeter-wave systems, the traditional carrier synchronization algorithms cannot work effectively. Therefore, we use open-loop phase compensation to resolve the carrier synchronization problem under severe phase noise. The user data are obtained from the compensated signal after it is demapped and decoded by the LDPC decoder. To reduce the computational complexity and power consumption, the LDPC decoder is implemented using probability calculation. The PHY parameters are summarized in Table 1.

3 Key technologies of baseband signal processing

3.1 Frequency-domain equalization: overlap-cut fractionally spaced equalization

Conventional equalization algorithms for wireless communications are based on symbol-spaced sampling. However, symbol-spaced equalizers are sensitive to the sampling timing error. To reduce the required timing recovery, a fractionally spaced equalizer is used in the system demo to eliminate intersymbol interference. The fractionally spaced equalizer has a higher sampling rate than the symbol-spaced equalizer. Hence, it is more robust to the timing error. In our system, the ADC sampling rate is 3.52 GHz, which is twice the symbol rate.

To perform frequency-domain equalization, the conventional SC-FDE system inserts a cyclic prefix (CP) to ensure that the convolution of the transmit signal block and the channel is circular. However, CP insertion reduces the transmission throughput. In contrast, overlap-cut processing requires no CP insertion. It has been shown that overlap-cut processing provides higher throughput than CP insertion, at the cost of increased complexity [10]. Overlap-cut processing in SC-FDE is illustrated in Figure 3. In our system demo, frequency-domain equalization is implemented using minimum mean square error equalization with a 256-point Fast Fourier Transform (FFT) length and 50% overlap window.

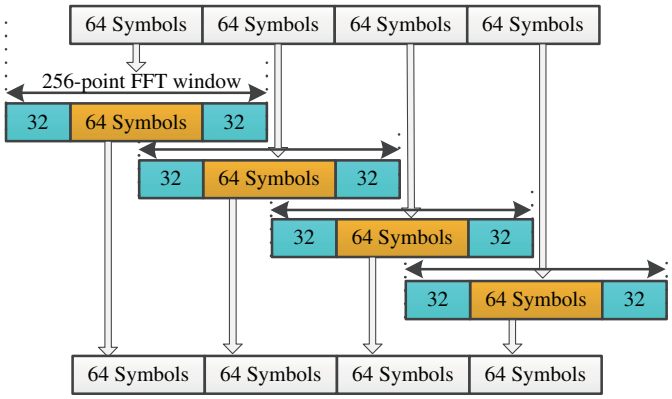


Figure 3 (Color online) Overlap-cut processing in SC-FDE [11] @Copyright 2014 IEEE.

3.2 Carrier synchronization and phase noise compensation

Because of temperature changes in the crystal oscillator, the carrier frequency drifts with time. Hence, there is a frequency difference between the local oscillator (LO) of the transmitter and that of the receiver, which is called the carrier frequency offset. This offset causes phase rotation with time in the constellation diagram of the received signal. Further, the random phase noise caused by the voltage-controlled oscillator and phase-locked loop (PLL) also introduces a random phase shift. Because both the carrier frequency offset and phase noise contribute to the phase error, we can compensate for them simultaneously by adjusting the phase of the received signal.

The phase shift is estimated through the guard interval (GI) sequence in the data block. Open-loop compensation is then performed on the basis of the estimated value. By applying the compensation algorithm, we successfully resolve the carrier synchronization problem under severe phase noise in the 60 GHz millimeter-wave communication system.

3.3 Channel coding: LDPC decoder based on probability calculation

Probability calculation is a method of designing low-precision digital circuits in which the probability messages are represented by streams of stochastic bits. In the bit streams, the probability message is encoded by changing the number of "1" bits. Hence, the probability of a given bit in the bit stream being "1" is equal to the value of the probability message. Thus, very simple circuits can be used for the probability calculations.

In our demonstration system, the LDPC decoder is implemented using probability calculation. The nature of the decoding algorithm is analogous to that of the well-known sum-product algorithm (SPA). The SPA is a message passing algorithm in which two types of processing nodes, known as the variable nodes and parity-check nodes, iteratively exchange their beliefs (in the form of probability messages) about the correctness of the symbols received from the channel. However, for the LDPC decoder based on probability calculation, a probability message is represented by a stream of stochastic bits rather than a specific value in the iteration process. Because of its bit-serial nature, the probability calculation significantly reduces the hardware complexity and power consumption of the LDPC decoder.

4 Hardware prototype and measurement results

The 60 GHz RF front-end hardware prototype is shown in Figure 4. An RF chip 3 mm $\times$ 3 mm in size is mounted on a printed circuit board with a 10-dBi-gain on-board antenna.

The RF transmitter is composed of a 12 GHz I/Q quadrature modulator (IQM), a 48 GHz up-conversion mixer (UM), and a PA. The RF receiver consists of an LNA, a 48 GHz down-conversion mixer (DM), a 12 GHz I/Q demodulator (IQDM), and an I/Q baseband VGA. The 48 GHz LO signal is provided by an

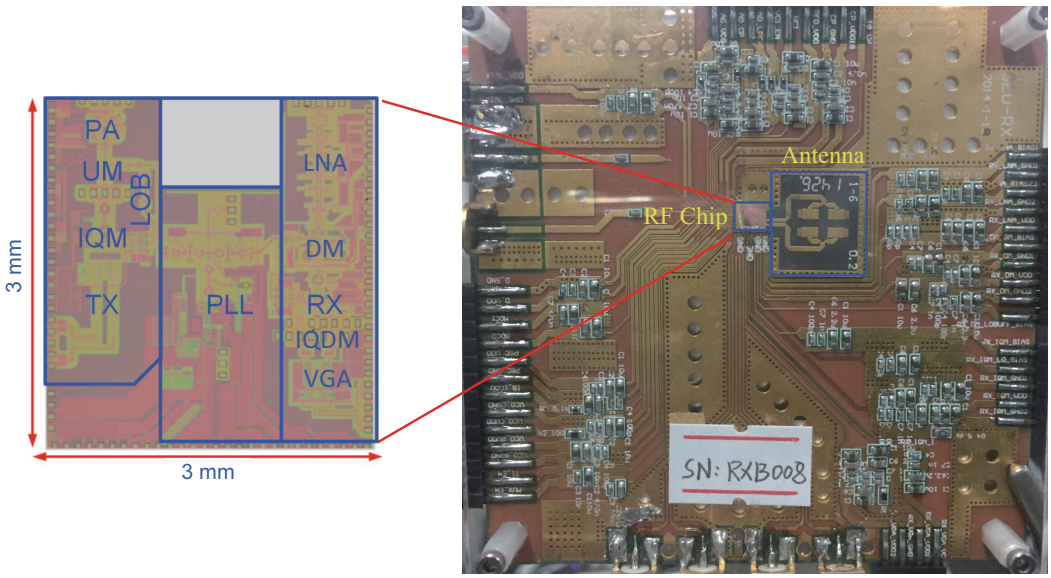
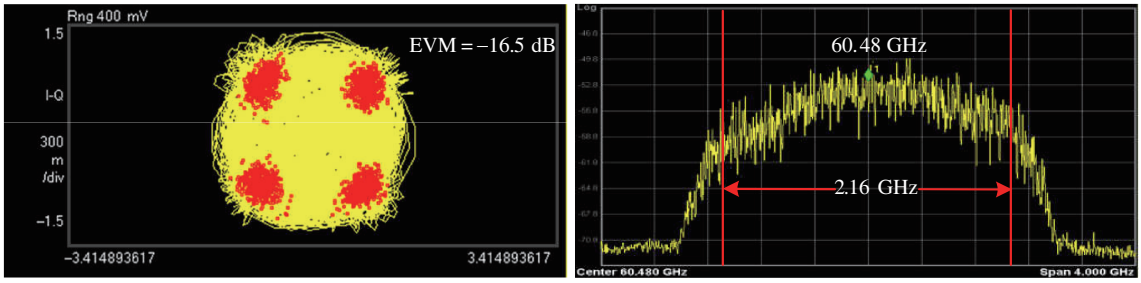


Figure 4 (Color online) 60 GHz RF front-end.



(a) (b)

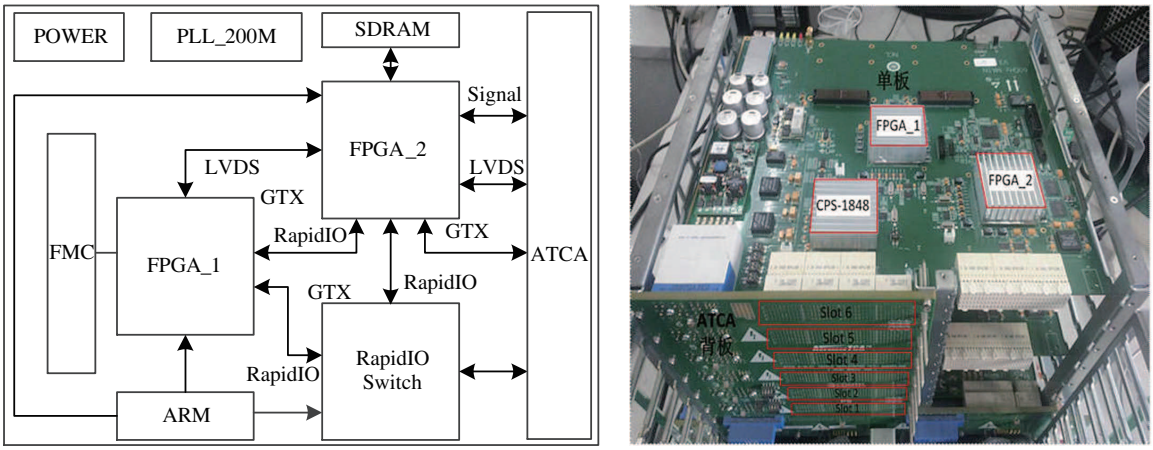
Figure 5 (Color online) RF front-end measurement results. (a) RF signal spectrum; (b) constellation graph.

external source and is divided into two paths; one path drives the RF mixer, and the other is sent to a divide-by-4 static frequency divider.

The performance of the RF front-end is measured using an arbitrary waveform generator to generate a QPSK baseband waveform with a 3.52 Gbps data rate. The transmission distance for measuring is set to 6 m. The measurement results in Figure 5 show that the carrier frequency is 60.48 GHz, and the 3 dB signal bandwidth is 2.16 GHz. The measured error vector magnitude (EVM) is −16.5 dB.

The baseband transceiver for the PHY function is implemented on a high-speed baseband signal processing platform. The user data are transmitted to the PHY layer through a high-speed Ethernet interface. The platform employs 16-path parallel signal processing with a 220 MHz system clock to satisfy the requirement of high-speed baseband signal processing. The baseband platform architecture and hardware prototype are shown in Figure 6. The hardware prototype is composed of two field-programmable gate array (FPGA) chips and an ARM chip.

A photograph of our high-definition video transmission system is shown in Figure 7. The demonstration system is tested in an indoor environment. The transmitted data are generated from a 3D high-definition video signal, which is taken by an eight-viewpoint video camera array and glasses-free 3D camera calibration system. After it is received by the 60 GHz wireless receiver, the decoded 3D high-definition video signal is displayed by a glasses-free 3D TV. The distance between the receiver and the transmitter is 5.109 m, and the data rate can reach as high as 3.52 Gbps with QPSK modulation. The packet loss for transmission is lower than 2%, which allows smooth high-definition video play.



(a) (b)

Figure 6 (Color online) High-speed baseband processing platform. (a) Platform architecture; (b) hardware prototype. (Acronyms: Advanced Telecom Computing (ATCA), FPGA Mezzanine Card (FMC), Low-Voltage Differential Signaling (LVDS))

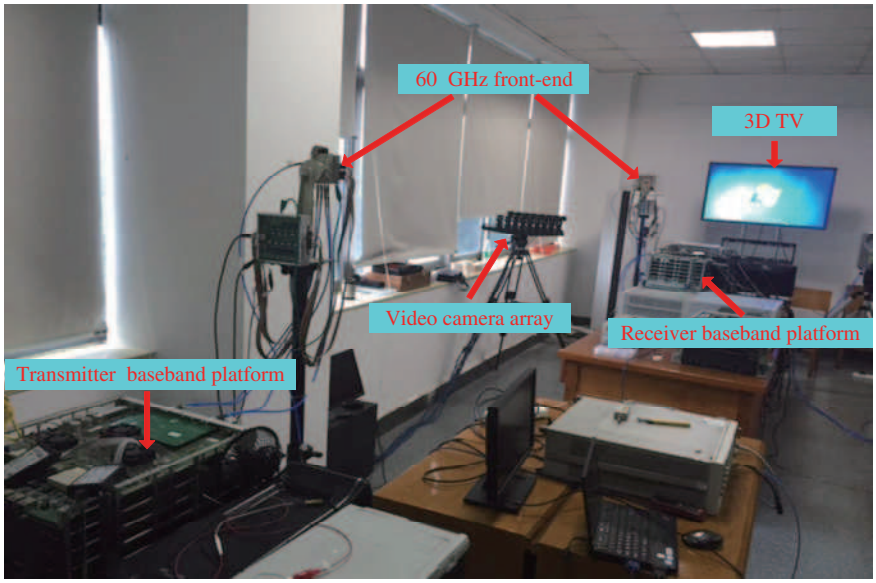


Figure 7 (Color online) High-definition video streaming transmission demonstration system.

5 Conclusion

In this paper, we introduced a 60 GHz wireless demonstration system. The key technologies, including carrier synchronization, phase noise compensation, frequency-domain equalization, and low-complexity LDPC decoding, were discussed. The demonstration system was tested by connecting it to a 3D video source and measuring the data rate. The results show that the demonstration system supports a 3.52 Gbps data rate over a distance of 5.109 m.

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Conflict of interest The authors declare that they have no conflict of interest.

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