60GHz Millimeter-Wave Short-Range Wireless Communication System Demonstration at 3.5Gbps over 5m Range

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- Introduction
- System Architecture
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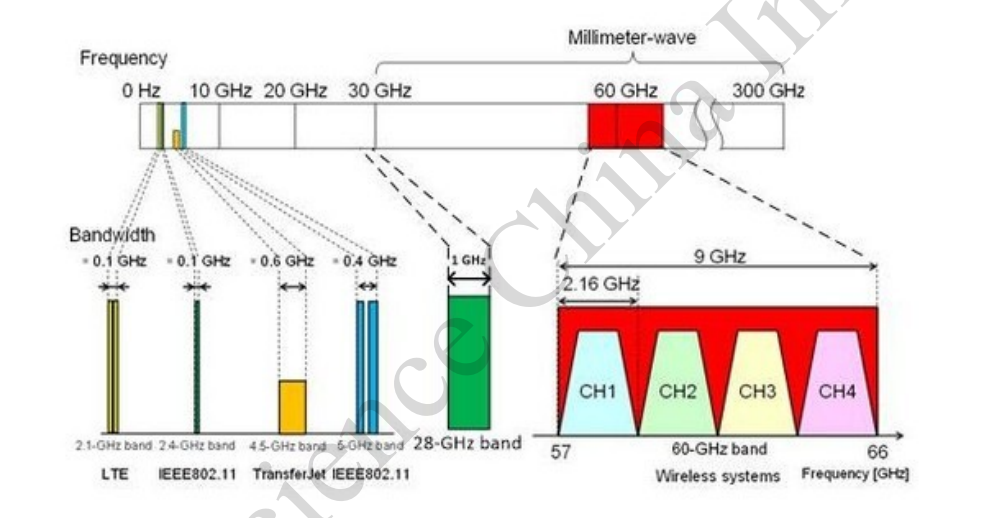
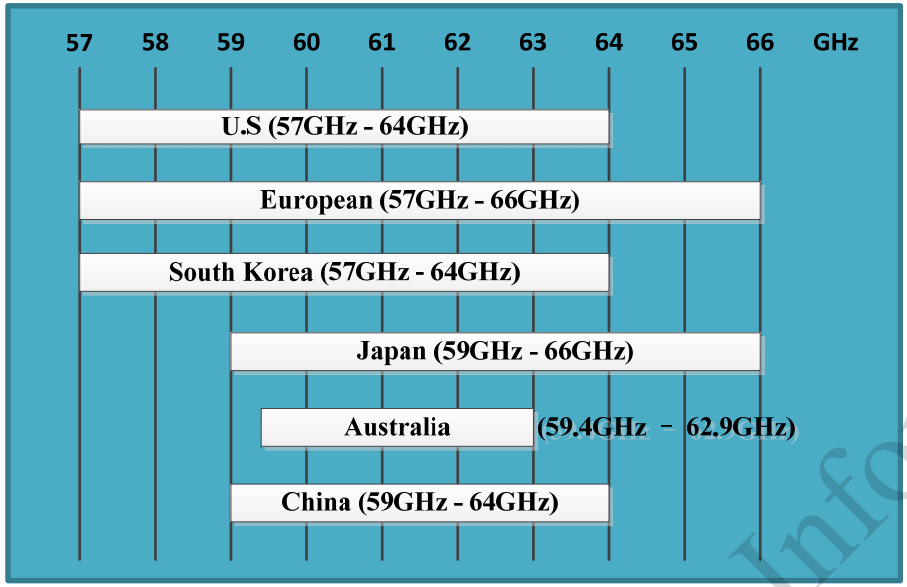
- Hardware Prototype and Measurement Results
- Conclusion

Introduction



- Sub-3GHz microwave band spectrum **crowded**
- 30GHz-300GHz millimeter-wave band **underutilized**

Introduction



- Large amounts of bandwidth
- License–free spectrum
- Security
- High level of chip integration circuits
- High path loss and oxygen absorption

IEEE802.15.3c

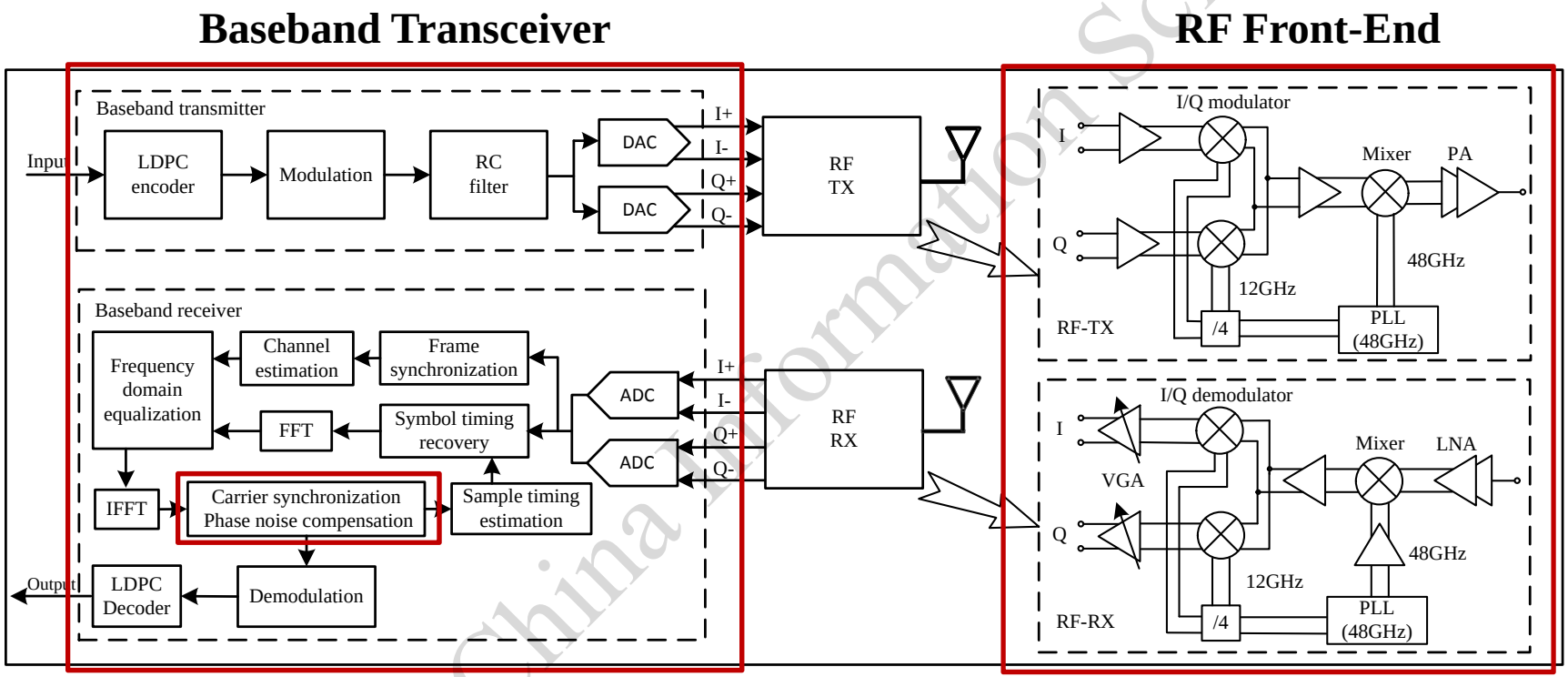
ECMA-387

IEEE802.11ad

60GHz millimeter-wave short-range wireless communication system demonstration for high-definition video transmission.

System Architecture

Baseband Transceiver + RF Front-End



Standard: IEEE802.11ad

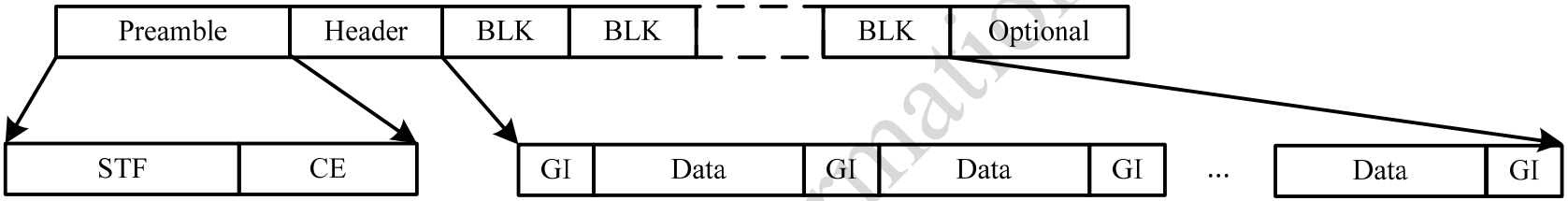
System scheme: single-carrier transmission with frequency-domain equalization(SC-FDE)

RF front-end architecture: dual-conversion(intermediate frequency-12GHz)

System Architecture

IEEE802.11ad SC-PHY Frame

Short Training Field(STF) + Channel Estimation Field(CE) + Header + Data Block + Optional Field.



STF: 16 $Ga_{128}(n)$ and 1$-Ga_{128}(n)$ Golay sequences.

CE: $Gu_{512}(n)$ + $Gv_{512}(n)$ + $Gv_{128}(n)$ Golay sequences.

$$Gu_{512} = [-Gb_{128} \quad -Ga_{128} \quad Gb_{128} \quad -Ga_{128}]$$
$$Gv_{512} = [-Gb_{128} \quad Ga_{128} \quad -Gb_{128} \quad -Ga_{128}]$$
$$Gv_{128} = -Gb_{128}$$

Header: 64bit.

Data Block: 448bit data symbol + Guard Interval($Ga_{64}(n)$).

In the 60GHz millimeter-wave communication system, there are 2304 data blocks in a SC-PHY frame.

System Architecture

Summary of the PHY Parameters

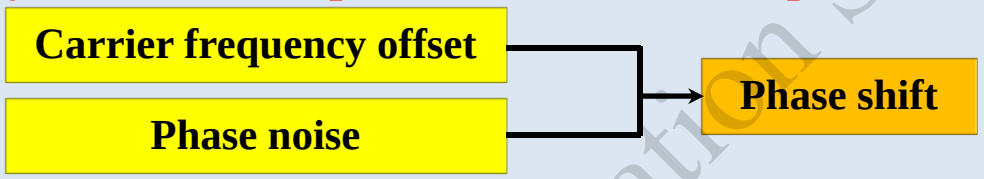
Constellation	QPSK
Coding scheme	LDPC(R=1/2)
System rate	1.76Gbps
Roll-off factor of raised-cosine filter	0.23
Bandwidth	2.16GHz
ADC/DAC sampling	3.52GHz
Number of FFT points	256

- The code rate of the LDPC encoder is 0.5.
- 2 times ADC sampling rate.
- The ADC consists of 4 parallel channel ADC with 880MHz sampling clock.

Baseband Key Technologies

Carrier synchronization and phase noise compensation

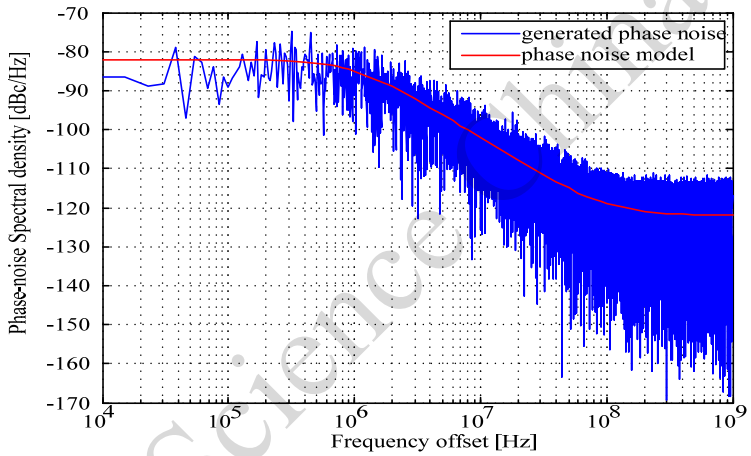
Problem: carrier synchronization problem under severe phase noise

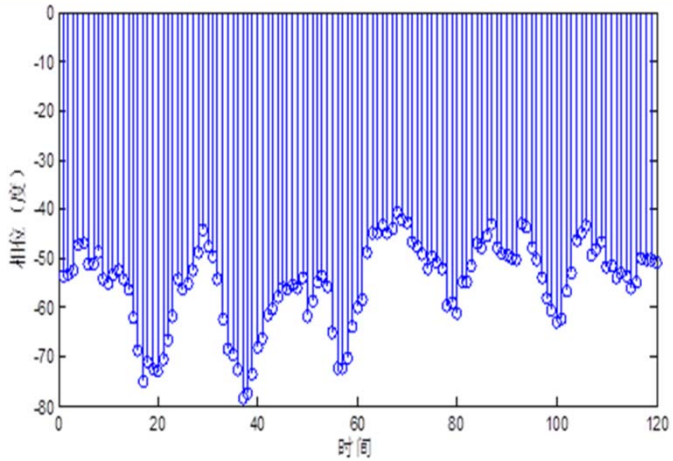


Carrier frequency offset-The changing in the temperature of the crystal oscillator.
Phase noise-The random phase noise caused by the VCO and the PLL.

Solution: open-loop phase compensation

The phase shift is estimated through the guard interval (GI) sequence in the data block. The open-loop compensation is then performed based on the estimated value.





Baseband Key Technologies

Overlap-cut fractionally spaced equalization

Problem: timing recovery and channel equalization

- Conventional symbol-spaced equalizer is sensitive to the sampling timing error.
- The conventional SC-FDE system inserts cyclic prefix (CP) to ensure that the convolution of the transmit signal block and the channel is circular. The CP insertion reduces the transmission throughput.

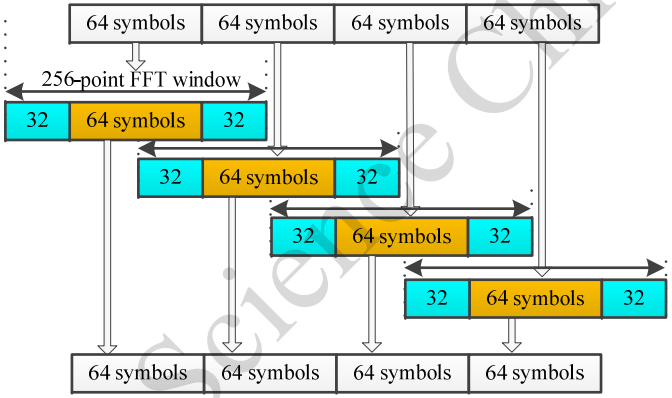
Solution: fractionally spaced equalization and overlap-cut processing

- **Fractionally spaced equalization**

The fractionally spaced equalizer sampling rate is greater than the symbol-spaced equalizer. In our system, the ADC sampling rate is 3.52GHz.

- **Overlap-cut processing**

Overlap-cut processing requires no CP insertion.



- ✓ minimum mean square error (MMSE) equalization.
- ✓ 256 points FFT length.
- ✓ 50% overlap window.

Baseband Key Technologies

LDPC decoder based on probability calculation

Probability calculation: the probability messages are encoded into streams of stochastic bits in a sense that the probability of observing a "1" in a stream is equal to the encoded probability. Probabilities can be manipulated using very simple circuits.

LDPC decoder based on probability calculation

Nature: sum-product algorithm(SPA)

The SPA is a message passing algorithm in which two types of processing nodes, known as the variable nodes (VNs) and the parity-check nodes (PNs), iteratively exchange their beliefs (in the form of probability messages) about the correctness of the symbols received from the channel.

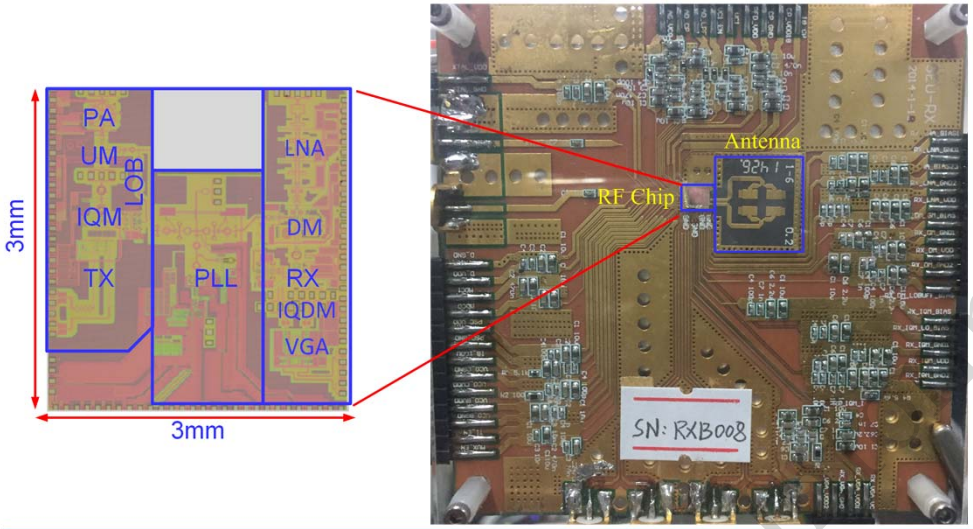
Difference

A probability message is represented by a stream of stochastic bits rather than a specific value in the iteration process.

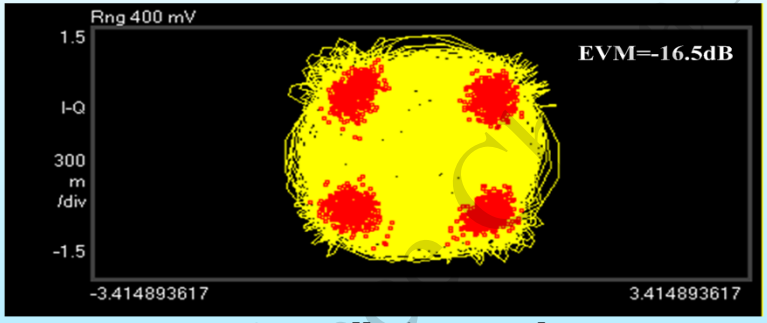
Reduce the hardware complexity and power consumption.

Hardware Prototype and Measurement Results

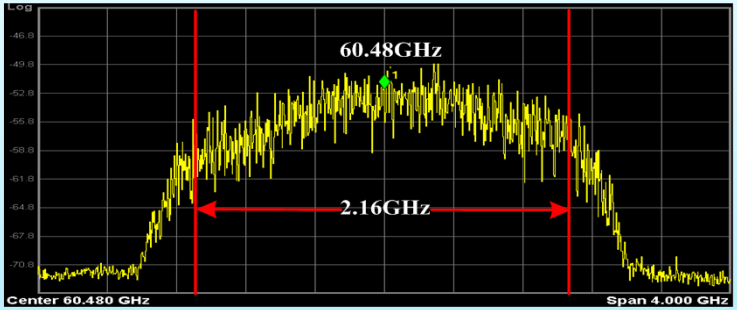
RF Front-End



- Chip size: $3mm \times 3mm$.
- 10 dBi gain on-board antenna.
- 65nm CMOS process.



Constellation graph



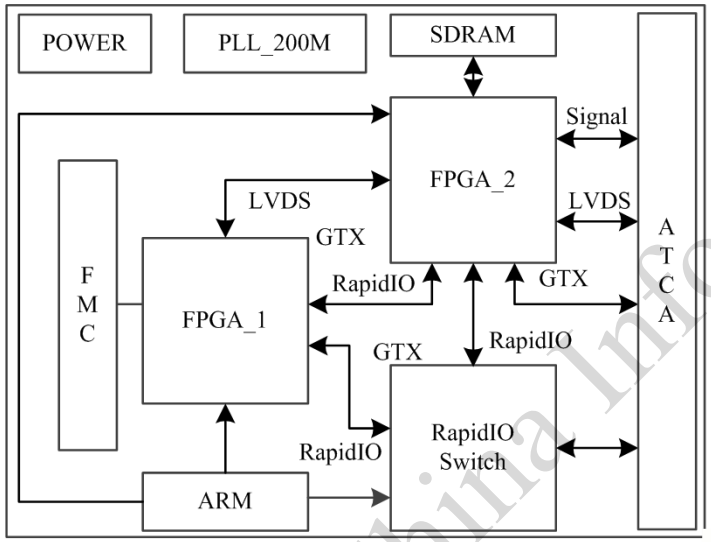
RF signal spectrum

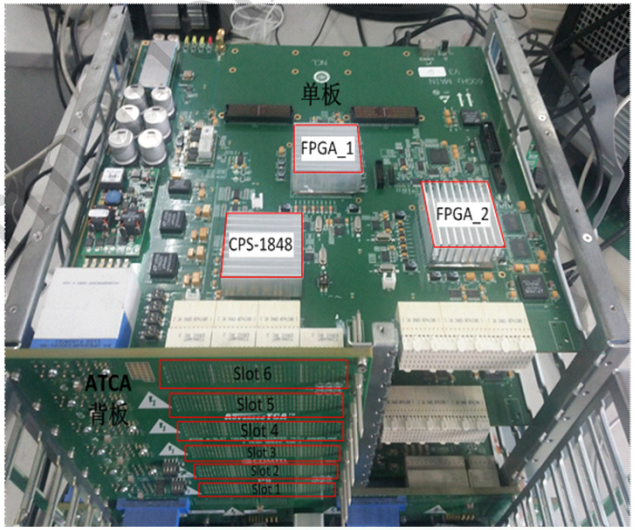
Test conditions: QPSK baseband signal with 3.52Gbps data rate, distance 6m.
Results: carrier frequency 60.48GHz, 3dB bandwidth 2.16GHz, EVM -16.5dB.

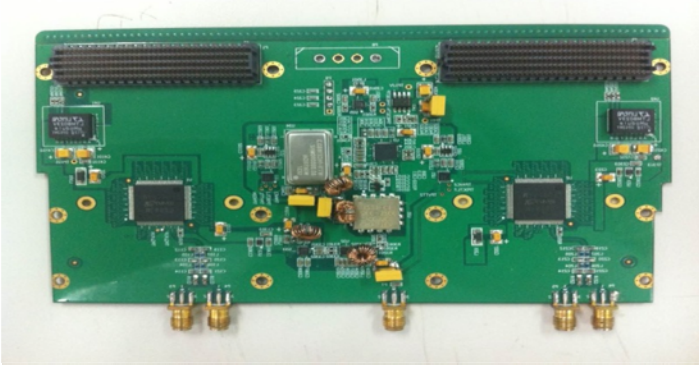
Hardware Prototype and Measurement Results

High speed baseband signal processing platform

- 16-path parallel signal processing with a 220MHz system clock.
- 2 FPGA chips and an ARM chip.

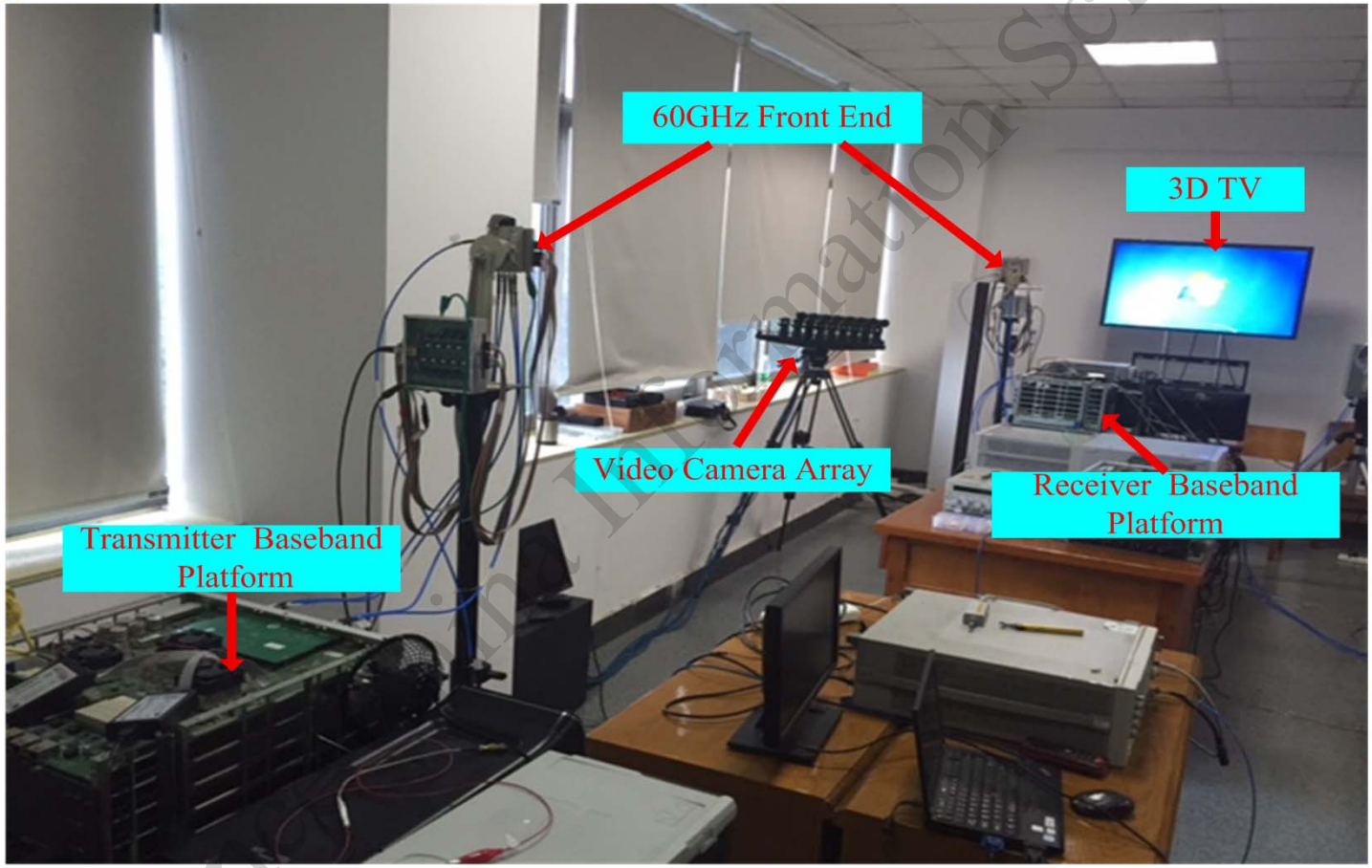






Hardware Prototype and Measurement Results

3D high-definition video demonstration system



Test conditions: 3D high-definition video signal with 3.52Gbps data rate, distance 5.109m.
Results: 2% packet loss, high-definition video play smoothly.

Conclusion

- A 60GHz millimeter-wave short-range wireless communication system adhering to IEEE802.11ad standard and targeting high-definition video streaming transmission.
- The hardware prototype consists of the RF front-end and the baseband transceiver.
- The RF front-end chip size is $3mm \times 3mm$ implemented in 65nm CMOS process.
- The demonstration system was tested by connecting it with a 3D video source. It supports 3.52Gbps data rate in 5.109m distance.
- The key baseband technologies, including the carrier synchronization, phase noise compensation, frequency-domain equalization and low-complexity LDPC decoder, were discussed.