SCIENCE CHINA
Information Sciences

• RESEARCH PAPER •
Special Focus on Millimeter Wave Communications Techniques and Devices for 5G

August 2017, Vol. 60 080303:1–080303:12
doi: 10.1007/s11432-016-9102-0

45-GHz and 60-GHz 90 nm CMOS power amplifiers with a fully symmetrical 8-way transformer power combiner

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Received March 14, 2017; accepted April 12, 2017; published online June 30, 2017

Abstract In this paper, 45 GHz and 60 GHz power amplifiers (PAs) with high output power have been successfully designed by using 90 nm CMOS process. The 45 GHz (60 GHz) PA consists of two (four) differential stages. The sizes of transistors have been designed in an appropriate way so as to trade-off gain, efficiency and stability. Due to limited supply voltage and low breakdown voltage of CMOS MOSFET compared with the traditional III-V technologies, the technique of power combining has been applied to achieve a high output power. In particular, a novel 8-way distributed active transformer power combiner has been proposed for realizing such mm-wave PA. The proposed transformer combiner with a fully symmetrical layout can improve its input impedance balance at mm-wave frequency regime significantly. Taking its advantages of this novel transformer based power combiner, our realized 45 GHz (60 GHz) mm-wave PA has achieved the gain of 20.3 dB (16.8 dB), the maximum PAE of 14.5% (13.4%) and the saturated output power of 21 dBm (21 dBm) with the 1.2 V supply voltage.

Keywords millimeter wave, power amplifier, CMOS, transformer power combiner, 45 GHz, 60 GHz

Citation Jiang Z D, Guo K Z, Huang P, et al. 45-GHz and 60-GHz 90 nm CMOS power amplifiers with a fully symmetrical 8-way transformer power combiner. Sci China Inf Sci, 2017, 60(8): 080303, doi: 10.1007/s11432-016-9102-0

1 Introduction

In millimeter-wave commercial applications, such as Gbps short-range wireless communication, automotive radar and radio imaging, CMOS technologies have attracted much attention from both industry and academia. It has the advantages of low cost in high volume production and SoC capability comparing with compound semiconductor GaAs or InP technology. The power amplifier (PA) is a key circuit block in a transmitter. However, this block is commonly implemented in expensive III-V technologies. The CMOS millimeter-wave PA faces many challenges including the low breakdown voltage and limited available gain of transistors, and significant loss of on-chip passive elements [1, 2].

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In recent years, many researches were carried out about millimeter-wave CMOS and HBT PA design [3–33]. In [3–8], parallel power combining was used in the PA design to achieve large output power. However, parallel power combining consumes large area which increases the cost. In [9], a dual-radial symmetric parallel power combining architecture was introduced to achieve compact and symmetric PA layout. In [10–14], stacked transistors were used to increase output voltage swing. However, a higher supply voltage may be needed and this might bring extra design complexity and cost. What is more, all of the stacked transistors based PA designs operate in frequency regime lower than V-band. In [15–28], transformer power combiner was used to achieve high output power and maintain high PAE without high voltage supplies. Because of the limited output voltage swing headroom, the low load resistance of the PA is required to achieve large output power without high voltage supplies. Transformer power combiner can maintain low loss when providing both large impedance-transformation ratio and multi-way power combining [34, 35]. Because of these advantages, multi-way power combining and low loss of a transformer power combiner, high output power and PAE can be achieved. In [15–20], the millimeter wave PAs using the transformer with two primaries for 4-way power combining were designed, whose output power was limited. In [21–25], the output ports of two 4-way transformer power combiners were parallel connected together to combine the output power. However, parallel connection not only doubles load impedance seen by the transformer but also limits the total transformation ratio and output power. In [26], another 4-way transformer power combiner was parallel connected but this design faced the same problem as those in [21–25]. In [27], a 60 GHz PA using 8-way transformer power combiner was proposed. However, in millimeter-wave frequencies regime, parasitic capacitance between the stacked primaries and secondary causes unbalanced voltage coupling between them. As a result, the differential input impedance of the four input ports are imbalanced and cannot provide optimal impedance to all the four differential amplifier stages. Therefore output power is limited and PAE is degraded. In this paper, a fully symmetrical 8-way transformer power combiner with uniform differential input impedance is proposed. 45 GHz and 60 GHz PAs using this 8-way power combiner were designed and fabricated in 90 nm RF CMOS technology.

Based on the authors' previous work presented in [28, 29], this paper further studies operation principle of our proposed 8-way mm-wave transformer combiner and design method of the 4-stage mm-wave PA in detail, with an extensive measured results provided for validation. It is organized as follows. Design and analysis of the proposed 8-way transformer power combiner is introduced in Section 2. Section 3 presents design of the 60 GHz PA. Section 4 shows and discusses measurement results of 45 GHz and 60 GHz PAs. Finally, conclusion is drawn in Section 5.

2 Design of fully differential 8-way mm-wave transformer power combiner

2.1 Comparison between different transformer power combining methods

To ensure reliability, supply voltage of PA must be limited below certain value. In 90 nm CMOS, DC voltage added to the drain of a common source PA should be 1.2 V [3]. While in 65 nm and 40 nm, it should be 1 V and 0.9 V [16, 23, 36]. Low supply voltage leads to limited output voltage swing. In this condition, AC current must be large to achieve large output power. Thus impedance matching network has to transform 50 Ω single-ended load or 100 Ω differential load to a low resistance value for output stage. Refs. [33, 34] showed that L-type impedance matching network with large impedance transforming ratio has high loss and degrades PAE and output power. The loss of transformer is mainly related to its Q factor and coupling coefficient. Thus transformer can provide large transforming ratio and maintain low loss. Transformer also consumes less chip area and provides virtual ground point for DC voltage connection. For all these reasons, transformer power combiner can achieve large output power with high peak PAE.

A transformer power combiner consists of series connected slab transformers, as shown in Figure 1. The transformer power combiner includes N primaries and a secondary coil. The voltage on the secondary of the transformer power combiner is the sum of the voltages on all the primaries. On the other hand, current in the secondary is identical with that in the primaries if all primaries carry the same current.

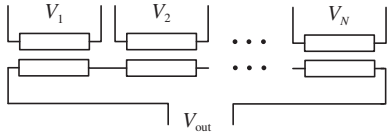


Figure 1 Transformer power combiner.

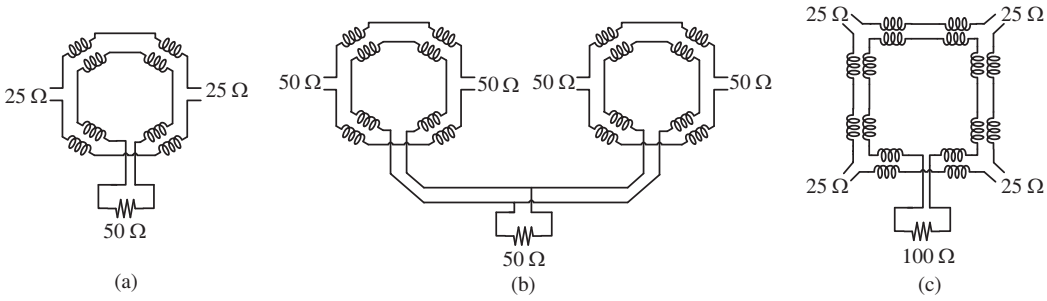


Figure 2 (a) 4-way transformer power combiner with two primaries; (b) parallel connected 4-way transformer power combiner; (c) 8-way transformer power combiner with four primaries.

Thus, a transformer power combiner can connect several PA cells together in series. When N PA cells are connected in series using a transformer power combiner with N primaries, the impedance seen by each PA cell is $1/N$ of the load impedance. It intuitively indicates that a transformer power combiner can provide larger impedance transformation ratio with more primaries. Figure 2 shows three types of transformer power combiner which are used in [15–28]. Figure 2(a) shows a 4-way transformer power combiner with two primaries. Figure 2(b) shows parallel connected 4-way transformer power combiner and Figure 2(c) shows an 8-way transformer power combiner with four primaries. The structure in Figure 2(a) and (b) can be matched to a single-ended 50 Ω load while the structure in Figure 2(c) can only be matched with differential 100 Ω [23, 27]. In Figure 2(a), the input impedance of the two input ports is 25 Ω according to the impedance transformation ratio. In Figure 2(b), input impedance of the four input ports is 50 Ω because parallel combining at the output terminal of the two transformer power combiner doubles the load impedance. With the same output voltage swing, the output power of the two power combiner in Figure 2(a) and (b) is the same. In Figure 2(c), input impedance of the four input ports is 25 Ω so that the output power is 3 dB higher than that in Figure 2(a) and (b) with the same output voltage swing. Loss of transformer is only related to its inductor quality factor and coupling coefficient [34, 35]. Thus, loss of the power combiner does not increase and the PAE is not degraded when the impedance transformation ratio increases with the number of the primaries. Additional matching network can be added before the power combiner in Figure 2(b) to compensate the impedance doubling effect, but this introduces some extra loss [21]. In conclusion, compared with transformer power combiner with two primaries, transformer power combiner with four primaries can deliver higher output power and does not degrade PAE.

Besides the former combing methods, parallel-series power combiners are proposed in [37, 38]. Compared with [37], the 4-way differential power combiner in [38] is improved at the low insertion loss and wide bandwidth mainly by using both metal-9 and aluminum as the primary winding of the series combiner and metal-10 as the secondary winding. However, this combiner is still not a completely symmetrical combiner. And the aluminum layer used in the circuits except for pads needs extra masks. It will increase the cost.

2.2 Challenges of the traditional 8-way transformer power combiner in millimeter wave frequency

In [27], a transformer power combiner with four primaries was firstly introduced to design a 60 GHz PA. The structure of the transformer power combiner in [27] is shown in Figure 3. The primary of the

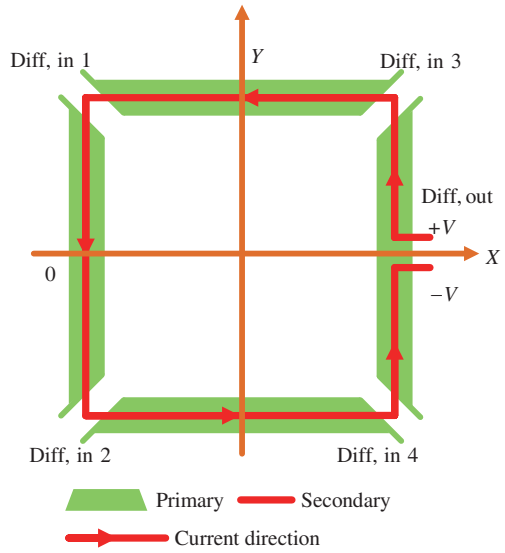


Figure 3 (Color online) Traditional transformer combiner.

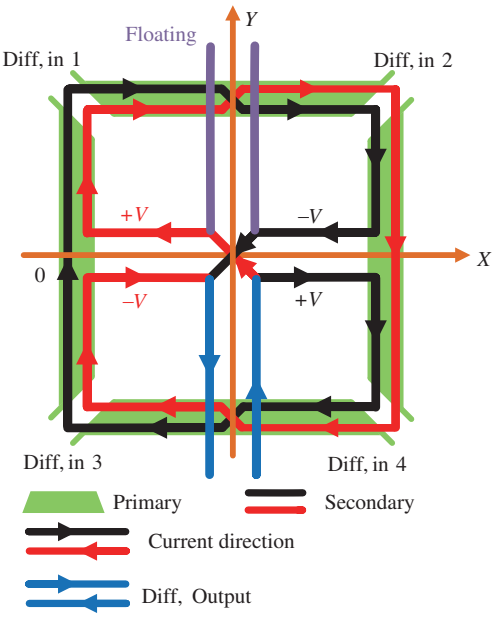


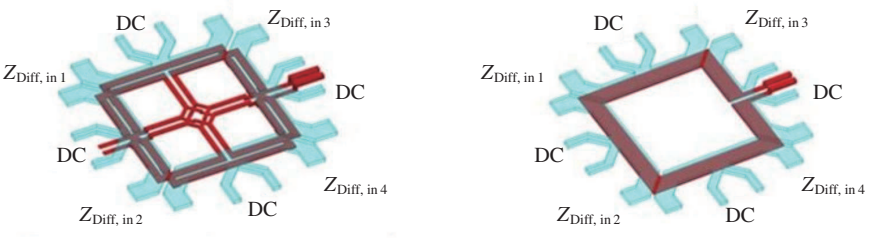
Figure 4 (Color online) Fully symmetrical 8-way transformer combiner.

transformer is stacked on the top of the secondary to increase coupling coefficient and reduce loss. The secondary voltage changes from V to 0 between the differential output terminals and the virtual AC ground as shown in Figure 3. Therefore, the voltage distribution on the secondary is not symmetrical to Y axis. Asymmetric voltage leads asymmetric coupling between primary and secondary. As a result, differential input impedances at the four differential input ports are asymmetric to Y axis. It means that differential input impedances at ports 1 and 2 are different with differential input impedances at ports 3 and 4. Although the difference of imaginary part of the input admittance in [27] is compensated by capacitance, the difference in real part is 40%. As a result, the output power and PAE is deteriorated.

2.3 Fully symmetrical 8-way transformer power combiner

The structure of the fully symmetrical power combiner is shown in Figure 4. The secondary consists of two parallel windings with identical structure but opposite direction. The current flows on two parallel windings to the same direction. Similar to the traditional transformer power combiner, the voltage on the secondary of this transformer power combiner is also unevenly distributed. However, the uneven voltage distributions on two identical windings become balanced when combined together. Thus, voltage coupling between primaries and secondary is symmetrical to the Y axis. The two parallel secondary windings connect together at the center of the transformer power combiner. The combined power goes from this center connection point to the output port through a differential transmission line. To make the transformer symmetric to the X axis, a floating dummy with the opposite direction is introduced to duplicate the coupling voltage between the secondary and the output differential line to maintain the symmetry about the X axis. The symmetry about both the X axis and Y axis leads to balance of the differential input impedance at four input ports.

Figure 5 shows the proposed fully symmetrical 8-way transformer power combiner and traditional 8-way power combiner. Simulated input impedances of the four input port in both transformer power combiners are also listed in the Figure 5. Primaries of the transformer are fabricated at the top metal layer with ultra-thick metal while the secondary is designed at one layer lower. DC supplies are applied at the center of each of four primaries which are able to be treated as the virtual AC ground. The length of a primary slab is 94 μm. The width of the primary winding and the secondary windings are 12 and 5 μm, respectively. The width and distance of the output differential line are both 3 μm. Simulation



$Z_{Diff, in 1}$	$Z_{Diff, in 2}$
10.45+j×12.49	10.73+j×12.89
$Z_{Diff, in 3}$	$Z_{Diff, in 4}$
11.14+j×13.21	11.14+j×13.2

$Z_{Diff, in 1}$	$Z_{Diff, in 2}$
12.39+j×19.17	12.7+j×19.23
$Z_{Diff, in 3}$	$Z_{Diff, in 4}$
2.11+j×12.78	2.37+j×12.4

Figure 5 (Color online) (a) Proposed fully symmetrical 8-way transformer combiner; (b) traditional 8-way transformer combiner.

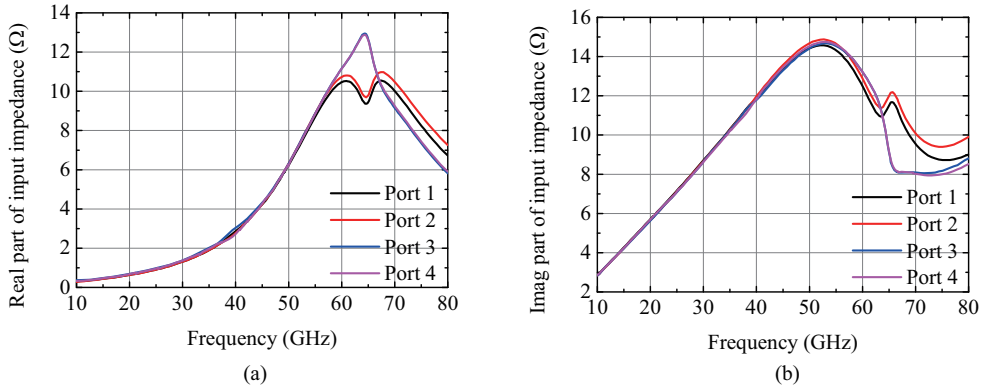


Figure 6 (Color online) (a) Real part of input impedance of fully symmetrical 8-way transformer power combiner; (b) imaginary part of input impedance of fully symmetrical 8-way transformer power combiner.

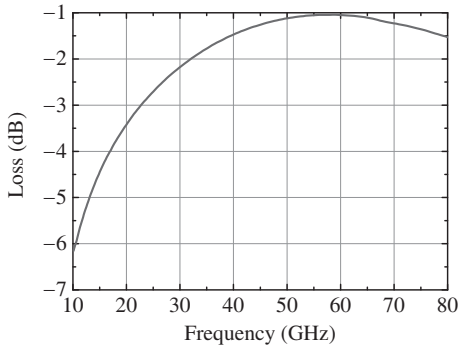


Figure 7 Loss of proposed fully symmetrical 8-way transformer power combiner.

results obtained from full wave EM solver demonstrate that the 100 Ω differential load is transformed to the optimal load impedance of the last power stage at 60 GHz. As shown in Figure 5, uniformities of the real and imaginary parts of four differential input impedances in the proposed transformer power combiner are better than 6% and 7%, respectively. Impedance imbalance is serious in the traditional transformer power combiner. Figures 6 and 7 shows simulated input impedances and loss of the proposed transformer power combiner from 10 GHz to 80 GHz. As shown in Figure 6, the proposed transformer power combiner can maintain impedance balance up to mm-wave frequency range. Figure 7 shows that loss in the transformer power combiner is about 1 dB at 60 GHz.

Table 1 Simulated maximum available gain of transistors at 60 GHz

FN × GW (μm)	76×1	38×2	29×2.62	19×4	15×5
G_{max} (dB)	5.78	6.87	7.13	7.42	5.77

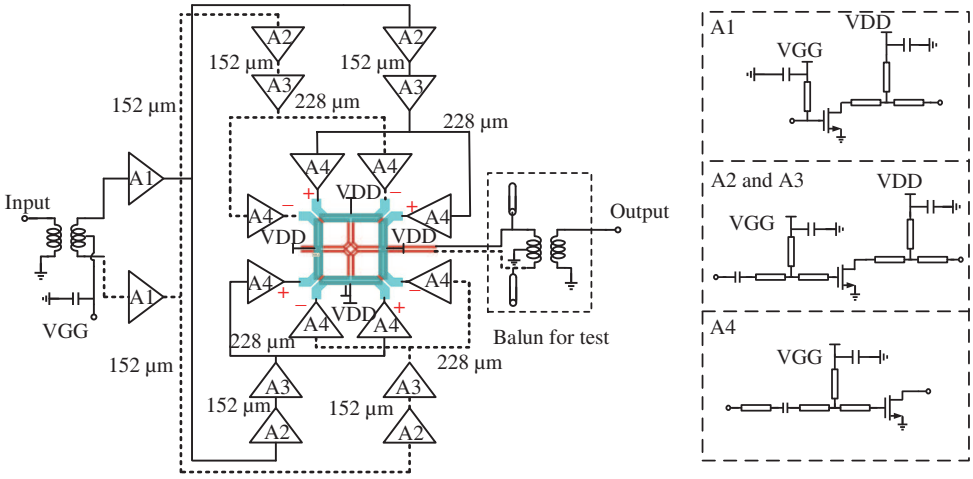


Figure 8 (Color online) Schematic of the proposed four-stage Class A power amplifier.

3 PA design

To design a multi-stage Class A or Class AB PA, sizes of transistors need to be carefully designed. Then schematic, matching network and DC supply of the proposed PA design is introduced. At last, the design of on-chip test Balun which is used for on-wafer differential circuit measurement is presented. The designing of the proposed 60 GHz PA is introduced as an example as the structures of the two PAs are similar.

3.1 Selection of width of transistors in the PA

Each common source (CS) amplifier stage in the PA consists of parallel PA cells. To determine gain of each stage, the gate width per finger and finger number of each PA cell are carefully chosen by thorough analysis. The gain of a transistor increases as its total gate width decreases. Small transistors mean that more parallel transistors are needed to achieve a certain output power. More parallel connected transistors bring the signal imbalance problem and larger parasitic inductance in PA cell interconnection. Thus, the gain of a transistor with a certain total gate width should be as large as possible to reduce the signal imbalance and parasitic inductance problem in the PA design.

For a certain total gate width, the different gate widths per finger and finger numbers can be selected. Table 1 shows the maximum available gain of transistors at 60 GHz with the same total gate width but different gate widths per finger and numbers of fingers. Therefore, the large total gate width is used to make sure that the transistor is always absolutely stable at 60 GHz. Table 1 shows that there is an optimum choice in selecting the finger number and gate width. The reason is that too many fingers or too large finger width will increase the total equivalent gate resistance.

In this PA design, the gate width and number of fingers of all the transistors are 4 μm and 19. This choice is made in consideration of the transistor gain, stability and PA cell signal balance. In all the PA stages, PA cells are comprised of this transistor, so the gain in each stage is similar.

3.2 Schematic of the four-stage PA

A four-stage 1.2 V class-A PA is designed using the proposed fully symmetrical 8-way transformer power combiner in 90 nm CMOS. The schematic of the PA is shown in Figure 8. The drain voltage is 1.2 V to insure the transistor reliability. The drain current density is designed to maintain the PA in a Class A operation. Four stages are selected to provide an enough gain. In Figure 8, Ai (i=1, 2, 3, 4) stands

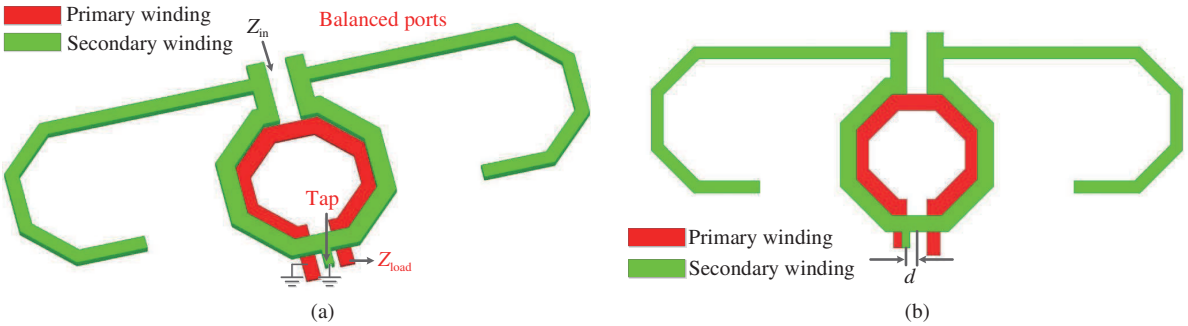


Figure 9 (Color online) (a) 3-D structure of the transformer balun; (b) top view of the transformer balun.

for each stage of the designed four-stage PA. The transformer power combiner provides the optimal load to the PA output stage. Therefore, no extra impedance transform network is needed at the input ports of the transformer. The last stage includes four differential CS amplifiers. In each differential CS amplifier, eight cells with the gate width of 228 μm per cell are used. The load impedance of every power stage is selected based on the output power consideration. The output port of the PA is differential so the circuit can be connected to a differential antenna. An on-chip balun is used to transform a 100 Ω differential load to a 50 Ω single-ended load for measurement. Inter-stage matching networks among A1–A4 are implemented by using transmission lines. The π-type matching network is used to provide both the optimum power load for transistors before it and conjugate match for the transistors after it. To transform single-ended signal to differential signal at the input port, a new balun is also used. Meanwhile, it provides the impedance matching for the first stage of the PA.

3.3 Power dividing and inter-stage matching network

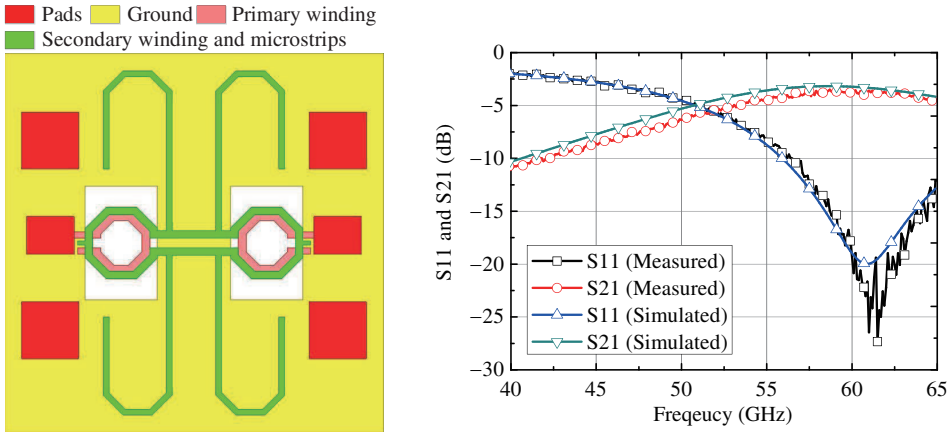
As shown in Figure 8, the inter-stage matching network also affects the power dividing. Four differential PA cells located at the four corners of the power combining transformer with the previous stage are difficult to connect together ensuring input signals delivered in phase. The Wilkinson power divider [27] and transformer [15, 31, 32] can be used in the power dividing network and inter-stage matching network. However, they consume large area or undergo difficulties in the layout.

The microstrip transmission line is implemented as the interstage matching network in the proposed PA because of its great flexibilities in the layout and moderate loss [39, 40]. For a microstrip transmission line with a length less than 1/8 wave length, its inductance can be simply estimated by using the equation $L = \beta l Z_0$ [41]. According to this equation, the microstrip transmission lines with different lengths can be used to realize the same inductance value by controlling the characteristic impedance Z_0. Thus, a complicate power dividing and impedance matching network with a compact layout can be easily realized. In addition, microstrip transmission lines can provide a well-defined current return path, which is critical to achieve a first pass silicon success. With these advantages, microstrip transmission lines are suitable to be used in the interstage matching network of a multistage PA with 8-way power combining transformer. The π-type matching network is used between each two cascade stages because it has the advantage of wide bandwidth and low loss [30].

The power and ground grids are applied in this design. VDD/GND/VGG planes are spread all around the layout through three different layers, i.e., metal layers 1–3. DC plane can act as reference ground plane of the microstrip transmission line.

3.4 Balun used for test purpose

The transformer balun is widely used in mm-wave circuit designs to achieve good amplitude and phase balance. Figure 9 shows the structure of the V-band transformer balun [42] with impedance transformation from single-ended 50 Ω to differential 100 Ω. The inner diameter of the primary winding and secondary winding are 65 and 88 μm, respectively. The width of the primary winding and the secondary



(a) (b)

Figure 10 (Color online) (a) Top view of the back-to-back structure; (b) the measured and EM simulated S parameters of the back-to-back.

windings are 12 and 6 μm, respectively. In order to reach the input differential impedance of 100 Ω, extra paralleled capacitances are applied. The paralleled capacitances are implemented by open microstrip stubs with the length of 423 μm each. Compared with the MIM capacitors, the open microstrip stub has a higher quality factor. The output balun can achieve a lower insertion loss with the open microstrip stub instead of the MIM capacitor. The second metal layer is used as the ground in this design. The area occupied by this balun is 150 μm×460 μm. Simulated phase and amplitude difference are 180.5° and 0.15 dB at 60 GHz.

4 Measurement results

4.1 Output balun measurement

Two identical baluns are laid out in a back-to-back structure. The top view of this structure is shown in Figure 10(a). It was measured using Agilent N5247A Network Analyzer and 100 μm pitch GSG (ground-signal-ground) probes. The measurement results agree well with the EM simulation results using a full wave solver as shown in Figure 10(b). According to measurement results, the insertion loss of this structure is 3.75 dB at 60 GHz. Therefore, the insertion loss of each balun is about 1.87 dB, the half of the total loss. The 3 dB bandwidth of each balun is from 42.5 GHz to 65 GHz.

4.2 45 GHz and 60 GHz PAs measurement results

The 45 GHz and 60 GHz PAs are fabricated using CMOS 90 nm process and their die photos are shown in Figure 11(a) and (b). Two PAs are measured using Agilent N5247 PNA, N1913A power meter and N8488A power sensor. In order to measure output saturated power and peak PAE, a driver amplifier is used to provide enough input power. The loss of the on-chip test balun is calibrated out for all the test data.

For the 45 GHz PA, Figure 12 shows the comparison between measured and simulated S parameters at 1.2 V VDD supply. Measured S11 and S22 are better than −9 dB from 40 GHz to 50 GHz. S21 is 20.3 dB at 45 GHz. From the S11 shown in Figure 12, it can be found that measured center frequency has a 3.2 GHz shift to low frequency. Figure 13 depicts the measured output power, gain and PAE as functions of input power at 45 GHz when VDD is 1.2V. At 45 GHz, the PA achieves 21.05 dBm maximum output power with a peak PAE of 14.5% and the output 1 dB compression point is 17.8 dBm.

For the 60 GHz PA, Figure 14 shows the comparison between measured and simulated S parameters at 1.2V VDD supply. Measured S11 and S22 are better than −13 dB from 55 GHz to 65 GHz. S21 is 16.8 dB at 60 GHz. From the S11 shown in Figure 14, it can be found that measured center frequency

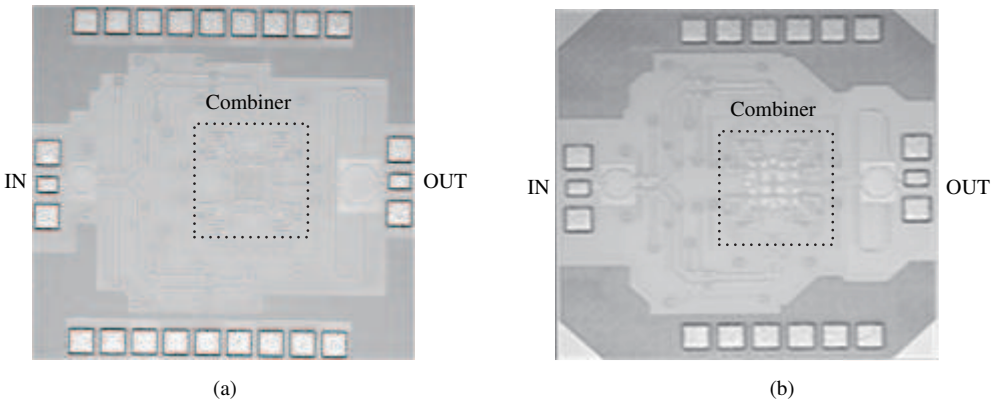


Figure 11 (a) Die micrograph of 45 GHz power amplifier; (b) Die micrograph of 60 GHz power amplifier.

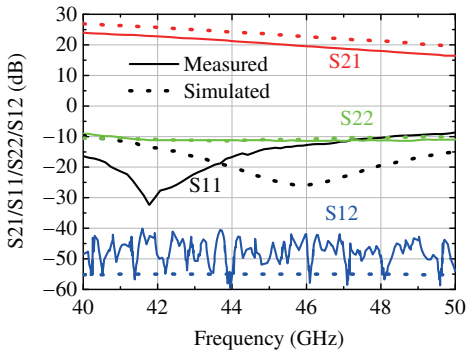


Figure 12 (Color online) Measured and simulated S parameters of the 45 GHz PA.

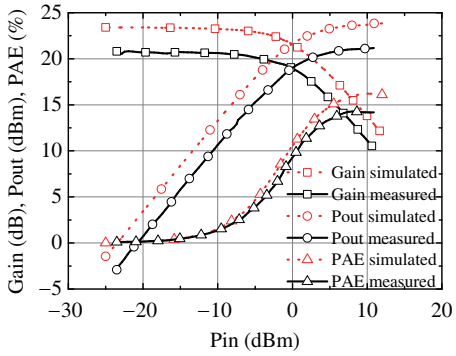


Figure 13 (Color online) Measured and simulated Pout, Gain and PAE at 45 GHz.

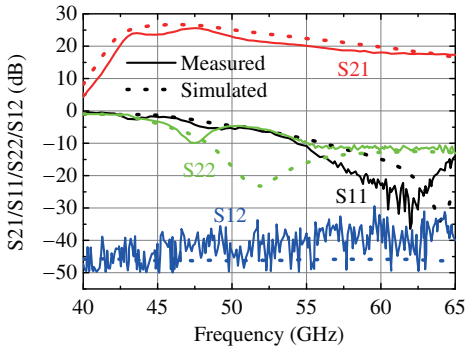


Figure 14 (Color online) Measured and simulated S parameters of the 60 GHz PA.

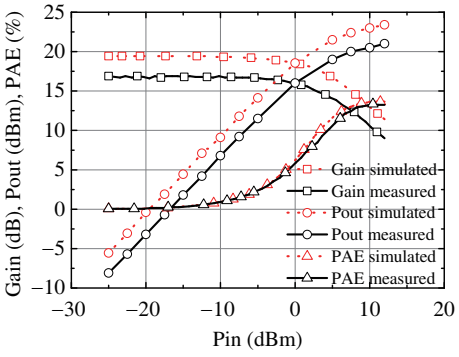


Figure 15 (Color online) Measured and simulated Pout, Gain and PAE at 60 GHz.

has a 2 GHz shift to low frequency. At 47.5 GHz, S11 and S22 are still better than −5 dB and S21 reaches its peak of 23 dB. The gain increases at lower frequency because π-type microstrip matching network has wideband characteristic and does not suppress the gain of the transistor at lower frequency. Figure 15 depicts the measured output power, gain and PAE as functions of input power at 60 GHz when VDD is 1.2 V. At 60 GHz, the PA achieves 21 dBm maximum output power with a peak PAE of 13.4%. Figure 16 provides the measured stability factors of two PAs. Here, the kf is the stability factor. From DC to 67 GHz, the value of kf is bigger than 1. Both PAs are stable.

Table 2 compares two PAs of this work with other reported cutting edge Q-band and V-band PAs in CMOS and SiGe processes [3, 7, 9, 15, 26, 43–49]. The proposed PAs achieve the highest output power

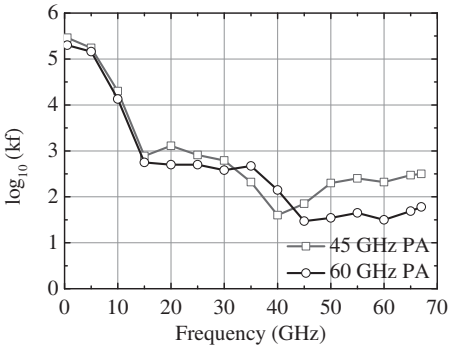


Figure 16 The measured stability factors of 45 GHz and 60 GHz PAs.

Table 2 Benchmark table

Ref.	Process	Freq. (GHz)	P_{sat} (dBm)	P_{1dB} (dBm)	Gain (dB)	PAE (%)	Supply (V)	Area (mm^2)
This work	90 nm CMOS	60	21	17.2	16.8	13.4	1.2	0.675*
[3]	90 nm CMOS	60	19.9	18.2	20.6	14.2	1.2	1.757
[7]	90 nm CMOS	64	23	19.6	16.3	10	1	2
[9]	65 nm CMOS	60	18.5	14.7	20.9	10.2	1.2	0.39*
[15]	130 nm HBT	60	20.5	19.9	20.5	19.4	1.8	0.72
[26]	40 nm CMOS	60	22.6	17	29	7	1.2	2.16
[43]	40 nm CMOS	60	17	13.8	17	30.3	1	0.074*
[44]	40 nm CMOS	60	15.6	15.6	15	25	1	0.96
This work	90 nm CMOS	45	21	17.8	20.3	14.5	1.2	0.918
[45]	45 nm SOI	45	16.5	14	22	23	2.5	–
[46]	120 nm SiGe	45	13.6	12	9.2	25	2.4	0.27
[47]	45 nm SOI	45	19.4	17	9.5	33.9	2.7	0.3
[48]	130 nm BICMOS	45	17.5	15.9	16.6	26	2.5	0.2
[49]	90 nm CMOS	45	10.6	7.5	14.5	8	1.5	0.72

*: Core area.

among PAs in 90 nm CMOS process. This demonstrates the advantages of our proposed fully symmetrical 8-way transformer combiner at mm-wave frequencies.

5 Conclusion

The 45 GHz and 60 GHz PAs based on the 8-way distributed transformer power combiners are presented in this paper. To achieve high output power, power combiner technique is applied. However, traditional distributed active transformer faces unbalanced input impedance among different input ports because of its unsymmetrical layout. Unbalanced port impedance degrades power combining efficiency and reduces output power seriously at the mm-wave frequency regime. Therefore, the transformer combiner with a fully symmetrical layout is proposed to improve the input impedance balance significantly at the mm-wave frequency regime. Both the PAs consist of differential CS stages. The sizes of transistors are carefully optimized to trade-off the gain, efficiency and stability of the circuits. Utilizing a commercial 90 nm CMOS process, the two millimeter-wave PAs are implemented. Taking advantages of the proposed transformer based power combiners, the 45 GHz PA achieves a power gain of 20.3 dB, a maximum PAE of 14.5% and a saturated output power of 21 dBm, and the measured power gain, the maximum PAE, and the saturated output power of the 60 GHz PA, under the 1.2 V supply voltage are 16.8 dB, 13.4%, and 21 dBm, respectively.

Acknowledgements This work was supported by National Natural Science Foundation of China (Grant Nos. 61331006, 61422104), National Science and Technology Major Project of the Ministry of Science and Technology of China (Grand No. 2016ZX03001015-004), and National High Technology Research and Development Program

of China (863) (Grand No. 2015AA01A704).

Conflict of interest The authors declare that they have no conflict of interest.

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