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A 5.8 GHz class-AB power amplifier with 25.4 dBm saturation power and 29.7% PAE

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Abstract In this paper, an effective and succinct radio-frequency (RF) grounding technique for class-AB power amplifier (PA) is presented. The proposed technique employs a grounding path, resonant with a capacitor in series at the center of the fundamental and second-order harmonic frequencies, between the critical ground nodes, to ensure a low impedance path. The power loss due to imperfect grounding is then reduced by 2 dB, and the saturated output power and power added efficiency (PAE) are therefore significantly improved. A fully integrated 5.8-GHz PA with the proposed technique is designed and implemented in a 65-nm CMOS process. Measured result shows a saturated output power of 25.4 dBm and a peak PAE of 29.7%, while with only 2.5 V of supply voltage.

Keywords power amplifier, class AB, high efficiency, fully integrated, CMOS

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1 Introduction

In recent years, great efforts have been made on the CMOS on-chip solution of wireless power amplifiers (PA), due to the benefits of low-cost and high-integration, but suffering from lower output power and efficiency versus their compound counterparts. Many switching-type CMOS PAs have been reported [1] for large output power and efficiency, but with insufficient linearity for variant envelope modulation schemes during application. Currently, industries would prefer the paradigms of an off-chip PA with on-chip pre-driver [2], or SiGe process rather than CMOS [3]. In order to boost the output power of linear CMOS PA, new techniques are investigated such as power combining [4–6], efficiency enhancement [4], and envelop detection [7]. The former two techniques require bulky passive devices [5] with large area consumption, while the latter turns out to be a good solution below 2 GHz band, however, the envelop operational transconductance amplifier (OTA) calls for square-law MOSFETs with large channel lengths and widths, unfortunately heavily loading the PA input and output for applications at higher frequencies. Moreover, along with the scaling down of the CMOS, shrunk supply voltage incurs aggressive scaling up of the current density to retain the same power level. Since the PAs typically use on-chip spiral coil inductor to carry DC current, the voltage headroom degrades substantially due to the finite resistance

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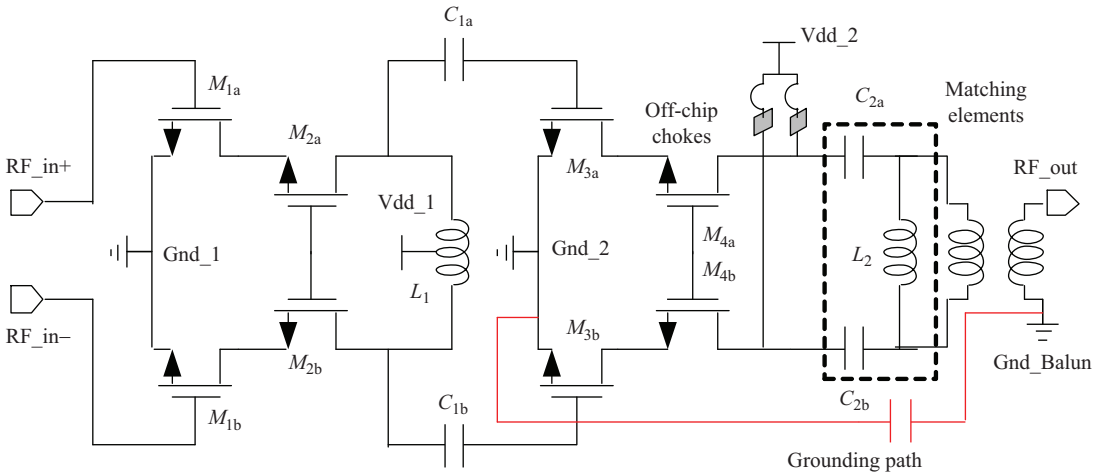

Figure 1 (Color online) Schematic of the proposed PA.

of the coil trace, bringing further challenges to the linearity, output power, and power added efficiency (PAE) of the PA.

In this paper, a 5.8 GHz class-AB CMOS PA with high linear output power and decent efficiency is presented, utilizing a simple but effective radio-frequency (RF) grounding technique to reduce the power loss due to imperfect grounding, and an offchip choke that realized by bond-wire and PCB runners to carry DC current of the power stage for operation under a 2.5-V supply. The PA is implemented fully on-chip in a 65-nm CMOS process and shows superior performances over prior arts.

2 Design of the 5.8 GHz CMOS PA

The schematic of the proposed PA is shown in Figure 1, operating in class-AB mode. The first stage is a pre-driver that provides gain with the differential load inductor resonating with the input capacitor of the next stage. The second stage is a power stage that capacitively couples to the first stage and delivers power to the output. An on-chip balun converts the differential output to single-ended with an insertion loss of 1.2 dB at 5.8 GHz, according to electromagnetic (EM) simulation.

One of the critical issues in PA design is the grounding of different devices, especially for the common source (CS) node of the pseudo-differential pair of power stage (M_3 in this design). The transconductance of this CS differential pair is usually several orders of magnitude larger than that of the gain stage, and it is therefore more easily degenerated by the unavoidable parasitic inductance due to the runner wire in layout or printed circuit board (PCB) [8], degrading the transconductance and output power. For small-signal inputs, this issue can be relaxed by routing the AC ground close to the source of the differential pair. However, due to the class-AB operation the total current of power stage of the PA contains higher order harmonics and is thus not a constant, which will cause AC voltage drop when flowing through the runner, degrading output power and efficiency.

To overcome this issue, critical ground nodes that are physically separated in layout must be shorted at RF. Since the total current of the pseudo-differential pair contains both fundamental and second-order harmonic frequencies in spectrum (because of the class-AB operation) as input power level increases, the RF grounding is therefore mandatory at both frequencies. To this end, the proposed PA introduces a grounding path with a capacitor in series, between the common-source node of the power stage and output ground node of the on-chip balun, as shown in Figure 1. The capacitor is designed to resonate with the parasitic inductors of the path at the center of the fundamental and second harmonic frequencies, ensuring a low impedance between the two ground nodes at both frequencies. Full layout EM-simulation is applied, by strictly distinguishing ground nodes in layout before the bond-wires and PCB runners (hence the ground nodes are not DC-connected on-chip). In this design, the capacitor is optimized as

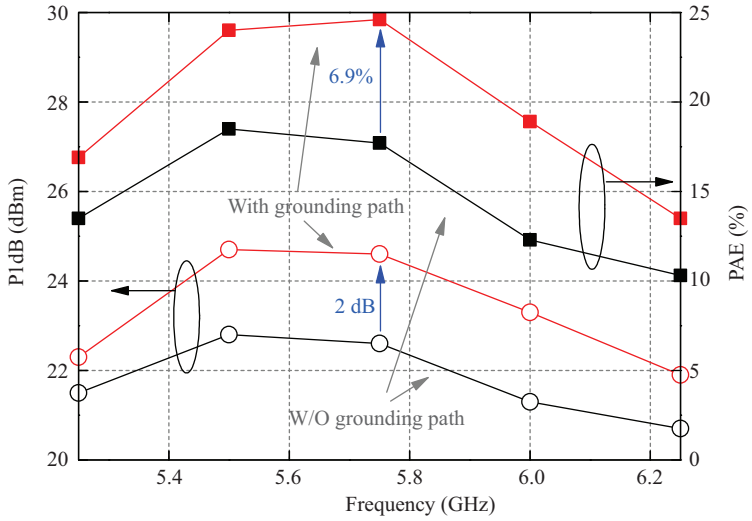

Figure 2 (Color online) Simulated compression point and PAE with or without grounding path.

0.58 pF, which is a reasonable value and readily available on-chip. The inductance of the grounding path is about 0.8 nH. It would be preferable to short the ground nodes separately at the two frequencies, however, two incurred grounding paths are difficult to layout considering the coupling and mutual inductance, complicating the design. Simulation shows an impedance of below 5.5 Ω from 5 GHz to 12 GHz by employing the proposed technique considering process-voltage-temperature (PVT) variations, well covering the bandwidth of interest. The impedance at 5.8 GHz is reduced from 21 Ω to 2.5 Ω.

The effectiveness of the grounding path is simulated and shown in Figure 2. Improvements of 2 dB on output compression point and the 6.9% on the corresponding P1dB PAE are observed at the vicinity of operation frequency.

To sustain the large voltage swing at the PA output, thick gate-oxide transistors (M_4) are used as cascode devices in the power stage. Since these transistors consume a large area, they are distributed in several groups, each of which is with a CS pseudo-differential pair to minimize parasitic inductances. Their gates are connected and bypassed to sources of the CS transistors. The output of each group is fed into the on-chip balun through load-pull matching elements. In addition, the DC of the power stage is supplied with top thick metals, connected to the drain of cascode transistor directly (also for heat dissipation considerations). The on-chip coils of PA do not carry any DC current except for the gain stage, where the current is sufficiently low. The DC feeding pad for the offchip chock is mounted to multiple parallel bong-wires to reduce the voltage drop from the supply line to the drain, allowing the PA to operate with only 2.5 V of supply.

3 Implementation and measurement

The proposed PA is designed and fabricated in a 65-nm CMOS process, and is measured with a vector network analyzer (VNA). The supply voltage is 1 V for the pre-driver and 2.5 V for the power stage. The power stage consumes a current of about 470 mA operating at "deep" class-AB region. The input of the PA is differential, hence an off-chip balun is inserted between the VNA and the differential PA. The S-parameter of this balun is de-embedded from the measurement by calibrations. The S_{11} is well below −10 dB over the entire band of interest (not shown). Figure 3(a) shows the measurement result of the small-signal gain (S_{21}), output saturation power, and PAE versus frequency, while the measured output power and PAE versus input power are shown in Figure 3(b). The measurement agrees with the simulation closely. The S_{21} is roughly 30 dB at the vicinity of an operation frequency of 5.8 GHz, with a $P_{\rm sat}$ of 25.4 dBm and a peak PAE of 29.7%.

The AM-PM distortion of CMOS PA contributes significantly to the error-vector-magnitude (EVM)

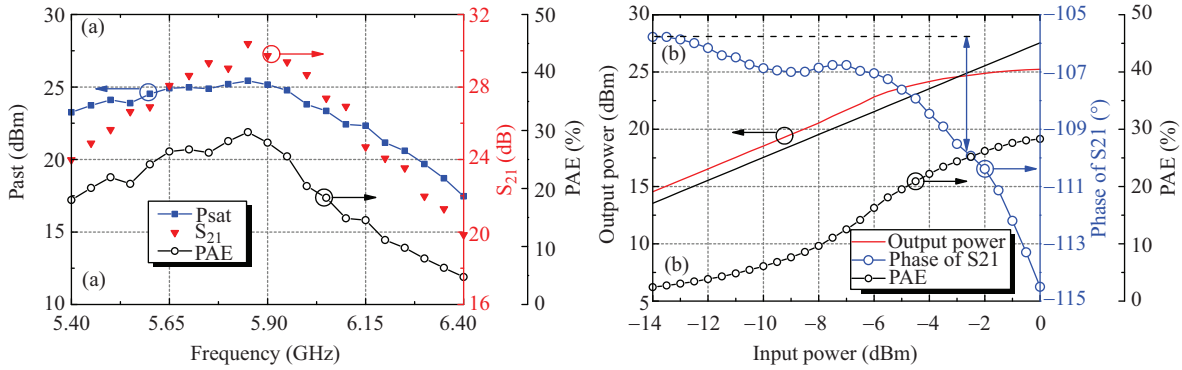

Figure 3 (Color online) Measurement results. (a) S_{21}, output saturation power, and PAE versus frequency; (b) output power, AM-PM distortion, and PAE versus input power.

Table 1 Design parameters of the PA

Devices	Design parameters
$M_{1,2(a/b)}$	32/0.06 (μm/μm)
$M_{3(a/b)}$	960/0.06 (μm/μm)
$V_{b1,2,3}$	0.6 V
$M_{4(a/b)}$	1600/0.28 (μm/μm)
V_{b4}	2 V
L_1	2 nH
C_1	3.3 pF
L_2	1.8 nH
C_2	3.6 pF

Table 2 Comparison with state-of-the-art PAs

	Ref. [4]	Ref. [9]	Ref. [10]	Ref. [7]	Ref. [11]	This work
Freq. (GHz)	2.4	5.5	5.5	1.88	2-6	5.8
S_{21} (dB)	–	12	–	28.3	24	30
P_{sat} (dBm)	27[a)]	26.7	25.5	27.1	22.4	25.4
AM-PM (°)	–	0[b)]	–	5	3.5	4.2
PAE (%)	24[c)]	20[c)]	25[c)]	28	28.4	29.7
V_{dd} (V)	1.2	3.3	3.3	3	3.3	2.5
Area (mm^2)	2	0.27	–	2.2	0.9	0.33
Technique	Power combine	Linearization calibration	Digital calibration	Envelop detection	Harmonic matching	RF grounding
CMOS process	130-nm	65-nm	65-nm	130-nm	65-nm	65-nm

a) Power combined; b) Calibrated; c) Estimated value.

during communication applications, and it is carefully examined versus input power in the measurement. The variation of phase of S_{21} is 4.2° up to 1-dB compression point, as shown in Figure 3(b).

All the design parameters of the PA are listed in Table 1.

Table 2 compares this work with state-of-the-art PAs. It can be seen that the proposed PA exhibits competitive saturated output power and PAE even with PAs operating at 2 GHz band, while the supply voltage is lower than the state-of-the-art levels. The AM-PM distortion is only 4.2° up to 1-dB compression point. Figure 4 shows the die photograph, and an active area of only 0.33 mm^2 is occupied, including the on-chip balun.

4 Conclusion

A fully integrated 5.8 GHz class-AB CMOS PA utilizing a simple but effective RF-grounding technique

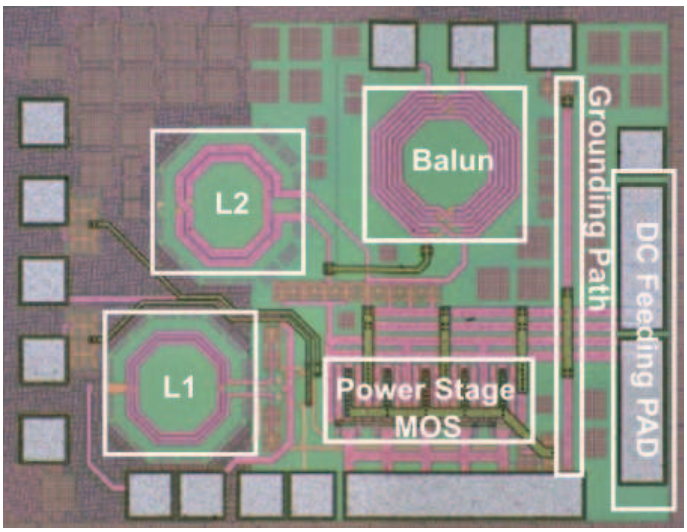

Figure 4 (Color online) Die photograph of the proposed PA.

to reduce the power loss due to imperfect grounding, and an offchip choke that realized by bond-wire and PCB runners to carry DC current of the power stage for operation under a low supply, is proposed and verified in a 65-nm CMOS process.

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Conflict of interest The authors declare that they have no conflict of interest.

References

1 Kim W Y, Son H S, Kim J H, et al. A fully integrated triple-band CMOS class-E power amplifier with a power cell resizing technique and a multi-tap transformer. IEEE Microw Wirel Compon Lett, 2013, 23: 659–661
2 He M, Winoto R, Gao X, et al. A 40 nm dual-band 3-stream 802.11a/b/g/n/ac MIMO WLAN SoC with 1.1 Gb/s over-the-air throughput. In: Proceedings of IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC), San Francisco, 2014. 350–351
3 Huang C W P, Antognetti P, Lam L, et al. A highly integrated dual-band SiGe power amplifier that enables 256QAM 802.11ac WLAN radio front-end designs. In: Proceedings of IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Montreal, 2012. 225–228
4 Liu G, Haldi P, Liu T J K, et al. Fully integrated CMOS power amplifier with efficiency enhancement at power back-off. IEEE J Solid-State Circ, 2008, 43: 600–609
5 Chowdhury D, Hull C D, Degani O B, et al. A single-chip highly linear 2.4 GHz 30 dBm power amplifier in 90 nm CMOS. In: Proceedings of IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC), San Francisco, 2009. 378–379
6 Kumar R, Krishnaswamy T, Rajendran G, et al. A fully integrated 2×2 b/g and 1×2 a-band MIMO WLAN SoC in 45 nm CMOS for multi-radio IC. In: Proceedings of IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC), San Francisco, 2013. 328–329
7 Kousai S, Onizuka K, Yamaguchi T, et al. A 28.3 mW PA-closed loop for linearity and efficiency improvement integrated in a +27.1 dBm WCDMA CMOS power amplifier. In: Proceedings of IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC), San Francisco, 2012. 84–86
8 Razavi B. RF Microelectronics. 2nd ed. Upper Saddle River: Prentice Hall, 2011
9 Afsahi A, Behzad A, Magoon V, et al. Fully integrated dual-band power amplifiers with on-chip baluns in 65 nm CMOS for an 802.11n MIMO WLAN SoC. In: Proceedings of IEEE Radio Frequency Integrated Circuits Symposium, Boston, 2009. 365–368
10 Lee C P, Behzad A, Marholev B, et al. A multistandard, multiband SoC with integrated BT, FM, WLAN radios and integrated power amplifier. In: Proceedings of IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC), San Francisco, 2010. 454–455
11 Ye W, Ma K, Yeo K S. A 2-to-6 GHz Class-AB power amplifier with 28.4% PAE in 65 nm CMOS supporting 256QAM. In: Proceedings of IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC), San Francisco, 2013. 1–3