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Testing of 1TnR RRAM array with sneak path technique

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Dear editor,

RRAM is regarded as one of the most promising candidates among emerging nonvolatile memory technologies [1,2]. Recently, the 1TnR RRAM structure, in which n RRAM cells in each row share a common bottom electrode connected to the drain node of a selector transistor, was proposed to improve the integration density [3,4]. The area of the 1T4R RRAM test chip is 30% smaller than that of the conventional 1T1R cell [3]. However, the complexity of the conventional March test algorithm for a memory array is proportional to the number of memory cells in the array, which results in a long test time when the algorithm is applied to the 1TnR RRAM array, because each memory cell is accessed in the test process. The test method poses a serious challenge for the 1TnR RRAM array, which has not been studied thus far. In this letter, we propose a test method for the 1TnR RRAM array that employs the sneak current of the 1TnR array as a signature.

The sneak current is the current flowing through the sneak path. When an RRAM cell is selected as the target cell, say, R1 in the 4×4 1T4R RRAM unit shown in Figure 1, the unselected cells are classified into three groups: (1) the cells in the same row as, but a different column from, the selected target cell (denoted by the red cells in Figure 1); (2) the cells in the same column as, but a different row from, the selected target cell (denoted by the yellow cells in Figure 1); and (3) the cells in a different row and different column from the selected target cell (denoted by the green cells in Figure 1). When the read voltage $V_{\rm read}$ is applied, the sneak current flowing in series through the selected transistor, and one RRAM cell of group1, group3, and group2, respectively, contributes to the read current on the bit line. This read current on the target bit line reveals the fault in the memory unit.

To exploit the sneak current information, in the test mode, the read operation is applied without any sneak current suppression technique. In the proposed method, the sneak-path-based read operation is applied in three steps.

Step1: Read each RRAM cell in one row, e.g., the first row of the RRAM array.

Step2: Compare the current on each bit line with the threshold value of the fault-free bit lines in order to find the suspicious columns that consist of faulty RRAM cells.

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Step3: Read each RRAM cell in the suspicious column except the cell read in Step1 in order to localize the faulty RRAM cells; do nothing if no suspicious column is detected in Step2.

This three-step read operation is based on the fact that the RRAM cells belonging to the first and second groups have a greater influence on the current on the bit lines. The addressing mode used in the proposed read operation is denoted as '$\updownarrow_T$' owing to its row-decision-column style.

By incorporating the proposed read operation with the traditional March elements, we design a test algorithm for the 1TnR RRAM array as follows:

$$\begin{aligned}&\text{RRAM-1TnR-Sneak}\\&\quad=\{\Updownarrow(w0,w0,w1);\updownarrow_T(r1);\Updownarrow(r1);\\&\qquad\updownarrow_T(r1);\Updownarrow(w1,w0);\updownarrow_T(r0)\}.\end{aligned}$$

The proposed algorithm covers most of the existing RRAM fault types [5,6], including the stuck-at 0/1 fault (SA0/1), slow write 0/1 fault (SW0/1), deep 0/1 fault (DEEP 0/1), unknown read fault (UR), read 1 disturb fault (R1D), and transition fault (TF), more effectively than the March C- and March C* algorithms [6].

The number of cell accesses in the proposed sneak-path-based read operation varies across cases because there is a decision in the read operation. Assume that a single faulty cell is distributed randomly in an $M\times N$ 1TnR RRAM array, where $N = k\times n$ and k is an integer. The proposed sneak-path-based read operation tests the faults in N cell accesses if the faulty cell is in the row read by Step1; otherwise, it needs $(N+M-1)$ cell accesses to detect the fault. The expectation on cell accesses for fault diagnosis of a single fault is given by $N+M-2+1/M$. For double fault cases, the average cell accesses required with the proposed read operation is approximately equal to $N+2M-4+M/N$.

For an $M\times N$ 1TnR RRAM array, where $N = k\times n$ and k is an integer, the complexity of the proposed RRAM-1TnR-Sneak test algorithm is only $6MN+3N$ for fault detection, because the algorithm consists of 6 read/write operations with the '$\Updownarrow$' addressing mode and 3 read operations with the '$\updownarrow_T$' addressing mode. The complexity of fault location depends on the number of faults and their distribution in the array. It is computed as $6MN+3(N+\text{sc}\times(M-1))$, where sc is the number of suspicious columns, $\text{sc}\leqslant N$. The proposed test algorithm is efficient and it outperforms the previous RRAM test algorithms that can be used to test the 1TnR RRAM array; both the March C- algorithm and the March C* algorithm have a complexity of $10MN$ [6].

Experiments. RRAM faults manifest as variations in the resistance values of the RRAM cells, and the stuck-at faults are typical faults of the resistance values. The effectiveness of the proposed test algorithm is limited by the resistance values of the RRAM cells. We conducted simulation experiments to determine the resistance variation limits for different cases.

The fabricated test chips all had the existing 1T4R RRAM structure [4], although the 1TnR RRAM model has been discussed in the literature [3,4]. The simulations were carried out on the 1T4R RRAM array in our work. Chen et al. [6] tested RRAM sample chips and found that the cells with SA1 and SA0 faults account for 9.04% and 1.75%, respectively, of the total memory cells in the array. In one 1T4R RRAM unit with 16 RRAM cells, the expected cells with SA1 and SA0 faults are $16\times9.04\% = 1.4464$ and $16\times1.75\% = 0.28$, respectively. Accordingly, in one 1T4R RRAM unit, the single-bit SA1 and SA0 faults and the double-bit SA1 fault are considered in our simulation experiments.

The experiment was performed in the following steps.

Step1: Four non-overlapping cases for the single-bit SA1 and SA0 faults and six non-overlapping cases for the double-bit SA1 fault were identified according to the location of the faulty cells in the 4×4 1T4R RRAM unit.

Step2: The simulations of the read current on the bit lines were conducted for these cases with the PSPICE simulator. In the simulation, the V_{read} was set to 1 V, and the typical resistance values of the high-resistance state and low-resistance state were 500 kΩ and 10 kΩ, respectively [4]. The read current difference between a column with a faulty cell and that without a faulty cell was employed as the signature of the suspicious columns. The cases with the smallest signature value were taken as the worst cases in the simulations because smaller resistance variations can erase the signature.

Step3: For the worst cases, read current vs. resistance variation curves were plotted on the basis of the simulations in which the same absolute resistance variations were applied to all the RRAM cells except the faulty cell. Here, we take the single-bit SA1 fault as an example. The read current decreases as the resistance variation increases if a memory cell in the same column as the faulty cell is read, whereas it increases if a memory cell in a different column is read. The intersection point of these two curves denotes the tolerance limit of the resistance variation of the proposed read oper-

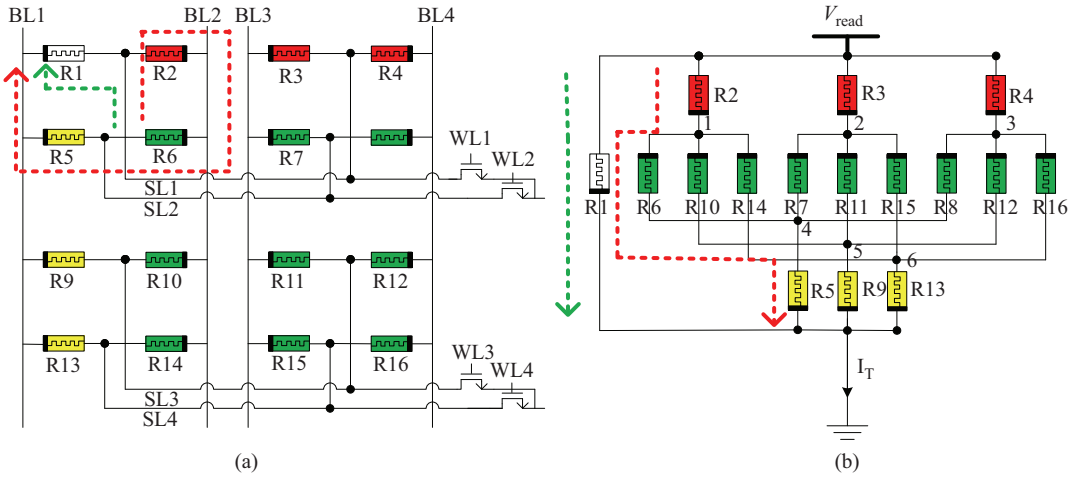

Figure 1 Sneak path in 1T4R RRAM unit. (a) Sneak path of the read operation for cell R1 and (b) the equivalent circuit.

ation for the single-bit SA1 fault. The simulation results indicate that the proposed read operation for the single-bit SA1 fault fails if the resistance variation is greater than 8.8%. Similarly, the resistance variation limits for the single-bit SA0 fault and the double-bit SA1 fault are found; the tolerance limits are 5.6% and 7.8%, respectively.

To determine the impact of array size on the proposed test method, simulations of resistance variation limits vs. size of the 1TnR RRAM array were carried out. The simulation results indicate that, for an $M\times N$ 1TnR RRAM array, where $N = k\times n$ and k is an integer, the resistance variation limit increases as n increases and decreases as M increases. This implies that the proposed test method is more applicable to flat 1TnR RRAM arrays, in which n is large and M is small. The limits are greater than 5% if M is less than 5. The application of the proposed test algorithm to a $4\times N$ 1TnR RRAM unit is a recommended test method.

Conclusion. This letter proposed a new sneak-path-based read technique that accesses the memory array in a row-decision-column style for 1TnR RRAM testing. For an $M\times N$ 1TnR RRAM array, this read technique tests the suspicious columns in only N cell accesses. The proposed read operation is able to tolerate the resistance variation within limits for different cases of faulty cell distribution. A March-like test algorithm, namely RRAM-1TnR-Sneak, incorporates the sneak-path-based read technique, and is able to cover all the fault types in the 1TnR RRAM array. It has a complexity of $6MN+3N$, which is much lower than that of the conventional March test algorithms, for fault detection. Moreover, the complexity of the proposed test algorithm for fault localization depends on the distribution of faulty cells, and it is lower than that of the March test algorithms even for the worst cases.

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