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Electrical performance of static induction transistor with transverse structure

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Abstract A novel static induction transistor with transverse surface gate structure was designed and successfully fabricated in this paper. Its basic electrical characteristics and frequency performance was investigated in depth. The optimum technological parameters such as source-gate space and epitaxial layer thickness for obtaining excellent frequency performance and high blocking voltage capacity were represented and discussed in detail. The main advantage of this work is that the performances of device were improved with simple structure and technological processes. The experimental and simulated results demonstrate the trans-conductance g_m and gate-source breakdown voltage BV_{GS} of the transverse type SIT increase from 60 to 87 ms and 20 to 26 V, respectively, in addition to obtaining higher than 100 MHz operating frequency under relatively simple technology processes compared with those of traditional vertical SIT.

Keywords static induction transistor, surface gate, transverse structure, parasitical capacitance, gate-source breakdown voltage

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1 Introduction

For the basic static induction transistor (SIT), many works focus on optimizing the materials and analyzing the operational mechanisms of SIT in recent years [1–6]. Although switching speed and voltage capacity of SIT have been increased because of the use of SiC or GaN, the immature theory and mechanism of the devices cause the difficulties of manufacturing processes [3,4]. And organic static induction transistors have a low operational voltage with reproducible characteristics but high resistivity of organic materials reduces device speed greatly [5,6]. So Si-based SITs have been practically recognized as the research focus duo to their excellent electrical characteristics and relatively complete theory compared with SiC or organic static induction transistor. Conditional vertical short channel Si-based SITs are also limited in high-speed and high-power operations due to some disadvantages including the local oxidation and self-aligning processes [7], the self-doping effect [8], complex technologies or low gate-source breakdown voltage [9,10]. And the drain and source regions of traditional SIT with vertical structure profiles

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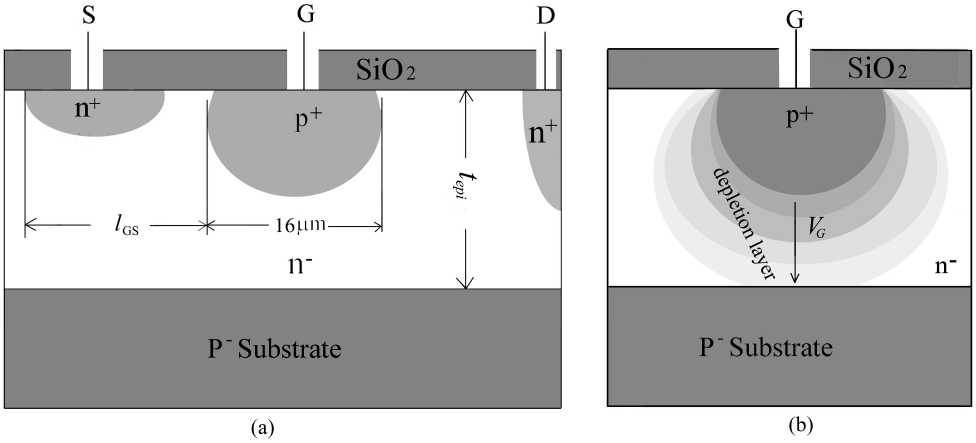

Figure 1 Cross-section of a unit of a TSIT (a) and potential distribution of channel at different gate voltages (b).

are distributed on the two sides of wafer, so the drain current must flow vertically through very long drifting region (usually about 330 μm) from the source to the drain, taking a rather long time for carriers to travel from the source to the drain terminals, so decreasing operating frequency. In order to improve operating frequency and power performances synchronously, a novel transverse structure SIT with surface gate, referred to as TSIT (transverse static induction transistor), has been designed and fabricated on thin film successfully in this paper. The effects of structure and technological parameters on switching frequency, gate efficiency and breakdown voltage are analyzed in depth. Some optimum technological measures for improving the breakdown voltage of TSIT are proposed. The experimental and simulated results indicate that TSIT is a desirable device for high power and high frequency applications.

2 Structure description and operating mechanism

In order to study the operating mechanism and electrical performances, a TSIT sample is fabricated. The main fabrication steps are as follows. A lightly doped p^--type single crystal Si with resistivity of 120 Ω-cm is used as the original wafer. An n^--type epitaxial layer doped at $N_d^- = 1\times10^{14}$ cm^{-3}, is thermally grown to the thickness t_{epi}, smaller than the sum of the diffusion depth of gate, the depletion region widths of p^+n^- and p^-n^- junction. An oxider layer is thermally grown on the epitaxial layer at 1050° about 0.4 μm, p^+ gate with the width of 16 μm is formed by boron diffusion and the junction depth is 8 μm. Next phosphorus are selectively diffused into the windows defined by masking at 1150° for 15 min forming n^+ source and n^+ drain regions. Finally, the electrodes of source, gate and drain are realized by DC sputtering Al/Ti/Pt metal layers and Nickel film on the samples [11]. The second epitaxy, local oxidation and mesa etching, used in conventional SIT, are not required for fabricating TSIT from the fabrication processes described above. The geometrical model of TSIT is given in Figure 1(a).

The epitaxial layer between the gate and substrate region of TSIT, called the channel, is pinched off by depletion layer of single p^+n^- junction formed between p^+-gate and n^--epitaxial layer, and the drain current is controlled by the potential barrier established in the channel. The electric filed in the direction from the drain to the source terminal generated by positive drain voltage V_D and the lateral component of the electric filed in the opposite direction produced by negative gate voltage V_G, constitute an electrical potential barrier with a saddle in the channel. Therefore, TSIT is a normally-on device, and is controlled by the potential barrier. In order to prevent carriers from flowing into substrate, the substrate (p^-) is doped very lightly, approaching intrinsic material and biased at the lowest potential to make the p-n junction between epitaxial layer and substrate zero or negatively biased.

Figure 1(b) shows the channel potential distribution between the gate and substrate with the increase in gate voltage. It can be seen that the potential barrier is rising with the increase in gate voltage. So the gate voltage V_G controls the drain current by means of controlling the channel potential barrier. In

blocking state, the depletion layer occupies all epitaxial layer space between the gate and substrate. The electrons injected from the source are blocked by the potential barrier in the channel, so that most of them can not reach the drain region. Only a very small part of them with energy higher than the height of potential barrier can penetrate potential barrier region to arrive at drain forming drain leakage current.

When the source, gate and drain regions are all laterally arranged on the surface of wafer, a considerably small effective junction area between the gate and the source results in good frequency performance and fast switching operation because of the small gate-source parasitical capacitance C_{GS} of TSIT. Furthermore, the gate efficiency, defined as the control sensitivity of gate voltage V_G to drain current I_D, might be high because the current I_D in TSIT flows transversely near the surface under the gate region from the source to drain.

3 Parameter design consideration

The channel between the drain and source of TSIT is blocked by the depletion layer between the gate and substrate, establishing a potential barrier saddle. The gate location directly affects the switching characteristics. For a given length between the drain and source edges, closer distance between the drain and gate means that the p^+- n- n^+ base region length becomes shorter, resulting in the increase in the leakage current. For more sensitive controlling the gate voltage to the potential barrier and higher gate efficiency, the reduction in the distance l_{GS} from the gate to source terminal is an effective step. But l_{GS} has contrary effect on the gate-source input capacitance C_{GS} that can result in frequency decreasing. And with the decrease in the space between gate and source, not only surface states and tunneling current effects would lead to device failure, but also the breakdown voltage BV_{GS} may be degenerated, resulting in low blocking gain. In order to improve gate-source breakdown performance without a lowering in gate efficient and frequency performance, an appropriate l_{GS} of 12 μm is adopted in the device by the trade-off about technological and structural design.

For the length, the pinch-off voltage V_p of 1.46 V to make the n^- region between the gate and the source depleted is obtained following Eq. (1) [12],

$$V_p = \frac{q \cdot N_d^-}{2 \cdot \varepsilon} l_{GS}^2 - V_{bi}, \tag{1}$$

where ε is the permittivity of free space, q is the elementary charge, and V_{bi} is a built-in voltage determined by the mechanism of the carriers going across the barrier, which is a function of the thermal voltage V_T, intrinsic carrier concentration n_i, the epilayer doping N_d^- and the gate density N_G, respectively. Here, it can be assumed that the abrupt plane junction is valid as the depth of the n^+ source region is much smaller than that of the p^+ gate region. It means that a 1.46 V additional biased gate voltage can build up enough high channel barrier to block the drain current. In the case the source, drain and gate regions are doped with impurity concentrations of N_S=1×10^{19} cm^{-3}, N_D=1×10^{19} cm^{-3} and N_G=1×10^{19} cm^{-3}, respectively, which are far higher than that of epitaxial layer and channel region, leading to the fact that the channel can be easily depleted to form high-level injection, and a high breakdown voltage can be formed for TSIT.

According to Poisson equation, we can obtain the channel potential distribution function $\Phi(x, y)$ [13,14],

$$\Phi(x, y) = \Phi_p(y) + \Phi_L(x, y), \tag{2}$$

where $\Phi_p(y)$ is Poisson potential generated by channel charge and $\Phi_L(x, y)$ is two-dimension Laplace potential caused by the applied voltage. Because channel electric-field distribution is mainly derived from ionized donor positive charges and ended by acceptor negative charge, $\Phi_p(y)$ can be expressed as

$$\Phi_p(y) = -\frac{qN_d^-}{2\varepsilon} y^2 + C, \tag{3}$$

where C is coefficients determined by boundaries condition. Suppose the lateral distribution along x which is vertical to the channel obeys Polman distribution, the total potential $\Phi(x, y)$ in the axial direction of

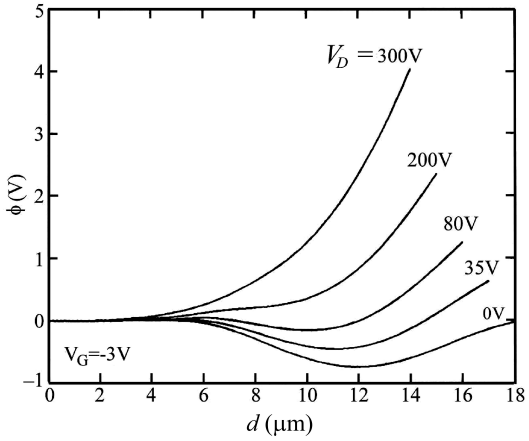

Figure 2 Potential distribution in channel under different drain voltage.

the channel ($y = 0$) is given by

$$\Phi(x,0) = V_G^* + \left[A\exp\left(-\frac{\pi}{2}\frac{x}{a}\right) + B\exp\left(\frac{\pi}{2}\frac{x}{a}\right)\right], \tag{4}$$

where the barrier-modulation factors A and B can be determined from the device structure and the applied voltage, a is the half-width between gate and substrate and $V_G^* = V_G + V_P$ is the net applied gate voltage.

The numerical simulation results of potential distribution in channel under different drain voltage are given in Figure 2 by substituting the device parameters. For the given −3 V gate voltage, with the increase in the drain voltage, the potential barrier is continuously lowered down, and its saddle point moves toward the source terminal of channel. So the distance of 12 μm between the edge of the n^+ source region and the edge of the p^+ gate at $V_D = 0$ is necessary for the researched TSIT when V_G is fixed at −3 V, which shows that the barrier vanishes at the source end of the channel beyond some limit of gate voltage, or electrostatically there is no current in the channel.

In order for the TSIT to have triode-like I-V characteristics, the drift region below the gate region must be fully pinched off by negative gate voltage before the drain voltage approaches the power source voltage. For more effective modulation of channel pinch-off at low injection for the designed transverse SIT, t_{epi} must be also smaller than the sum of the depth of boron diffusion of gate region (about 8 μm), the depletion region widths of p^+n^- and p^-n^- junction which are about 3 μm and 19 μm following Eq. (5), respectively, by supposing the abrupt plane junction,

$$W = \left\{\frac{2\varepsilon\cdot(V_{bi}+V_G)}{q}\cdot\frac{n_d+n_a}{n_d\cdot n_a}\right\}^{\frac{1}{2}}, \tag{5}$$

where n_a,n_d, and V_{bi} are the corresponding doping density and built-in voltage of the gate region or drain region and epitaxial layer, respectively. So the thickness of the epitaxial layer t_{epi} is less than 30 μm by substituting the relevant device data.

The given two-dimension potential distribution has a saddle shape shown as in Figure 2. The channel barrier is decreasing and moving toward the end of the source with the increase in the drain voltage V_D. When V_D increases to a certain value the potential produced by the interaction of gate-source and drain-source electric field will vanish in the channel. The minimum potential $\Phi_{\min}$ can be expressed as [15]

$$\Phi_{\min}(x_{\min},0) = V_G^* + 2\sqrt{A\cdot B}. \tag{6}$$

Then, we can acquire the minimum intrinsic drain voltage $V_{D\min}^*$ by letting $\Phi_{\min} = 0$, or

$$\Phi_{\min}(x_{\min},0) = V_G^* + 2\sqrt{A\cdot B} = 0, \tag{7}$$

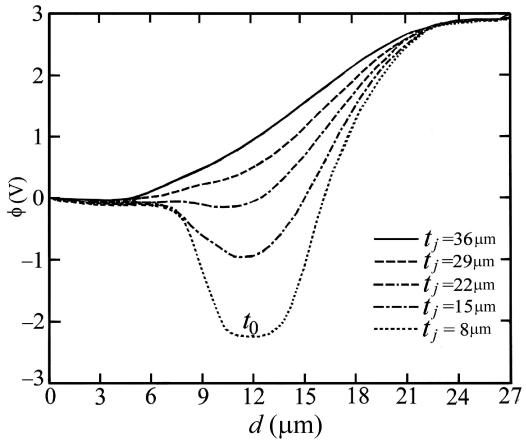

Figure 3 Potential distribution profile along the channel.

$$V^*_{D\,\min} = \frac{1}{2} \cdot \frac{(\mu_0 - 1)^2}{\mu_0} \cdot V^*_G, \tag{8}$$

where $\mu_0 \approx \exp \frac{\pi L}{2a} > 1$ is the intrinsic electrostatic gain determined by the channel length L (here is approximately to gate width) and the distance between the gate and substrate, which is evaluated as a value of 8.35 in our device structure. So $V^*_{D\min}$ is about 4.98 V at -3 V gate voltage, by which the maximum drain voltage of about 5 V is estimated in order for building nonzero barrier potential in the channel.

The two-dimensional numerical simulations of channel potential distribution along central line at different depth for 3 V gate voltage, 5 V drain voltage are given in Figure 3, in which the coordinate denotes the transverse distance of each inner point to the source. The potential in channel t_0 corresponds to the valley point of the potential, where the electric field is zero and blocks electrons flowing from source to drain. The closer the channel to the surface, the higher potential barrier saddle is, the more sensitive the controlling capability of the gate. And the barrier gets flattened when t_j approaches to 22 μm, which means the maximum epitaxial layer thickness for good blocking state and controlling capacity. So an epitaxial layer thickness t_{epi} of about 22 μm is an appropriate trade-off when the distance between the edge of the n^+ source region and the edge of the p^+ gate equals 12 μm for the designed device.

For the special structure, the barrier is built up under a certain biasing condition. It can be noted that the two values such as t_{epi} and l_{GS} are only valid for the researched device structure and vary with different device geometrical structure.

4 Results and discussion

4.1 I-V characteristics

The experimental samples are tested and the measured I-V characteristics of TSIT indicate the TSIT has the standard features of non-saturating triode-like I-V characteristics shown as in Figure 4(a). Large trans-conductance is obtained from the slope of the abruptly straight I-V characteristic lines to indicate the ability of V_G controlling the channel potential barrier related to V_D, and high quality breakdown performance is demonstrated by Figure 4(b). The measured main electrical parameters of a single cell TSIT and a vertical type SIT with similar doping concentration from [13,16] are tabulated in Table 1. Comparison of two sets of experimental results shows there is an apparent improvement in the key parameters including V_p, gate-source breakdown voltage BV_{GS}, trans-conductance under a certain gate biased voltage although there is a slight reduction in the maximum BV_{GD} from 140 to 134 V due to the decrease in epitaxial thickness and the saturation drain current from 0.53 to 0.49 A because of the decrease in gate-drain effective area possibly. And g_m and BV_{GS} increase from 60 to 87 ms and 20 to 26 V, respectively by the technological measures proposed in this paper, which shows that the superior

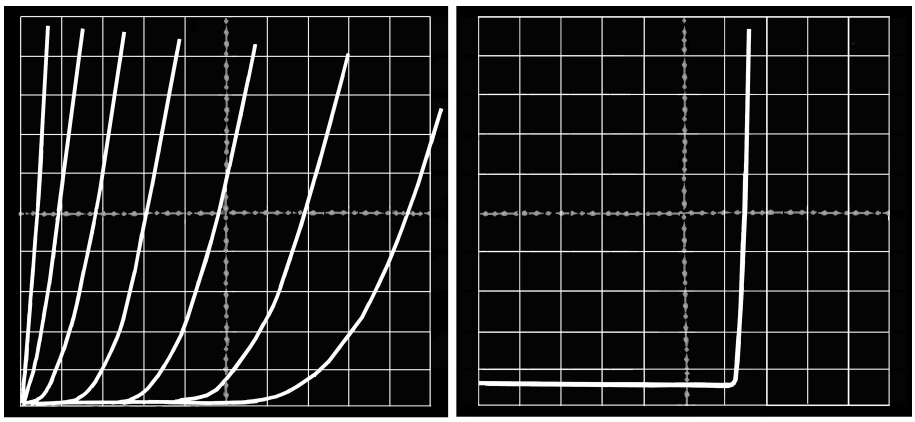

Figure 4 Measured results of TSIT. (a) I-V characteristics, V_{DS}: 20 V/div; I_D: 5 A/div; (b) gate-source breakdown performance, BV_{GS}: 4 V/div; I_D: 0.1 mA/div.

Table 1 Experiment parameters of single cell TSIT and vertical SIT

Parameters	$-V_p$ (V)	I_{DSS} (A) (V_G=0 V, V_D=10 V)	g_m (mS)	BV_{GD} (V)	BV_{GS} (V)	Frequency (MHz)
Vertical structure SIT	1.57	0.53–1	60	14	2	25
TSIT	146	0.49–1	87	134	26	>100

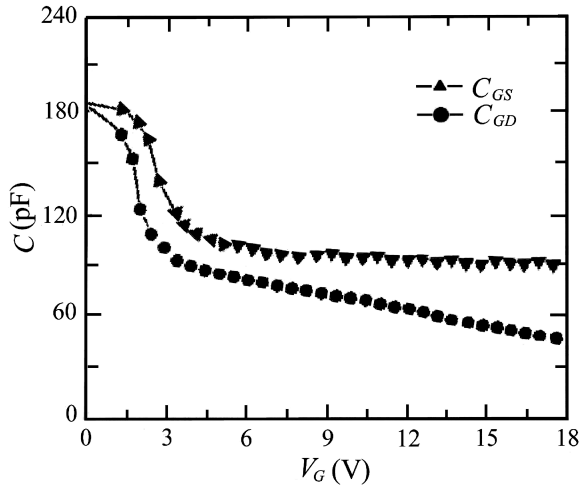

Figure 5 Dependence of capacitance C_{GS}, C_{GD} on negative gate voltage.

electrical performance including high gate efficiency and high frequency characteristic can be realized from its small junction area and simple technology compared with traditional SIT.

4.2 Frenquency performance

The dependences of input capacitance C_{GS} and C_{GD} on negative bias-voltage are demonstrated in Figure 5. It is observed the capacitance C_{GS} and C_{GD} are varying greatly with the increase in the gate voltage $|V_G|$. Compared with the gate-drain capacitance, larger gate-source capacitance C_{GS} is key parameter of influencing frequency. C_{GS} is decreasing greatly when V_G is larger than 1.5 volts, which nearly corresponds to the calculated value of -1.46 V by Eq. (1) at which the region between the gate and source is completely pinched off. And C_{GS} is almost constant when more than 3 V gate voltage is applied. So in order to improve frequency performance significantly, the high bias voltage (>3 V) should be applied on the gate in the experiment.

Thus the frequency performance f_m is estimated following the Eq. (9) [17],

$$f_m \approx \frac{g_m}{2\pi C_{GS}}, \tag{9}$$

where g_m and C_{GS} are the parameters determined by the results from Figures 4 and 5, which are 87 mS and 135 pF under 3 V gate biased voltage, respectively. So f_m is about 103 MHz for the researched TSIT. The experimental data indicates that if the total parasitical capacitance is reduced below 4 pF, the operating frequency will larger than 300 MHz.

Some technological approaches have been developed according to the experimental results for the consideration of the trade-off among gate sensitivity, frequency performance and BV_{GD}. For example large sheet resistance of the gate region ($R_\square = 45\ \Omega/_\square$), the relatively low epitaxial layer impurity concentration of $1-3\times 10^{13}/\mathrm{cm}^{-3}$, and a field plate with 50 μm length are necessary [18].

5 Conclusion

Besides high breakdown voltage BV_{GS}, the other electrical performances of TSIT such as potential distribution and I-V characteristics are obtained successfully by the simple fabrication processes. For the relatively small area between the source and gate, gate-source parasitical capacitance C_{GS} decreases significantly, which is favorable for raising the frequency characteristics and gate efficiency compared with the conventional surface gate SIT. The shorter the distance from gate to the source terminal, the higher the gate efficiency. However, the breakdown voltage BV_{GS} may be degenerated, and the parasitical capacitance C_{GS} may increase, resulting in a decrease in operating frequency of TSIT. In order to achieve high breakdown voltage and frequency efficiency, structural parameters, technological parameters and gate voltage should be taken into compromise consideration in practice.

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Conflict of interest The authors declare that they have no conflict of interest.

References

1 Zhang Y, Yang J H, Cai X Y, et al. Exponential dependence of potential barrier height on biased voltages of inorganic/organic static induction transistor. Chinese J Semicond, 2010, 31: 044002
2 Wang Y S, Wu R, Liu C J, et al. Researches on the injected charge potential barrier occurring in the static induction transistor in the high current region. Semicond Sci Tech, 2008, 23: 152–156
3 Chen G, Wu P, Bai S, et al. 213 W 500 MHz 4H-SiC static induction transistor. Appl Mech Mater, 2012, 130: 3392–3395
4 Weimann N G, Eastman L F, Obloh H, et al. GaN static induction transistor fabrication. In: Proceedings of the 26th International Symposium on Compound Semiconducors, Berlin, 1999
5 Fanghua P, Yasuyuki W, Hiroshi Y, et al. Effect of gate insulating layer on organic static induction transistor characteristics. Thin Solid Films, 2009, 518: 514–517
6 Chen J B, Wang D, Zhang Y, et al. Analysis of the current transport mechanism of copper phthalocyanine organic static induction transistor. In: Proceedings of International Conference on Measurement, Information and Control (ICMIC), Harbin, 2013. 190–193
7 Yang J H, Sheng X Y, Wei Y, et al. Potential barrier height dependence on biased voltages of static induction thyristors. In: Proceedings of the 7th International Power Electronics and Motion Control Conference (IPEMC), Harbin, 2012. 2–5
8 Liu C J, Liu S, Bai Y J. Dependence of transient performance on potential distribution in a static induction thyristor channel. Chinese J Semicond, 2012, 33: 044009
9 Zhang L J, Yang J H, Zhao F H. The characteristics of ESD protection device based on static induction thyristors. Appl Mech Mater, 2013, 303: 1803–1807
10 Nishizawa J I, Motoyan K. The 2.45 GHz 36 W CW Si recessed gate type SIT with high gain and high voltage operation. IEEE Trans Electron Devices, 2000, 47: 82–87
11 Liu C J, Liu S, Bai Y J. Switching performances of static induction thyristor with buried-gate structure. Sci China Inf Sci, 2014, 57: 062401

12 Michio K, Yukio H, Mar1 K J, et al. Characteristics of high-power and high-breakdown-voltage static induction transistor with the high maximum frequency of oscillation. IEEE Trans Electron Devices, 1982, 29: 194–198
13 Li S Y. Static Induction Devices Theory (in Chinese). Lanzhou: Lanzhou University Press, 2002. 187–202
14 Wang C, Wu C L, Wang J X, et al. Analytical current model of tunneling field-effect transistor considering the impacts of both gate and drain voltages on tunneling. Sci China Inf Sci, 2015, 58: 022402
15 Li H R, Li S Y. Physical features of the barrier-controlled blocking function of the static induction thyristor. IEEE Trans Electron Devices, 2011, 58: 1149–1157
16 Zhu Y C, Liu Y H, Zhang L J, et al. Surface-gate SIT with high breakdown voltage for low power applications. In: Proceedings of the 2nd International Symposium on Instrumentation and Measurement, Sensor Network and Automation (IMSNA), Toronto, 2013. 867–870
17 Wang Y S, Li H R, Hu D Q. A microwave high power static induction transistor with double dielectrics gate structure. Chinese J Semicond, 2004, 25: 19–25
18 Wang Y S, Feng J J, Liu C J, et al. Improvements on voltage-resistant performance of bipolar static induction transistor (BSIT) with buried gate structure. Sci China Inf Sci, 2012, 55: 962–970