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Design of a novel static-triggered power-rail ESD clamp circuit in a 65-nm CMOS process

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Abstract This work presents the design of a novel static-triggered power-rail electrostatic discharge (ESD) clamp circuit. The superior transient-noise immunity of the static ESD detection mechanism over the transient one is firstly discussed. Based on the discussion, a novel power-rail ESD clamp circuit utilizing the static ESD detection mechanism is proposed. By skillfully incorporating a thyristor delay stage into the trigger circuit (TC), the proposed circuit achieves the best ESD-conduction behavior while consuming the lowest leakage current ($I_{\rm leak}$) at the normal bias voltage among all investigated circuits in this work. In addition, the proposed circuit achieves an excellent false-triggering immunity against fast power-up pulses. All investigated circuits are fabricated in a 65-nm CMOS process. Performance superiorities of the proposed circuit are fully verified by both simulation and test results. Moreover, the proposed circuit offers an efficient on-chip ESD protection scheme considering the worst discharge case in the utilized process.

Keywords electrostatic discharge (ESD), power-rail ESD clamp circuit, detection mechanism, transient-noise immunity, false triggering, transmission line pulsing (TLP) test

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1 Introduction

On-chip electrostatic discharge (ESD) protection design is one of the most important reliability concerns for integrated circuits [1]. Power-rail ESD clamp circuits are indispensable elements for the whole-chip ESD protection strategy [2–15]. Transient-triggered power-rail ESD clamp circuits often utilize the resistor-capacitor (RC) network to distinguish ESD events from normal power-up pulses [2–12]. The fundamental design concern of transient-triggered circuits is to ensure the full active on state of the clamp device in ESD conditions while employing reduced RC time constants [2]. Feedback techniques, dual trigger paths and the capacitance-boosting technique provide efficient solutions towards the fundamental design concern [3–12]. However, transient-noise immunity remains an inevitable design challenge for transient-triggered circuits [3]. Specifically, both the false-triggering and transient induced latch-up (TLU) issues are important aspects of transient-noise immunity and these issues may cause enormous power consumptions in normal operation conditions [4,5]. Static-triggered power-rail ESD clamp circuits

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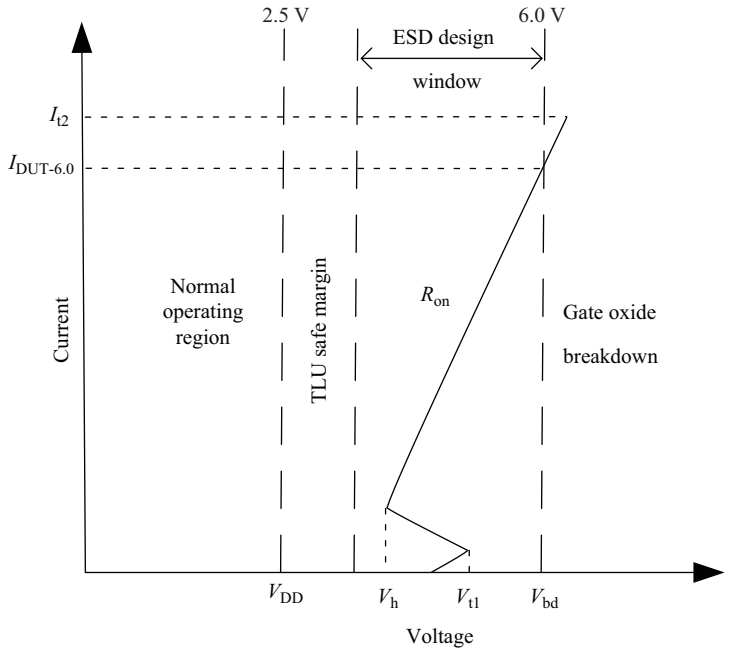

Figure 1 ESD design window concerning the utilized process in this work.

often utilize the resistor and diode string network to detect electrical overstress (EOS) events on power lines [13–15]. By employing the voltage-level sensitive detection mechanism, static-triggered circuits have superior transient-noise immunity over transient-triggered ones [15]. This superiority can be further analyzed: in case the concerned transient noise has the same transient feature with the orientated ESD events, transient-triggered circuits would mostly respond to this noise regardless of the response time being short or long. While for static-triggered circuits, they are theoretically immune to all transient noises whose peak voltages are lower than their triggering voltages (V_{t1}). The main design concern of static-triggered circuits is to obtain reduced V_{t1} levels for prompt reactions towards ESD events while maintaining acceptable leakage current (I_{leak}) in normal operation conditions [15]. Regarding the footprint compactness of power-rail ESD clamp circuits, the silicon-controlled rectifier (SCR) can be utilized as the main clamp device [1]. However, the discharge behavior of the SCR is process and layout-parameter dependent, which is beyond the simulation scope of SPICE models [1].

Base on the above concerns, a novel static-triggered power-rail ESD clamp circuit is proposed. The proposed circuit incorporates a thyristor delay stage into its trigger circuit (TC) to obtain an enhanced ESD-conduction behavior relative to that of the traditional static-triggered circuit [4,13]. Figure 1 depicts the ESD design window in this work based on transmission line pulsing (TLP) test results [16]. We utilized a 65-nm CMOS process to conduct this study. Input/output (I/O) devices with a normal V_{DD} of 2.5 V are employed to construct different power-rail ESD clamp circuits. To ensure the safety of the most fragile gate oxide in the utilized process, 6.0 V (V_{bd} in Figure 1) is taken as the upper voltage boundary of the ESD design window. V_h, R_{on}, I_{t2} in Figure 1 represent the holding voltage, on-resistance and second breakdown current of the concerned ESD protection cell, respectively. $I_{DUT-6.0}$ stands for current of the device under test (DUT) at the clamping voltage (V_c) of 6.0 V and this parameter is the evaluation of the protection efficiency considering the worst discharge case. Due to the improved static control methods and increased ESD protection cost in advanced processes, the industry has recommended lowering the human body model (HBM) ESD protection level from 2 kV to 1 kV [17]. Considering the worst discharge case, $I_{DUT-6.0}$ should exceed 0.67 A to meet the recommended 1 kV HBM level [1,17]. Direct current (DC), TLP, turn-on verification and HBM tests are executed to fully evaluate the performance of investigated circuits. Through the full evaluation, the proposed circuit achieves the best ESD-conduction behavior and lowest I_{leak} at the normal bias voltage (2.5 V) among all investigated circuits in this work, which presents an efficient on-chip ESD protection scheme considering the worst discharge case in the utilized

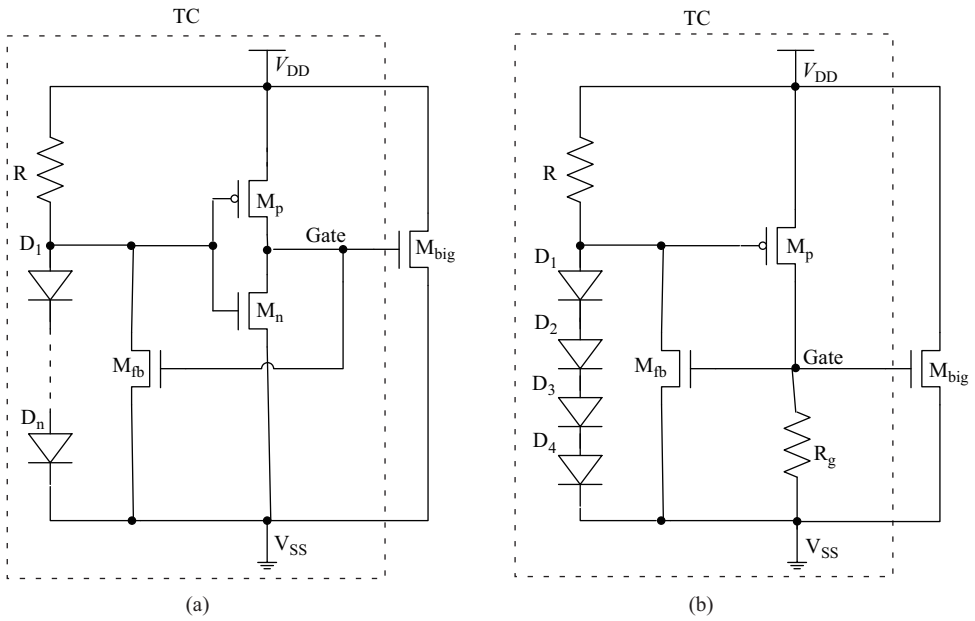

Figure 2 (a) The traditional static-triggered power-rail ESD clamp circuit and (b) the proposed power-rail ESD clamp circuit.

Table 1 Device parameters of investigated circuits in this work

Circuit type	R (kΩ)	R_g (kΩ)	D_n (area)	M_p (W/L)	M_n (W/L)	M_{fb} (W/L)	M_{big} (W/L)
DC with *n*-diode	21.2	N/A	4 μm^2	8.0 μm/0.5 μm	4.0 μm/0.5 μm	1.8 μm/7.0 μm	1280.0 μm/0.28 μm
Proposed circuit	21.2	13.0	4 μm^2	8.0 μm/0.5 μm	N/A	1.0 μm/8.0 μm	1280.0 μm/0.28 μm

process. Additionally, the proposed circuit is immune to false-triggering issues under power-up pulses with their rise-times ranging from 5 ns to 100 μs.

2 Pre-silicon design of investigated power-rail ESD clamp circuits

Figure 2 depicts the traditional static-triggered and the proposed power-rail ESD clamp circuits. Regarding the traditional static-triggered circuit (abbreviated as DC circuit with *n*-diode) in Figure 2(a) [13], its V_{t1} can be directly adjusted by changing the diode number. Reduced V_{t1} levels, which are beneficial for the promotion of the ESD-conduction behavior and the ESD-reaction speed, can be directly realized by employing fewer diodes. However, I_{leak} at 2.5 V would be seriously degraded with reduced diodes in Figure 2(a). DC circuits with diode numbers of 2, 3 and 4 are investigated in this work to confirm the aforementioned design tradeoff.

Simulation and test results exhibited later will reveal that I_{leak} at 2.5 V of only the DC circuit with 4-diode is acceptable for practical applications among all investigated DC circuits in Figure 2(a). In order to enhance the ESD-conduction behavior of static-triggered circuits while maintaining an acceptable I_{leak} at 2.5 V, a novel static-triggered power-rail ESD clamp circuit employing 4-diode is proposed in this work as depicted in Figure 2(b). The traditional inverter is replaced by a thyristor delay stage in the proposed circuit. With the absence of the pull-down M_n transistor in the proposed circuit, a better logic-high voltage can be delivered to Gate node in Figure 2(b) compared with those in Figure 2(a) in an EOS state in case R_g is properly sized. Besides, R_g also provides a DC path to ground for Gate node in normal operation conditions. Device parameters of investigated circuits optimized under the aforementioned design concerns are presented in Table 1.

The utilized diodes for all investigated circuits in this work are of the p+/n-well type. Unlike transient-triggered circuits whose feedback transistors have to be sized relatively wide to combat the *RC* time-out effect [3,4], feedback transistors (M_{fb}) have relatively narrow dimensions in this work as depicted in

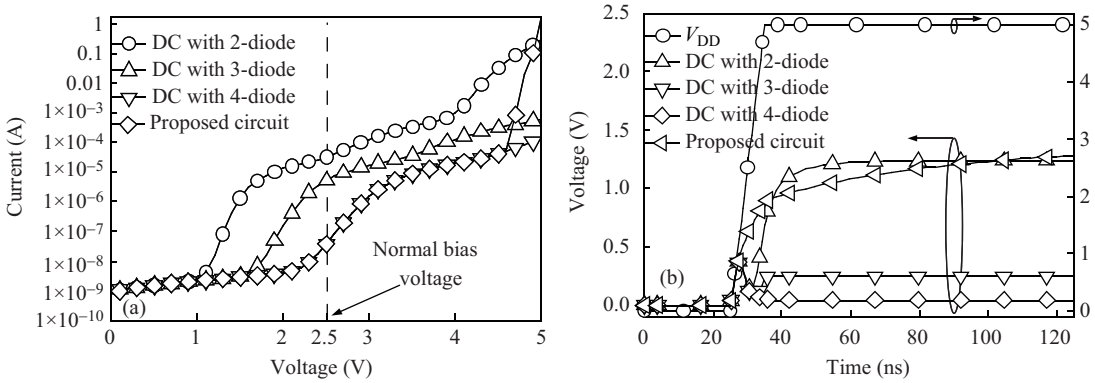

Figure 3 (a) DC simulation results for all investigated circuits and (b) ESD-like transient simulation results for all investigated circuits.

Table 1 with the absence of the *RC* detection network in static-triggered circuits. The narrow dimensions of M_{fb} are additional factors that enhance transient-noise immunity of static-triggered circuits over transient-triggered ones, especially with respect to TLU issues [5]. DC and ESD-like transient simulation results for all investigated circuits are depicted in Figure 3. In DC simulations in Figure 3(a), voltage sweeps are performed on V_{DD} lines and currents drawn by different circuits are plotted. The adjustability of V_{t1} for DC circuits with different diode numbers can be confirmed in Figure 3(a). Moreover, I_{leak} at 2.5 V of DC circuits with 2 and 3 diodes is unacceptable for practical applications. The proposed circuit consumes almost the same I_{leak} at 2.5 V with the DC circuit with 4-diode while its triggering behavior in Figure 3(a) is the steepest, confirming the performance superiority of the proposed circuit over other DC circuits. In ESD-like transient simulations in Figure 3(b), a transient pulse with a rise-time of 10 ns and peak voltage of 5.0 V is simulated on V_{DD} lines and gate voltages of M_{big} in different circuits are plotted. Peak gate voltages of M_{big} of the proposed circuit and the DC circuit with 2-diode are almost the same in Figure 3(b), which are much higher than those of other DC circuits, confirming the better logic-high voltage at Gate node delivered by the thyristor delay stage in Figure 2(b) compared with those delivered by the traditional inverter. This better logic-high voltage at Gate node will result in an enhanced ESD-conduction behavior through an enlarged trans-conductance of M_{big}.

Since the performance superiorities of the proposed circuit over the traditional static-triggered circuit have been preliminarily confirmed in Figure 3, it makes sense to characterize the performance of the proposed circuit under both fast and normal power-up conditions and the corresponding simulation results are depicted in Figure 4. It is noteworthy that simulation setups between Figure 3(b) and Figure 4 are almost identical. The only difference is the transient pulse applied on the V_{DD} line. In the fast power-up simulation in Figure 4(a), V_{DD} has a rise-time of 10 ns and peak voltage of 2.5 V. The peak gate voltage of M_{big} in Figure 4(a) stays below its threshold voltage (around 0.6 V), indicating the false-triggering immunity of the proposed circuit against this fast power-up pulse. For previously reported transient-triggered circuits in [2–12], the false-triggering immunity against fast power-up pulses with rise-times on the order of 100 ns has been extremely nice. In this work, it is shown that by utilizing the static ESD detection mechanism, the proposed circuit is immune to the fast power-up pulse with a rise-time as fast as that of an ESD event, achieving significant false-triggering immunity improvement relative to those of transient-triggered circuits.

In the normal power-up simulation in Figure 4(b) with a pulse rise-time of 100 μs and peak voltage of 2.5 V, the gate voltage of M_{big} is almost negligible in the whole simulation duration. One thing needs further clarification when comparing simulation results between Figure 4(a) and (b): gate voltage of M_{big} has a relatively much more obvious reaction in Figure 4(a) than that in Figure 4(b). This much more obvious reaction can be explained by the transient voltage coupling effect resulting from the parasitic gate-drain capacitor of M_{big} and R_g in Figure 2(b) [19]. This effect becomes negligible when rise-time of the simulated pulse becomes sufficiently slow.

In the layout design phase, M_{big} in each investigated circuit is drawn in the multi-finger style with a

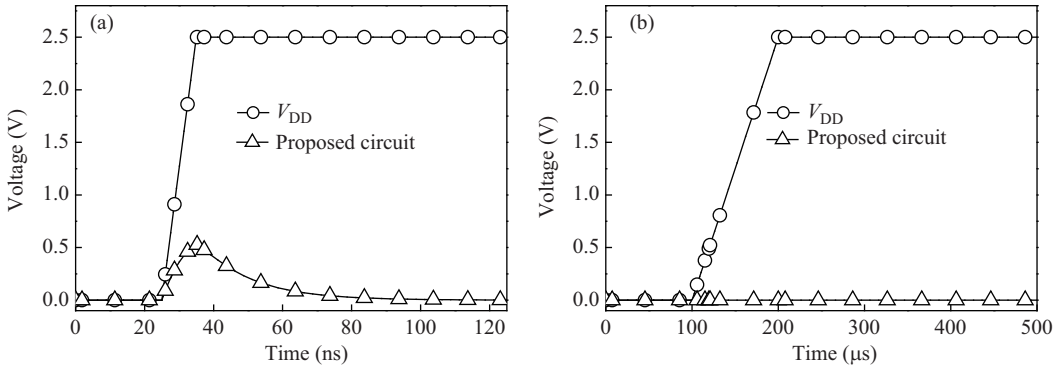

Figure 4 Power-up simulation results for the proposed circuit (a) under a fast power-up pulse with a rise-time of 10 ns and (b) under a normal power-up pulse with a rise-time of 100 μs.

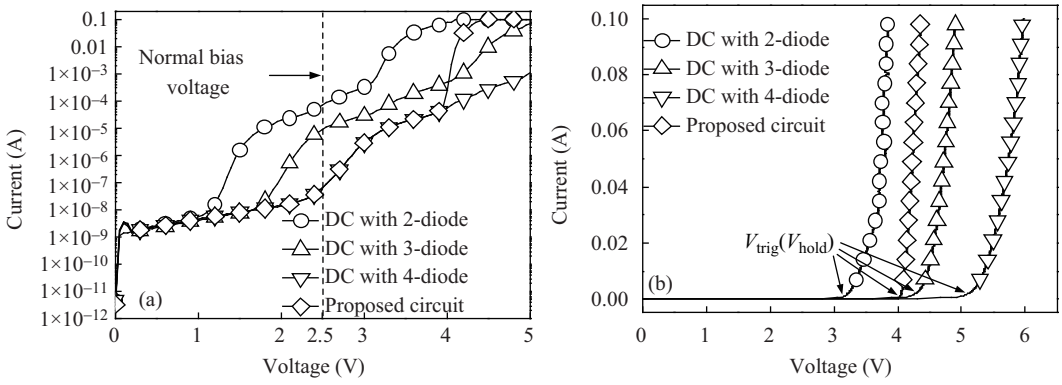

Figure 5 DC test results for all investigated circuits: (a) F-V test results and (b) F-I test results.

total finger number of 16 [18]. Silicide-blocking (SB) masks are added on drain sides of M_{big} to increase its R_{on} when driven in the active discharge mode [1]. The increased R_{on} is beneficial for on-chip ESD elements burdening less system ESD current in printed circuit board (PCB) applications with transient voltage suppressors placed in parallel [19].

3 Silicon data verification

This section covers test results and detailed discussions towards these results. Both previous analyses and simulation results will be fully confirmed in this section.

3.1 DC test results

An Agilent 4156C curve trace is employed to characterize DC performance of investigated circuits. Force-voltage (F-V) and force-current (F-I) tests are executed to extract I_{leak} at 2.5 V and to depict triggering behaviors in DC conditions, respectively.

Figure 5 depicts all executed DC test results. F-V test results in Figure 5(a) have fully confirmed simulation predictions in Figure 3(a). For F-I test results in Figure 5(b), V_{trig} and V_{hold} stand for the triggering voltage and holding voltage in DC conditions respectively, which are different from V_{t1} and V_h defined in Figure 1. All investigated circuits exhibit no snapback behavior in Figure 5(b) due to the voltage-level sensitive detection mechanism utilized, making their V_{trig} and V_{hold} identical. The proposed circuit exhibits a reduced V_{trig} even compared with that of the DC circuit with 3-diode in Figure 5(b) while consuming almost the same I_{leak} at 2.5 V with the DC circuit with 4-diode in Figure 5(a).

Table 2 summarizes DC test results in this sub-section. With all V_{hold} in Table 2 being far above 2.5 V, all investigated circuits are safe towards the static latch-up risk [20].

Table 2 Summary of DC test results for all investigated circuits

Parameter type	DC with 2-diode	DC with 3-diode	DC with 4-diode	Proposed circuit
$I_{\rm leak}$ at 2.5 V (nA)	70.9×10^3	8.9×10^3	66.0	65.0
$V_{\rm trig}$ (V)	3.30	4.39	5.24	4.08
$V_{\rm hold}$ (V)	3.30	4.39	5.24	4.08

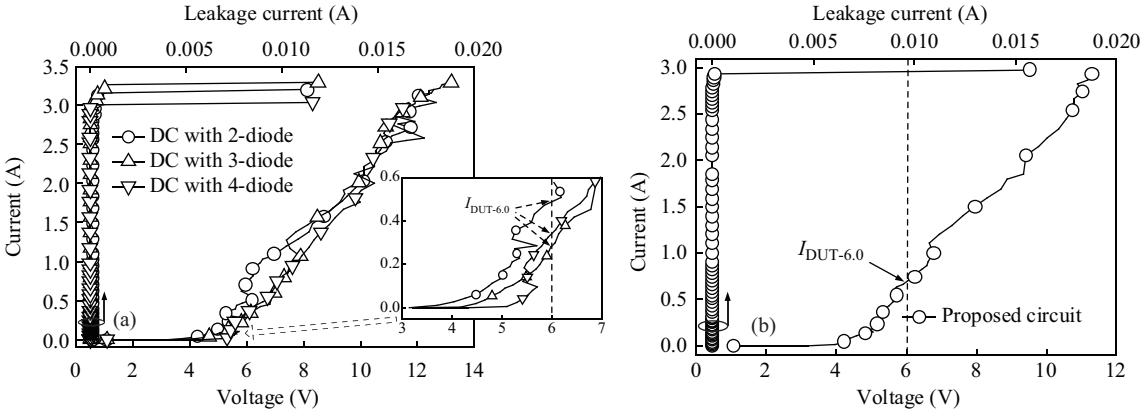

Figure 6 TLP test results for: (a) DC circuits and (**b**) the proposed circuit.

Table 3 Summary of TLP test results for all investigated circuits

Parameter type	DC with 2-diode	DC with 3-diode	DC with 4-diode	Proposed circuit
$V_{\rm t1}$ (V)	3.14	4.17	5.10	4.09
$V_{\rm h}$ (V)	3.14	4.17	5.10	4.09
$I_{\rm DUT-6.0}$ (A)	0.50	0.30	0.36	0.70
$I_{\rm t2}$ (A)	3.20	3.29	3.04	2.98

3.2 TLP test results

A Barth 4002 TLP test system is employed to generate transient pulses with the same rise-time of 10 ns and pulse width of 100-ns to mimic HBM ESD events [21]. Failure is judged by the significant shift of the post $I_{\rm leak}$ relative to the initial $I_{\rm leak}$ after each transient pulse is applied to the DUT. Figure 6 depicts TLP test results for all investigated circuits.

For TLP test results in Figure 6(a), all curves exhibit multiple minor snapbacks due to the inefficiency of corresponding TCs. The adjustability of $V_{\rm t1}$ by utilizing different diode numbers is again confirmed in the inset of Figure 6(a). However, none of the $I_{\rm DUT-6.0}$ exhibited in Figure 6(a) exceeds 0.67 A. The proposed circuit achieves the fewest minor snapbacks in Figure 6(b) compared with those in Figure 6(a), confirming the validity of the optimization effort on its TC. Further, $I_{\rm DUT-6.0}$ of the proposed circuit can well exceed 0.67 A due to the enhanced ESD-conduction behavior relative to those of DC circuits. All circuits are free from TLU issues with their $V_{\rm h}$ exhibited in Figure 6 being far above 2.5 V [22].

$R_{\rm on}$ of each investigated circuit is relatively large in Figure 6 compared with other pure component-level orientated designs [2–15], confirming the validity of the utilized SB layout strategy for on-chip ESD elements burdening less system ESD current in PCB applications.

Table 3 summarizes TLP test results in this sub-section. There might be over-estimations for $I_{\rm t2}$ of DC circuits with 2 and 3 diodes as their initial $I_{\rm leak}$ levels at 2.5 V are very high as depicted in Figure 5(a). Finally, it can be concluded in Table 3 that the proposed circuit is able to provide an efficient on-chip ESD protection scheme considering the worst discharge case in the utilized process.

3.3 Turn-on verification test results

A three-terminal test method presented in [12] is employed in this work to characterize turn-on behavior of the proposed circuit with respect to different transient pulses. In the three-terminal test method, the

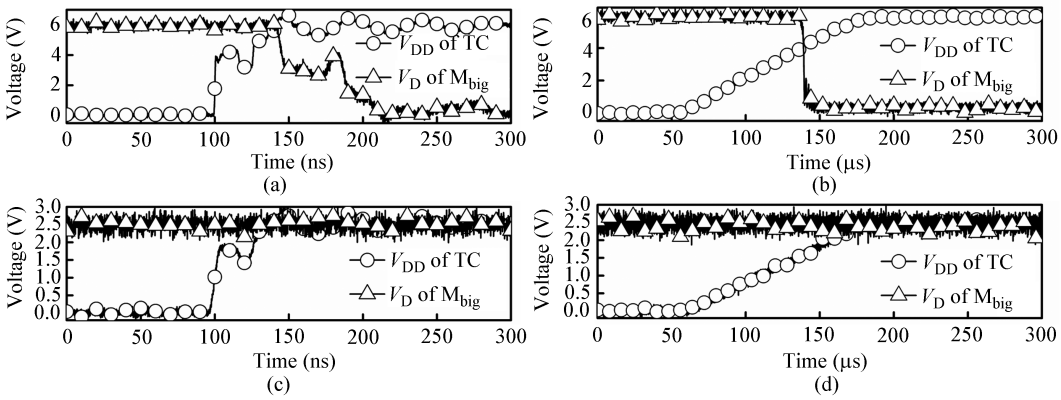

Figure 7 Turn-on verification test results for the proposed circuit under different transient pulses on V_{DD} of TC with: (a) 5-ns rise-time and 6.0-V peak voltage, (b) 100-μs rise-time and 6.0-V peak voltage, (c) 5-ns rise-time and 2.5-V peak voltage and (d) 100-μs rise-time and 2.5-V peak voltage.

Table 4 HBM test results for all investigated circuits

	DC with 2-diode	DC with 3-diode	DC with 4-diode	Proposed circuit
HBM level (kV)	5.25	5.25	5.25	5.25

drain terminal of M_{big} is separated from V_{DD} of TC in Figure 2(b). An arbitrary waveform generator generates transient pulses with various rise-times and peak voltages to drive V_{DD} of TC while a DC power supply drives the drain terminal of M_{big} through a current-limiting resistor with a resistance of 100 Ω. The DC power supply voltage (V_{DC}) is set to the peak level of the transient pulse on V_{DD} of TC. Both V_{DD} of TC and drain voltage (V_D) of M_{big} are captured to observe the triggering action. Initially, V_D of M_{big} stays close to V_{DC} as the impedance of M_{big} in the off state is infinity in theory. Once the applied transient pulse meets the triggering criterion of the TC, V_D of M_{big} will fall from an initial level of around V_{DC} to a low level determined by R_{on} of M_{big}, forming an obvious signature of the triggering action. Figure 7 depicts test results in this sub-section.

The concerned rise-times of applied pulses on V_{DD} of TC include 5 ns and 100 μs in correspondence with the simulation stimuli in Figure 4. The discrepancy of the 5-ns rise-time from the simulated 10-ns rise-time is due to the consideration that the real rising edge may be slowed down due to the existence of parasitic capacitors or impedance mismatch in the real test environment. In addition, the concerned peak voltages of applied pulses on V_{DD} of TC include 2.5 V and 6.0 V, which is supposed to cover both the normal V_{DD} and the upper voltage boundary defined in Figure 1.

Test results in Figure 7 have fully confirmed previous simulations in Figures 3 and 4. Regardless of the rise-time of the applied transient pulse, the proposed circuit would be triggered in case the transient stimulus has a peak voltage above the corresponding V_{t1}. Similarly, the proposed circuit is immune to power-up pulses with both fast and slow rise-times as long as their peak voltages keep the same at the normal V_{DD} level.

3.4 HBM test results

A Thermo Key Tek Zapmaster 7/4 is utilized to evaluate HBM robustness of investigated circuits [23,24]. The initial HBM stress voltage and minimum increase step of the HBM stress voltage are both 250 V [24]. Over 30% post DC *I*-*V* curve shift from the initial curve is taken as the failure criterion. Table 4 presents HBM test results for all investigated circuits.

A same HBM level of 5.25 kV is achieved by all investigated circuits, which is due to the same clamp device utilized. In addition, this same HBM level confirms the I_{t2} over-estimations of DC circuits with 2 and 3 diodes discussed previously.

3.5 Discussion

While test results have been fully presented, a few more issues need further clarifications such that more insightful implications of these test results can be obtained.

The SB layout strategy has been successfully adopted to increase $R_{\rm on}$ of $\rm M_{big}$ in this work. While the benefit of the increased $R_{\rm on}$ has been clearly clarified, it inevitably becomes more challenging to design on-chip ESD elements fitting the corresponding ESD design window with the increased $R_{\rm on}$. The proposed circuit in this work provides an efficient scheme towards this challenge by properly optimizing its TC.

While the turn-on behavior with respect to different transient pulses of only the proposed circuit is characterized in this work, the conclusion on the false-triggering immunity of the proposed circuit against fast power-up pulses is mostly valid for other static-triggered circuits. Regarding extremely fast power-up pulses with their rise-times as fast as that of an ESD event, the aforementioned transient voltage coupling effect can be attenuated by utilizing narrower clamp devices whose parasitic gate-drain capacitors have reduced capacitances. The potential risk of utilizing narrower clamp devices is the degradation of the overall $I_{\rm t2}$ or standalone HBM level.

The standalone HBM level evaluates the robustness of the ESD protection circuit itself. For the evaluation of the protection efficiency in the utilized process, $I_{\rm DUT\text{-}6.0}$ is the appropriate parameter. Efficient ESD protection schemes should firstly be self-robust enough, in the meantime, ensure the safety of the device to be protected. Hence, both the HBM level and $I_{\rm DUT\text{-}6.0}$ concerned in this work are necessary parameters for the full evaluation of an efficient ESD protection scheme.

4 Conclusion

Based on the superior transient-noise immunity of the static ESD detection mechanism over the transient one, a novel static-triggered power-rail ESD clamp circuit is proposed in this work. By the proper optimization on the trigger circuit, the proposed circuit is experimentally verified to exhibit superior performance over the traditional static-triggered circuit. In addition, the proposed circuit provides an efficient on-chip ESD protection scheme considering the worst discharge case in the utilized process. Moreover, the excellent false-triggering immunity of the proposed circuit against fast power-up pulses is fully confirmed by the turn-on verification test. Finally, the optimization process of the proposed circuit presented in this work provides an insightful reference for other efficient power-rail ESD clamp circuit designs.

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Conflict of interest The authors declare that they have no conflict of interest.

References

1 Amerasekera A, Duvvury C, Anderson W, et al. ESD in Silicon Integrated Circuits. 2nd ed. Chichester: John Wiley & Sons, Ltd, 2002
2 Ker M D. Whole-chip ESD protection design with efficient VDD-to-VSS ESD clamp circuits for submicron CMOS VLSI. IEEE Trans Electron Devices, 1999, 46: 173–183
3 Smith J, Cline R, Boselli G. A MOSFET power supply clamp with feedback enhanced triggering for ESD protection in advanced CMOS technologies. In: Proceedings of Electrical Overstress/Electrostatic Discharge Symposium, Las Vegas, 2003. 1–9
4 Sarbishaei H, Semenov O. A transient power supply ESD clamp with CMOS thyristor delay element. In: Proceedings of Electrical Overstress/Electrostatic Discharge Symposium, Anaheim, 2007. 395–402
5 Ker M D, Yen C C. Investigation and design of on-chip power-rail ESD clamp circuits without suffering latchup-like failure during system-level ESD test. IEEE J Solid-State Circ, 2008, 43: 2533–2545

6 Wang Y, Zhang L, Cao J, et al. Research on electrostatic discharge characteristics of tunnel field effect transistors. Acta Phys Sin, 2014, 63: 178501
7 Li J J, Gauthier R, Mitra S, et al. Design and characterization of a multi-RC-triggered MOSFET-based power clamp for on-chip ESD protection. In: Proceedings of Electrical Overstress/Electrostatic Discharge Symposium, Anaheim, 2006. 179–185
8 Zhang L, Wang Y, Lu G, et al. A novel diode string triggered gated-PiN junction device for electrostatic discharge protection in 65 nm CMOS technology. Chin Phys B, 2015, 24: 000001
9 Liu H X, Yang Z N, Li L, et al. A novel ESD power supply clamp circuit with double pull-down paths. Sci China Inf Sci, 2013, 56: 102401
10 Lu G Y, Wang Y, Cao J, et al. Design and verification of a novel multi-RC-triggering power clamp circuit for on-chip ESD protection. In: Proceedings of Electrical Overstress/Electrostatic Discharge Symposium, Las Vegas, 2013. 56–62
11 Altolaguirre F A, Ker M D. Aea-efficient ESD clamp circuit with capacitance-boosting technique to minimize standby leakage current. IEEE Trans Device Mater Reliab, 2015, 15: 156–162
12 Wang Y, Lu G Y, Guo H B, et al. Area-efficient transient power-rail ESD clamp circuit with mis-triggering immunity in a 65-nm CMOS process. Sci China Inf Sci, in press, 2016. doi:10.1007/s11432-015-5398-3
13 Young W, Croft G. Schmitt Triggered-Configured ESD Protection Circuit. U.S. Patent 5978192. 1999
14 Ker M D, Chen T, Wang T, et al. On-chip ESD protection design by using polysilicon diodes in CMOS process. IEEE J Solid-State Circ, 2001, 36: 676–686
15 Altolaguire F A, Ker M D. Power-rail ESD clamp circuit with diode-string ESD detection to overcome the gate leakage current in a 40-nm CMOS process. IEEE Trans Electron Devices, 2013, 60: 3500–3507
16 Maloney T, Khurana N. Transmission line pulsing techniques for circuit modeling of ESD phenomena. In: Proceedings of Electrical Overstress/Electrostatic Discharge Symposium, Minneapolis, 1985. 49–54
17 Industry Council on ESD Target Levels. White Paper 1: a case for lowering component level HBM/MM ESD specifications and requirements. 2nd ed. 2010
18 Lu G Y, Wang Y, Zhang L Z, et al. Investigation on the layout strategy of ggNMOS ESD protection devices for uniform conduction behavior and optimal width scaling. Sci China Inf Sci, 2015, 58: 042402
19 Industry Council on ESD Target Levels. White paper 3—system level ESD, part I: Common misconceptions and recommended basic approaches. 1st ed. 2010
20 JEDEC Standard. IC latch-up test. JESD78D. http://www.jedec.org. 2011
21 Barth electronics. BARTH model 4002 TLP+ ^{TM}specifications. http:// barthelectronics.com
22 Ker M D, Hsu S. Transient-Induced Latchup in CMOS Integrated Circuits. New York: Wiley, 2009
23 JEDEC Standard. Electrostatic discharge (ESD) sensitivity testing, human body model (HBM). JESD22-A114F. http://www.jedec.org. 2007
24 Thermo Fisher Scientific. Key Tek zapmaster series 7: performance specifications. http://www.thermofisher.com