SCIENCE CHINA
Information Sciences

• RESEARCH PAPER •
Special Focus on All Optical Networks

October 2016, Vol. 59 102302:1–102302:17
doi: 10.1007/s11432-016-0326-1

Designs of low insertion loss optical router and reliable routing for 3D optical network-on-chip

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Received June 3, 2016; accepted July 13, 2016; published online September 9, 2016

Abstract Three-Dimensional Optical Network-on-Chip (3D ONoC) has recently emerged as a high-performance on-chip communication solution; however, owing to the intrinsic characteristics of photonic devices in existing 3D ONoC, the insertion loss caused by undesirable coupling among optical signals degrades network performance. Considering manufacturing defects and unpredictable noise sources that cause the failure of Optical Routers (ORs) in 3D ONoC, previous work simply abandoned the disabled OR when computing the restore path. In this paper, we propose a new OR structure that reduces insertion loss, and we present the design of a novel adaptive routing algorithm, FTRA-BL, based on the new OR structure with bidirectional waveguides, without abandoning any disabled ORs. Our FTRA-BL selects the normal waveguide in the disabled OR as the backup link so that the best macroscopic restore path can be guaranteed. Simulation results show that our method performs better than previous work in improving transmission reliability and latency.

Keywords 3D ONoC, low insertion loss, reliable routing, bidirectional waveguide, low latency

Citation Guo P X, Hou W G, Guo L. Designs of low insertion loss optical router and reliable routing for 3D optical network-on-chip. Sci China Inf Sci, 2016, 59(10): 102302, doi: 10.1007/s11432-016-0326-1

1 Introduction

As the scale of transistors enters the nanometer level, hundreds or even thousands of cores will be integrated on a single chip in the near future. For such a multi-core system, traditional Network-on-Chip (NoC), which uses metal interconnections, faces many issues concerning limited bandwidth provisioning, low transmission speed, and unacceptable energy consumption [1]. With an increasing number of processing elements on the chip, this situation will become more serious. Fortunately, Optical NoC (ONoC) [1–10] was proposed for solving the current problems and challenges of NoC. As an emerging communication architecture for many-core systems, ONoC can potentially offer high communication bandwidth, low latency, and high energy efficiency. Furthermore, the employment of Wavelength Division Multiplexing (WDM) technology in ONoC can further boost the bandwidth in optical interconnects by simultaneously transmitting many optical signals on different waveguides in parallel on a signal transmission line.

The design of topology and router structures is the basis of ONoC. Currently, a list of ONoC topologies and Optical Router (OR) structures have been proposed based on optical waveguides and Microring Resonators (MRs) [1–6]; however, because of the intrinsic characteristics of photonic devices in existing

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ORs, the power loss caused by undesirable coupling among optical signals will introduce insertion loss and degrade Signal-to-Noise Ratio (SNR). Though some efforts have been made to analyze the insertion loss in ONoC [7–9], all of them were restricted to 2D structures, and could not establish an effective mathematical model to analyze insertion loss. In addition, the router structure is not optimal.

Furthermore, manufacturing defects and unpredictable noise sources (e.g., an unexpected increase in cross-coupling between interconnects) may result in glitches and delay effects, causing logic errors and chip faults. As the OR is the core component that affects transmission efficiency and accuracy, the tolerance of OR faults becomes urgent. According to [11], the OR fault can be divided into static and dynamic types. The static OR faults appear when the system is powered on, while the dynamic OR failures appear randomly during the operation of the system. As for OR-fault tolerant methods, previous reliability solutions can be divided into two types: deterministic reliable routing and adaptive reliable routing [12–14]. Deterministic reliable routing always uses a fixed restore path, which results in long transmission latency and poor transmission quality. The adaptive reliable routing algorithm [15] selects the restore path based on the current status of the system. Unfortunately, previous adaptive reliable routing algorithms completely abandoned disabled ORs during the process of computing the restore path, which causes an increase in routing hops and poor transmission quality.

To solve the problem above, in this paper, we first present our design for the optimal OR structure, then analyze the insertion loss and scalability at the optical switch level, router level, and network level for our ONoC architecture and other architectures proposed in [2] and [3]. Finally, we propose a fine-grained OR-fault model. We confine the fault granularity into the internal part of an OR when we perform our adaptive reliable routing to tolerate OR faults. Correspondingly, a novel Fault-Tolerant Routing Algorithm based on Bidirectional waveguide Link (FTRA-BL) is designed for 3D ONoC. When the fault of an intra-OR waveguide occurs, FTRA-BL utilizes the normal waveguide in the disabled OR as the backup link of the optimal path, instead of rerouting packets along the sub-optimal restore path detouring around disabled OR(s). Thus, the best macroscopic path along with the least number of ORs and the weakest degradation of transmission performance can be guaranteed. In summary, the main contributions of this paper are the following:

• We propose a new OR structure and establish an effective analysis model of insertion loss. Compared with the 7×7 OR in 3D mesh [2] and the OR in 3D torus [3] (referred to as Method-1 and Method-2, respectively in later sections), our new OR structure in 3D torus topology reduces the best-, worst- and average-case router-level insertion loss by 10.28%, 54.45%, and 41.89% for Method-1, and 0%, 21.15%, and 3.3% for Method-2, respectively. Moreover, it reduces the network-level insertion loss by 44.9%, 51.18%, 56.98%, 58.89%, 61.64%, 62.99%, 64.73%, and 65.56% for Method-1, and 10.26%, 15.94%, 9.72%, 10.86%, 6.87%, 11.52%, 5.84%, and 10.07% for Method-2 with network sizes of $3 \times 3 \times 3$, $4 \times 4 \times 3$, $5 \times 5 \times 3$, $6 \times 6 \times 3$, $7 \times 7 \times 3$, $8 \times 8 \times 3$, $9 \times 9 \times 3$, and $10 \times 10 \times 3$, respectively.

• Based on our novel OR structure with bidirectional waveguide links in 3D torus ONoC topology, we design a novel adaptive reliable routing algorithm called FTRA-BL that utilizes the bidirectional waveguides in disabled ORs as backup resources, which can achieve an improvement ratio of insertion loss up to 58.1% for a single OR fault, 59.48% for two OR faults, and 96.8% for three OR faults and can achieve an improvement ratio of transmission latency up to 13.7% for a single OR fault, 17.6% for two OR faults, 21.2% for three OR faults, and 24.5% for four OR faults.

The rest of this paper is organized as follows: Section 2 introduces two types of ONoC topologies, 3D mesh and 3D torus, and their OR structure; we propose the new OR structure and present the analysis of insertion loss and scalability at different levels in Section 3; our fault-tolerant method and adaptive reliable routing algorithm are described in Section 4; and finally, we conclude this paper in Section 5.

2 3D ONoC topology and OR architecture

As the most effective interconnection pattern for multicore systems, 3D ONoCs [2, 3] based on photonic and 3D integration techniques potentially offer high communication bandwidth, low latency, and high

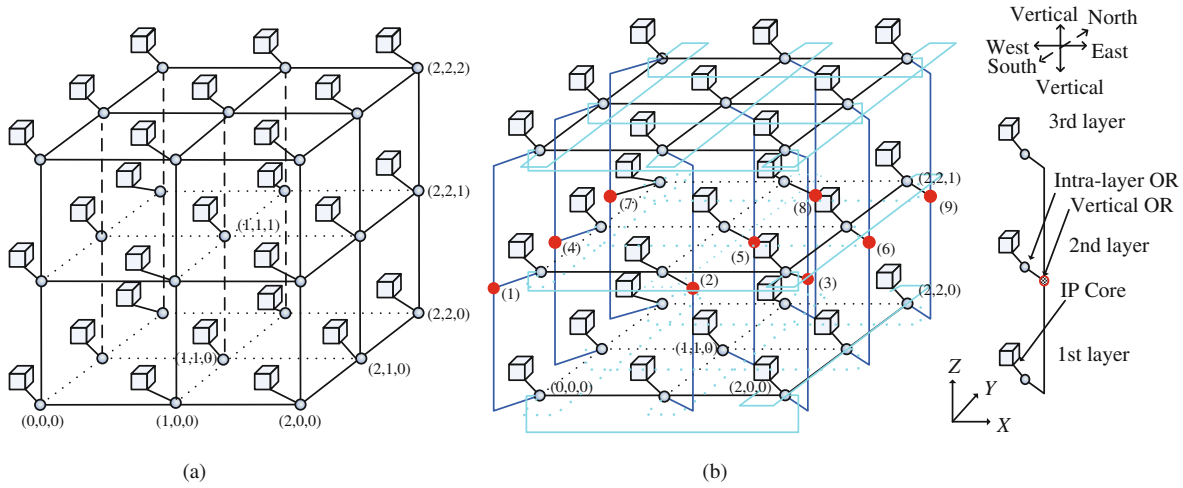

Figure 1 (Color online) Topology structures. (a) 3D mesh topology structure; (b) 3D torus topology structure.

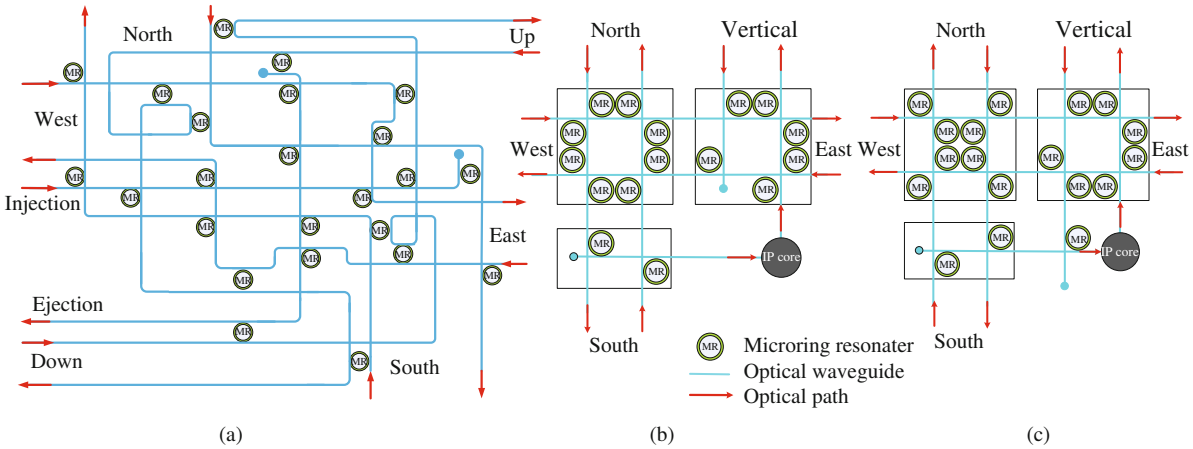

Figure 2 (Color online) OR structures. (a) OR structure in [2]; (b) OR structure in [3]; (c) OR structure in this paper.

energy efficiency. Ref. [2] proposed the 3D mesh ONoC topology shown in Figure 1(a). It has three layers, each of which is a standard 2D mesh with three rows and three columns. Each row and each column has three ORs to implement the packet transmission, and every OR connects with one local 'IP Core' where the packet is generated. The ORs in different layers are directly connected through waveguides. The corresponding 7×7 OR structure is shown in Figure 2(a), and it has a total of seven ports: 'East', 'West', 'North', 'South', 'Up', 'Down' and 'Injection/Ejection'. The ports 'East', 'West', 'North', and 'South' are used for the packet transmission among adjacent ORs located in the same layer, while the ports 'Up' and 'Down' are used for the packet transmission among adjacent ORs located in different layers. Finally, the 'Injection/Ejection' port is connected with 'IP Core' for sending the packet from the local 'IP Core' to the network or receiving the packet from the network to the local 'IP Core'.

It is noteworthy that, the ORs at the network edge or corner cannot fully utilize the 7×7 optical switching function, resource and power waste will result. In addition, the average amount of routing hops will linearly grow with an increase in network size for 3D mesh topology, thus leading to a long transmission latency. In fact, compared with the 3D mesh topology, the 3D torus has more regular OR structure and shorter transmission delay owing to its loopback feature. Therefore, in our preliminary work [3], Hou et al. proposed the 3D torus ONoC topology shown in Figure 1(b). It also has three vertical layers, but the second-layer node is additionally equipped with a vertical OR. The packet can be transferred from one vertical layer to the others via vertical ORs. As a result, the 3D torus topology includes intra-layer and inter-layer (vertical) ORs. The intra-layer OR structure is shown in Figure 2(b). Each intra-layer OR has six types of ports: 'East' and 'West' along the X axis, 'North' and 'South' along

the Y axis, 'Vertical' along the Z axis, and 'IP Core'. The inter-layer OR structure can be found in [3], and we will not introduce it in this paper. Both for intra- and inter-layer ORs, each type of port has an input and an output, i.e., it supports bidirectional packet transmission, and every optical waveguide between a pair of ORs in the network is bidirectional.

Based on our preliminary work, in this paper, we propose the new OR structure shown in Figure 2(c), which will further reduce insertion loss and increase the scalability of the network compared with existing structures. A detailed comparison of the three structures is discussed in the next section.

3 Insertion loss analysis

3.1 Switch-level insertion loss analysis

From Figure 2, we can see that there are four different switch elements in ORs.

• 1×2 parallel switch element: this optical switch consists of one MR and two parallel optical waveguides as shown in Figure 3(a), and it has two states: an *on* state when the signal wavelength is equal to the resonance wavelength of the MR, and an *off* state when the signal wavelength is different from the resonance wavelength. The optical signal injected to the input port will propagate directly to the through port when the MR is in the *off* state (i.e., the dotted line in Figure 3(a)) or will be coupled into the MR and then delivered to the drop port when the MR is in the *on* state (i.e., the solid line in Figure 3(a)).

• 1×2 cross switch element (near): this optical switch consists of one MR and two crossing optical waveguides as shown in Figure 3(b), and it also has an *on* and an *off* states. The optical signal injected to the input port will bypass the *off* state MR but suffer from crossing waveguides to the through port (i.e., the dotted line in Figure 3(b)), or it will be delivered to the drop port when the MR is in the *on* state without crossing waveguides (i.e., the solid line in Figure 3(b)).

• 2×2 cross switch element: this optical switch consists of two MRs and two crossing optical waveguides as shown in Figure 3(c), and it also has an *on* and an *off* states. The optical signal injected to the input port will bypass two *off* state MRs but suffer from crossing waveguides to the through port, or it will be delivered to the drop port when the MR is in the *on* state without crossing waveguides.

• 1×2 cross switch element (far): this optical switch consists of one MR and two crossing optical waveguides as shown in Figure 3(d), and it also has an *on* and an *off* states. The optical signal traveling from the input port to the through port is the same as with the 1×2 cross switch element (near); however, for the packet transmission from the input port to the drop port, as demonstrated by the solid line in Figure 3(d), it will first pass through crossing waveguides and then be coupled into the MR, and it then suffers from crossing waveguides for the second time before it arrives at the drop port. In other words, the signal will suffer from crossing waveguides twice under this case.

To analyze the exchange of optical power between waveguide and resonator, we give the geometry illustrated in Figure 4 (a)–(d) for each type of switch element. For the 1×2 parallel switch element in Figure 4(a), there are two coupling regions. According to [16], the transmission equation of the optical field for the first coupling region (coupling region 1) is as follows:

$$A_2 = t_1 A_1 + k_1 B_1, \tag{1}$$

$$B_2 = -k_1^* A_1 + t_1^* B_1. \tag{2}$$

Similar to coupling region 1, the transmission equation of coupling region 2 is as follows:

$$A_4 = t_2 A_3 + k_2 B_3, \tag{3}$$

$$B_4 = -k_2^* A_3 + t_2^* B_3, \tag{4}$$

where A_1, A_2, A_3, and A_4 are the complex mode amplitudes at the input port, through port, drop port, and add port, respectively; k_i $(i = 1, 2)$ is the coupling coefficient; t_i $(i = 1, 2)$ is the transmission

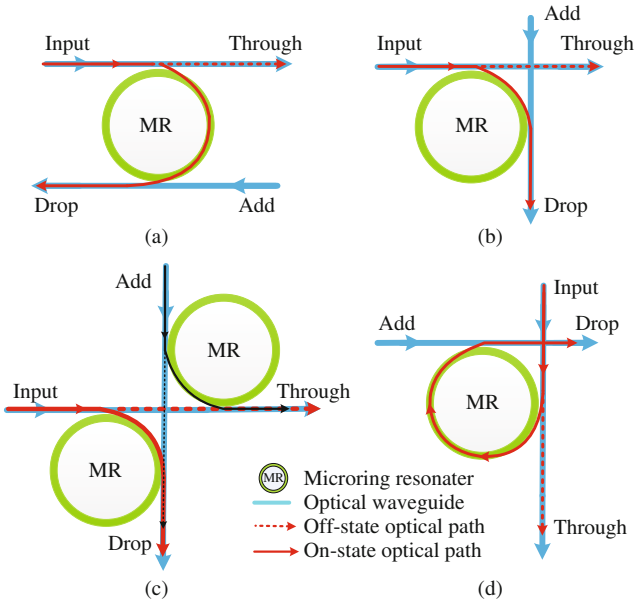

Figure 3 (Color online) (a) 1×2 parallel switch; (b) 1×2 cross switch (near); (c) 2×2 cross switch; (d) 1×2 cross switch (far); the solid line arrow denotes the on-state optical path, and dotted arrow denotes the off-state optical path.

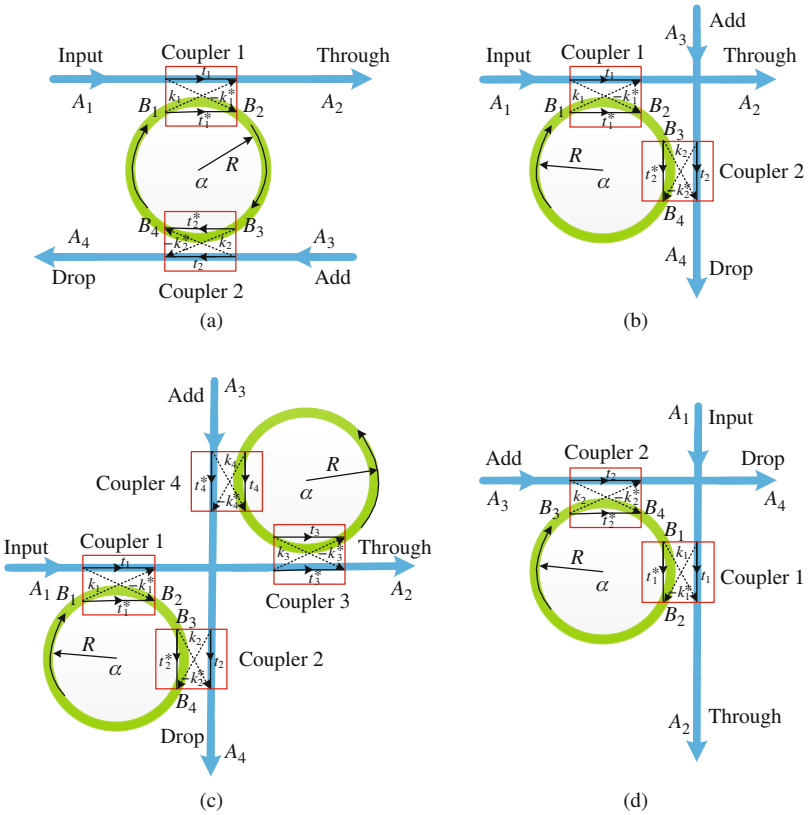

Figure 4 (Color online) (a) Model of 1×2 parallel switch; (b) model of 1×2 cross switch (near); (c) model of 2×2 cross switch; (d) model of 1×2 cross switch (far).

coefficient; and "$*$" means the conjugate relation. We assume that the coupling is lossless, thus, $|t_i|^2 + |k_i|^2 = 1$ for each coupler.

In the circular waveguide, B_1, B_2, B_3, and B_4 have the following relationship:

$$B_3 = \alpha^{\frac{1}{2}} \mathrm{e}^{\frac{\theta}{2}\mathrm{j}} B_2, \tag{5}$$

$$B_1 = \alpha^{\frac{1}{2}} \mathrm{e}^{\frac{\theta}{2}\mathrm{j}} B_4, \tag{6}$$

where α is the microring round-trip amplitude attenuation coefficient ($\alpha = 1$ means an ideal lossless); and θ is the phase delay. According to (2), (4), (5), and (6), we can deduce

$$\begin{aligned} B_1 &= \frac{A_1 k_1^* t_2^* \alpha \mathrm{e}^{\mathrm{j}\theta}}{t_1^* t_2^* \alpha \mathrm{e}^{\mathrm{j}\theta} - 1} + \frac{A_3 k_2^* \alpha^{\frac{1}{2}} \mathrm{e}^{\frac{\theta}{2}\mathrm{j}}}{t_1^* t_2^* \alpha \mathrm{e}^{\mathrm{j}\theta} - 1}, \\ B_2 &= \frac{A_1 k_1^*}{t_1^* t_2^* \alpha \mathrm{e}^{\mathrm{j}\theta} - 1} + \frac{A_3 t_1^* k_2^* \alpha^{\frac{1}{2}} \mathrm{e}^{\frac{\theta}{2}\mathrm{j}}}{t_1^* t_2^* \alpha \mathrm{e}^{\mathrm{j}\theta} - 1}, \\ B_3 &= \frac{A_1 k_1^* \alpha^{\frac{1}{2}} \mathrm{e}^{\frac{\theta}{2}\mathrm{j}}}{t_1^* t_2^* \alpha \mathrm{e}^{\mathrm{j}\theta} - 1} + \frac{A_3 t_1^* k_2^* \alpha \mathrm{e}^{\mathrm{j}\theta}}{t_1^* t_2^* \alpha \mathrm{e}^{\mathrm{j}\theta} - 1}, \\ B_4 &= \frac{A_1 k_1^* t_2^* \alpha^{\frac{1}{2}} \mathrm{e}^{\frac{\theta}{2}\mathrm{j}}}{t_1^* t_2^* \alpha \mathrm{e}^{\mathrm{j}\theta} - 1} + \frac{A_3 k_2^*}{t_1^* t_2^* \alpha \mathrm{e}^{\mathrm{j}\theta} - 1}. \end{aligned} \tag{7}$$

According to (1) and (7), we can deduce

$$A_2 = \frac{\left(t_2^* \alpha \mathrm{e}^{\mathrm{j}\theta} - t_1\right) A_1}{t_1^* t_2^* \alpha \mathrm{e}^{\mathrm{j}\theta} - 1} + \frac{k_1 k_2^* \alpha^{\frac{1}{2}} \mathrm{e}^{\frac{\theta}{2}\mathrm{j}} A_3}{t_1^* t_2^* \alpha \mathrm{e}^{\mathrm{j}\theta} - 1}. \tag{8}$$

According to (3) and (7), we can deduce

$$A_4 = \frac{k_1^* k_2 \alpha^{\frac{1}{2}} \mathrm{e}^{\frac{\theta}{2}\mathrm{j}} A_1}{t_1^* t_2^* \alpha \mathrm{e}^{\mathrm{j}\theta} - 1} + \frac{\left(t_1^* \alpha \mathrm{e}^{\mathrm{j}\theta} - t_2\right) A_3}{t_1^* t_2^* \alpha \mathrm{e}^{\mathrm{j}\theta} - 1}. \tag{9}$$

When there is no optical signal injected to the add port, i.e., $A_3 = 0$, we can simplify (8) and (9) as follows:

$$A_2 = \frac{\left(t_2^* \alpha \mathrm{e}^{\mathrm{j}\theta} - t_1\right) A_1}{t_1^* t_2^* \alpha \mathrm{e}^{\mathrm{j}\theta} - 1}, \tag{10}$$

$$A_4 = \frac{k_1^* k_2 \alpha^{\frac{1}{2}} \mathrm{e}^{\frac{\theta}{2}\mathrm{j}} A_1}{t_1^* t_2^* \alpha \mathrm{e}^{\mathrm{j}\theta} - 1}. \tag{11}$$

The power transmission to the through port and drop port can be obtained as

$$\frac{P_{\mathrm{Through}}}{P_{\mathrm{Input}}} = \left|\frac{A_2}{A_1}\right|^2 = \frac{t_1^2 - 2\alpha t_1 t_2 \cos\theta + \alpha^2 t_2^2}{1 - 2\alpha t_1 t_2 \cos\theta + \alpha^2 t_1^2 t_2^2}, \tag{12}$$

$$\frac{P_{\mathrm{Drop}}}{P_{\mathrm{Input}}} = \left|\frac{A_4}{A_1}\right|^2 = \frac{k_1^2 k_2^2 \alpha}{1 - 2\alpha t_1 t_2 \cos\theta + \alpha^2 t_1^2 t_2^2}. \tag{13}$$

Therefore, the insertion loss (dB) for the through port and drop port of a 1×2 parallel switch element can be obtained as

$$\text{Power Loss}_T\,(a) = 10 \cdot \lg\left(\frac{t_1^2 - 2\alpha t_1 t_2 \cos\theta + \alpha^2 t_2^2}{1 - 2\alpha t_1 t_2 \cos\theta + \alpha^2 t_1^2 t_2^2}\right), \tag{14}$$

$$\text{Power Loss}_D\,(a) = 10 \cdot \lg\left(\frac{k_1^2 k_2^2 \alpha}{1 - 2\alpha t_1 t_2 \cos\theta + \alpha^2 t_1^2 t_2^2}\right). \tag{15}$$

Similarly, for the 1×2 cross switch element (near) in Figure 4(b), the value of A_4 can be obtained as ($A_3 = 0$):

$$A_4 = \frac{k_1^* k_2 \alpha^{\frac{1}{4}} \mathrm{e}^{\frac{\theta}{4}\mathrm{j}} A_1}{t_1^* t_2^* \alpha \mathrm{e}^{\mathrm{j}\theta} - 1}. \tag{16}$$

In addition, the signal will pass the *off* state MR and suffer from one round of crossing waveguides to the through port. Correspondingly, the insertion loss (dB) for the through port and drop port of a 1×2 cross switch element (near) can be obtained as

$$\text{Power Loss}_T\,(b) = 10 \cdot \lg\left(\frac{t_1^2 - 2\alpha t_1 t_2 \cos\theta + \alpha^2 t_2^2}{1 - 2\alpha t_1 t_2 \cos\theta + \alpha^2 t_1^2 t_2^2}\right) - \text{Loss}_{\mathrm{wc}}, \tag{17}$$

$$\text{Power Loss}_D\,(b) = 10 \cdot \lg\left(\frac{k_1^2 k_2^2 \alpha^{\frac{1}{2}}}{1 - 2\alpha t_1 t_2 \cos\theta + \alpha^2 t_1^2 t_2^2}\right). \tag{18}$$

Table 1 Insertion loss (dB) of different cases in optical switches

	α										
Optical switch	0.950	0.955	0.960	0.965	0.970	0.975	0.980	0.985	0.990	0.995	1
1×2 Parallel through	0.0238	0.0226	0.0214	0.0202	0.0190	0.0178	0.0167	0.0155	0.0143	**0.0132**	0.0121
1×2 Parallel drop	3.4501	3.1535	2.8481	2.5332	2.2084	1.8727	1.5254	1.1656	0.7922	**0.4041**	0.0000
1×2 Cross (near) through	0.1738	0.1726	0.1714	0.1702	0.1690	0.1678	0.1667	0.1655	0.1643	**0.1632**	0.1620
1×2 Cross (near) drop	3.3387	3.0535	2.7594	2.4559	2.1422	1.8177	1.4815	1.1327	0.7704	**0.3932**	0.0000
1×2 Cross (far) through	0.1738	0.1726	0.1714	0.1702	0.1690	0.1678	0.1667	0.1655	0.1643	**0.1632**	0.1620
1×2 Cross (far) drop	3.8615	3.5535	3.2367	2.9106	2.5745	2.2277	1.8693	1.4984	1.1140	**0.7150**	0.3000
2×2 Cross through	0.1975	0.1951	0.1927	0.1904	0.1880	0.1857	0.1833	0.1810	0.1787	**0.1764**	0.1741
2×2 Cross drop	3.3387	3.0535	2.7594	2.4559	2.1422	1.8177	1.4815	1.1327	0.7704	**0.3932**	0.0000

The insertion loss (dB) for the through port and drop port of a 2×2 cross switch element can be obtained as

$$\text{Power Loss}_T\,(c) = 2 \cdot 10 \cdot \lg\left(\frac{t_1^2 - 2\alpha t_1 t_2 \cos\theta + \alpha^2 t_2^2}{1 - 2\alpha t_1 t_2 \cos\theta + \alpha^2 t_1^2 t_2^2}\right) - \text{Loss}_{\text{wc}}, \tag{19}$$

$$\text{Power Loss}_D\,(c) = 10 \cdot \lg\left(\frac{k_1^2 k_2^2 \alpha^{\frac{1}{2}}}{1 - 2\alpha t_1 t_2 \cos\theta + \alpha^2 t_1^2 t_2^2}\right). \tag{20}$$

For the 1×2 cross switch element (far) in Figure 4(d), the value of A_4 can be obtained as ($A_3 = 0$)

$$A_4 = \frac{k_1^* k_2 \alpha^{\frac{3}{4}} \mathrm{e}^{\frac{3\theta}{4}\mathrm{j}} A_1}{t_1^* t_2^* \alpha \mathrm{e}^{\mathrm{j}\theta} - 1}. \tag{21}$$

The insertion loss (dB) for the through port and drop port of 1×2 cross switch element (far) can be obtained as

$$\text{Power Loss}_T\,(d) = 10 \cdot \lg\left(\frac{t_1^2 - 2\alpha t_1 t_2 \cos\theta + \alpha^2 t_2^2}{1 - 2\alpha t_1 t_2 \cos\theta + \alpha^2 t_1^2 t_2^2}\right) - \text{Loss}_{\text{wc}}, \tag{22}$$

$$\text{Power Loss}_D\,(d) = 10 \cdot \lg\left(\frac{k_1^2 k_2^2 \alpha^{\frac{3}{2}}}{1 - 2\alpha t_1 t_2 \cos\theta + \alpha^2 t_1^2 t_2^2}\right) - 2 \cdot \text{Loss}_{\text{wc}}. \tag{23}$$

Moreover, for the packet transmission in the MR, in the aspect of the optical length, the MR resonance occurs when the optical length of the light traveling around the ring is a multiple of the wavelength. Thus, the state of MR resonance satisfies the following equation:

$$2\pi R n_{\text{eff}} = m\lambda. \tag{24}$$

In terms of the optical phase, the MR resonance occurs when the phase is a multiple of 2π. Thus, the state of MR resonance satisfies the following equation:

$$2\pi R\beta = 2\pi m, \tag{25}$$

where m is an integer, R is the radius of one MR, and we let $R = 10$ μm; n_{eff} is the effective index of the optical mode and $n_{\text{eff}} = -0.91384 \cdot \lambda + 3.86394$; and β is the propagation constant and $\theta = 2\pi\beta$. We let $|k_1|^2 = |k_2|^2 = 0.1$ [17]. The waveguide crossing is 0.15 dB [18]. For the different values of α (we choose $\alpha \in [0.95, 1]$), the insertion loss of various cases in optical switches is shown in Table 1.

From Table 1, we can see that

• With the increment of α, the insertion loss becomes small for all cases. According to the current level of the production technology, the value of α is less than 1, and it can be equal to 0.995. Hence, we determine the simulation parameters in Table 2 when $\alpha = 0.995$.

• The insertion loss of the 1×2 cross (near) through is equal to that of the 1×2 cross (far) through, and the insertion loss of the 1×2 cross (near) drop is equal to that of the 2×2 cross drop.

Table 2 Simulation parameters of insertion loss (dB)

Parameter	Value	Parameter	Value
1×2 Parallel through	0.0132	1×2 Cross (far) drop	0.7150
1×2 Parallel drop	0.4041	2×2 Cross through	0.1764
1×2 Cross (near) through	0.1632	2×2 Cross drop	0.3932
1×2 Cross (near) drop	0.3932	Waveguide crossing	0.15
1×2 Cross (far) through	0.1632	Waveguide bend	0.005

Table 3 Insertion loss (dB) of different OR structures

	OR structure in [2]	OR structure in [3]	Our OR structure
Best-case insertion loss	0.39322	0.35278	0.35278
Worst-case insertion loss	3.218	1.85882	1.4656
Average insertion loss	1.48507	0.89241	0.86296

Table 4 Hardware consumption of different OR structures

	OR structure in [2]	OR structure in [3]	Our OR structure
Number of MRs	24	16	18
Number of waveguides	8	7	7
Number of terminators	2	2	2

• For the insertion loss of the through port, which means that the MR is in the *off* state, the 1×2 parallel through performs the best while the 2×2 cross through performs the worst. For the insertion loss of drop port, which means that the MR is in the *on* state, the 1×2 cross (near) drop and the 2×2 cross drop perform the best while the 1×2 cross (far) drop performs the worst.

3.2 OR-level insertion loss analysis

Based on the above analysis, we will compare our OR structure illustrated in Figure 2(c) with other structures illustrated in Figure 2 (a) and (b) in terms of insertion loss and hardware consumption.

3.2.1 *Insertion loss*

Because the transmission paths between different port pairs within the OR result in various degrees of insertion loss, we compare the worst-case, best-case, and average insertion loss among three OR structures. The best-case insertion loss is the power loss of the shortest transmission path inside the OR, while the worst-case insertion loss corresponds to the longest transmission path inside the OR. The simulation results are in Table 3. We can see that, from the perspective of the best-case insertion loss, our OR and the OR in [3] have the same value lower than that of the OR in [2]. Both for the worst-case and average insertion loss, our OR structure has the best performance of insertion loss.

3.2.2 *Hardware consumption*

In this section, we compare the performance of three OR structures in terms of the number of consumed MRs, waveguides and terminators. The optical terminator is an important but expensive device used in the open end of the optical link. Its function is to absorb light and prevent light from returning to the transmission line. The comparative results are shown in Table 4. From Table 4, the number of consumed terminators for those ORs is the same, which means all of them have the potential of reducing the amount of utilized terminators. Furthermore, all of those ORs can passively route optical signals, which means that they do not need to turn on any MR if an optical signal travels in the same dimension through the OR, such as from the 'South' port to the 'North' port or from the 'East' port to the 'West' port.

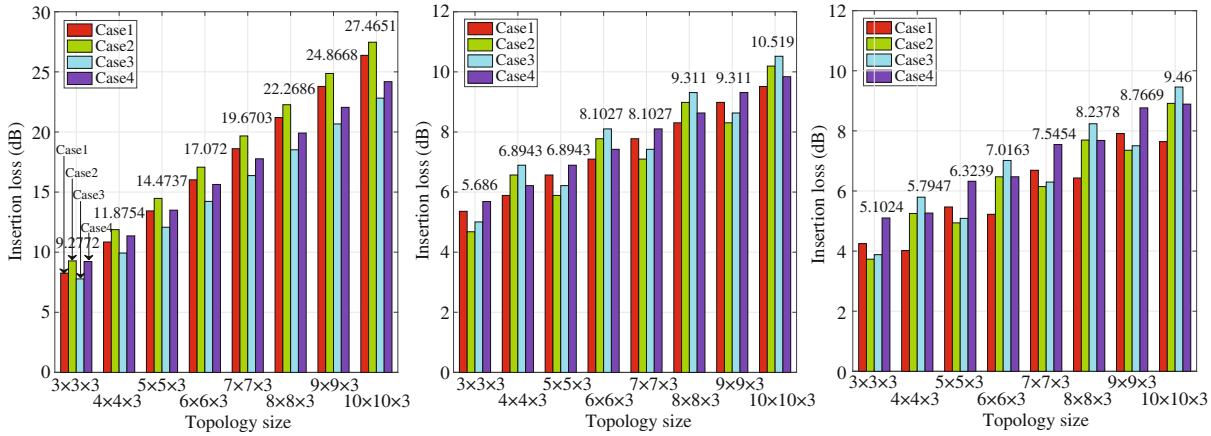

Figure 5 (Color online) Insertion loss for different OR structures each with increasing size. (a) OR structure in [2]; (b) OR structure in [3]; (c) OR structure in this paper.

3.3 Network-level insertion loss and scalability

In this section, we analyze the insertion loss in three different networks: 3D mesh topology with its 7×7 OR structure [2], 3D torus topology assorted with intra- and inter-layer OR structures [3], and 3D torus topology utilizing our OR structure. We consider only the worst-case, which plays a role in determining the complexity and scalability of the network. Under the worst-case, the source and destination are at the two points that have the longest distance. There are four cases: (case 1) destination is located in the upper right of the source; (case 2) destination is located in the upper left of the source; (case 3) destination is located in the lower left of the source; and (case 4) destination is located in the lower right of the source. For the problem of thermal shift, because there have been solutions such as integrated heaters for thermal compensation [19] and heatless devices [20], the thermal shift is neglected in our simulations. The simulation results are shown in Figure 5 when the topology size varies from $3 \times 3 \times 3$ to $10 \times 10 \times 3$. The following conclusions can be clearly seen from Figure 5:

• As the network topology scale increases, the optical signal suffers from the more serious power loss caused by crossing waveguides.

• For any topology size, the insertion loss of 3D mesh topology with its 7×7 OR structure [2] is higher compared with others, while the insertion loss of our OR structure is the lowest, e.g., even when the topology size becomes $10 \times 10 \times 3$, the insertion loss is still less than 10 dB.

• For the topology in Figure 5(a), the insertion loss of case 2 is the worst, and the insertion loss of case 3 is the best. For the topology in Figure 5 (b) and (c), when the topology size is an odd number, the insertion loss of case 4 is the worst, and that of case 2 is the best, but when the topology size is an even number, the insertion loss of case 3 is the worst, and that of case 1 is the best. Those conclusions provide important references for designing effective routing algorithms for 3D ONoCs.

Closely related to insertion loss, optical power budget of interconnects is constrained by multiple physical aspects of photonic devices [18]. According to [18], the design constraint is as follow:

$$Pb \geqslant \mathrm{IL}_{\max} + 10\log_{10} n, \tag{26}$$

where Pb is the network-level optical power budget, and $Pb = 20$ dB or $Pb = 30$ dB [18]; $\mathrm{IL}_{\max}$ is the worst-case insertion loss of the network, which can be obtained from Figure 5; and n determines the number of wavelengths that will be used for the WDM signal.

Figure 6 shows the maximum number of wavelengths that are allowed for varying topology sizes. For instance, assuming a 20 dB allowed network-level optical power budget, as shown in Figure 6(a), the number of access points for Method-1 only reaches to $7 \times 7 \times 3$, but for other OR structures, the number of access points is much larger than $10 \times 10 \times 3$. Moreover, the number of available wavelength channels for our OR structure is more than others under different topology sizes. When the network-level optical

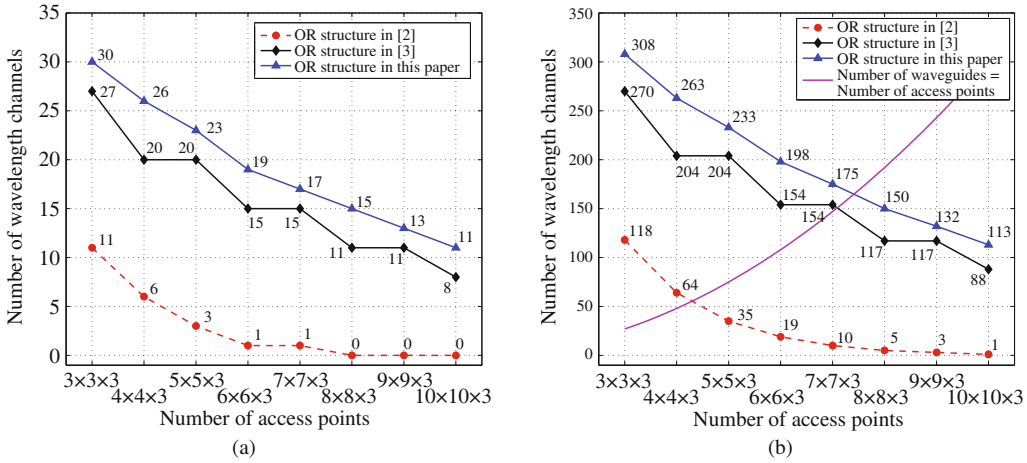

Figure 6 (Color online) Relationship between the number of access points and available wavelength channels. (a) $Pb = 20$ dB; (b) $Pb = 30$ dB.

power budget is 30 dB, as shown in Figure 6(b), the number of access points and wavelength channels are greater for our OR structure than for those of the other OR structures, which means that our OR structure has better scalability than the others. Most importantly, as shown in Figure 6(b), for our OR structure, when the number of access points is less than $7 \times 7 \times 3$, the number of available wavelength channels becomes more than the number of access points, which means that the network can achieve non-blocking packet transmission using WDM technology.

From the analysis above, we can conclude that our OR structure offers significant performance advantages over Method-1 and Method-2. Furthermore, through simple extension, our OR structure will realize fault-tolerance abilities. The details of fault-tolerant schemes, including an extended OR structure, bidirectional channel fault-tolerance mechanism, and adaptive reliable routing algorithm, are discussed in the next section.

4 Our fault-tolerant schemes for 3D ONoCs

In the Introduction, we pointed out that many factors affect the reliability of 3D ONoCs. Thus, the study of a reliable OR structure and routing policy have great practical significance. The conventional fault-tolerant OR structure and routing policy well utilize the availability of redundant routes, but abandon disable ORs during the process of computing the restore path, thus leading to the increment of routing hops and bad transmission quality. In this section, we first design a novel OR structure with bidirectional waveguide links for 3D torus ONoC topology. Next, a fine-grained OR-fault model is proposed with the help of dynamically reconfigurable bidirectional channel for fault-tolerant schemes. We confine the fault granularity into the internal part of an OR when we perform our adaptive reliable routing to tolerate OR faults.

4.1 Design of extended OR structure

In conventional OR structures, two ports communicate via a pair of single-directional waveguides, one for transmitting (TX) data and another for receiving (RX) data; however, NoC-based OR architectures cofigured with bidirectional channels, which can offer signficant performance advantages over conventional NoC-based ORs equipped with unidirectional channels, have been proposed [21,22]. Thus, in this section, we use bidirectional waveguides to replace original single-directional waveguides within the OR. Moreover, with the help of WDM technology, the intra-OR waveguide is able to transmit packets simultaneously in two different directions. In Figure 7(a), 'West' and 'East' denote two ports of the OR; meanwhile, 'Tx' and 'Rx' are the transmitter and receiver of the 'West', respectively. As we can see, if the single-directional waveguide is utilized in Figure 7(a), the data will be lost when the 'Tx' becomes disabled owing to the

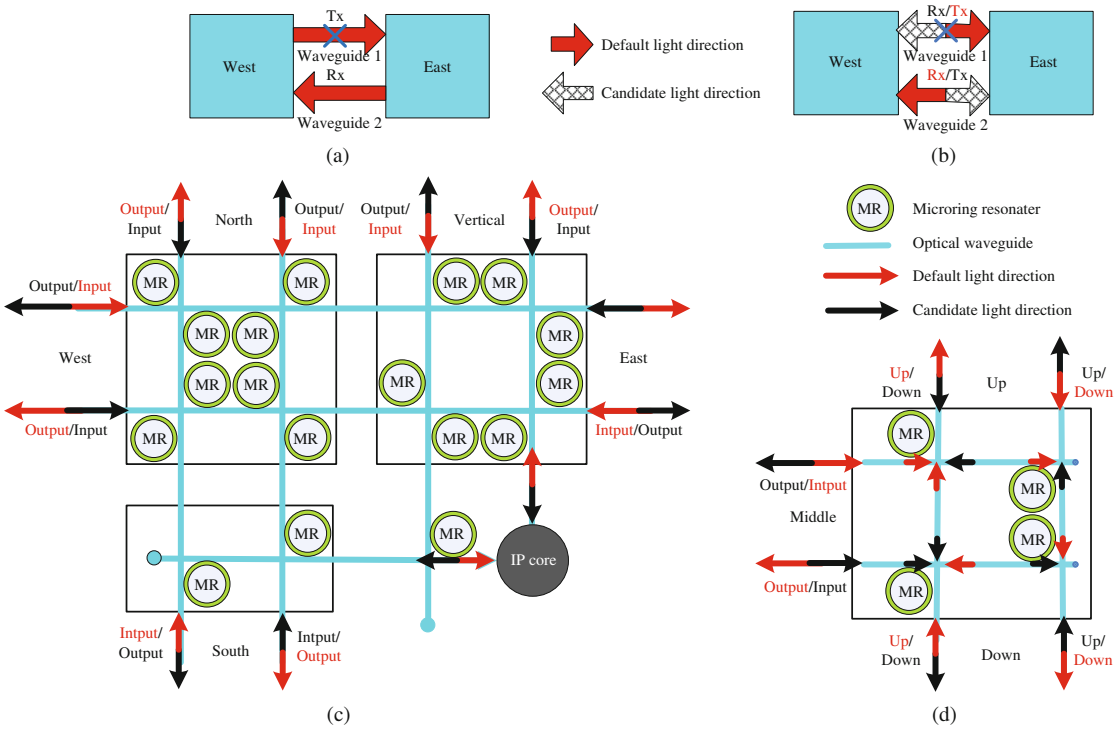

Figure 7 (Color online) (a)(b): Examples of unidirectional and bidirectional waveguides; (c)(d): extended intra- and inter-layer OR structures.

fault of waveguide 1. Using the bidirectional waveguide in Figure 7(b), the packet can still be transferred via waveguide 2 in the fault case. In this paper, we assume there has been a well-established mechanism for fault diagnosis.

Base on the analysis above, we improve the intra- and inter-layer OR structures in Figure 7(c) and Figure 7(d), respectively. We replace the single-directional waveguide with a bidirectional one (such as the bidirectional waveguide between ports 'West' and 'East' in Figure 7(b)) in the new structure. Each bidirectional waveguide has default (red arrow) and candidate (black arrow) light directions. As described in Figure 7(b), we need to make the handover from the default light direction of the disabled waveguide to the candidate light direction of the normal waveguide. To mitigate the communication conflict caused by the handover operation, we have the following definition:

Definition 1. The waveguide handover operation is executed by the direction configurator when this configurator becomes aware of the OR waveguide fault.

For instance, when the 'Tx' becomes disabled because of the fault of waveguide 1 in Figure 7(b), the packet can be transferred via the 'Tx' (candidate light direction) of waveguide 2, however, if another packet is simultaneously transferred via the 'Rx' (default light direction) of waveguide 2, the communication conflict will arise. We will use the Time Division Multiplexing (TDM) technology to avoid this conflict.

Definition 2. The direction configurator executes the handover process from default to candidate if the number of currently arrived packets exceeds the total amount of ports in the OR.

If no fault occurs, or the number of currently arrived packets does not exceed the total number of ports in the OR, the microscopic path will only traverse along the default light direction, i.e., the handover operation will not be invoked.

4.2 Dynamically reconfigurable bidirectional channel for fault-tolerant schemes

In this section, we propose a dynamically reconfigurable bidirectional channel for fault-tolerant schemes, as described in Figure 8. As shown in Figure 8(a), it includes the control unit of the bidirectional waveg-

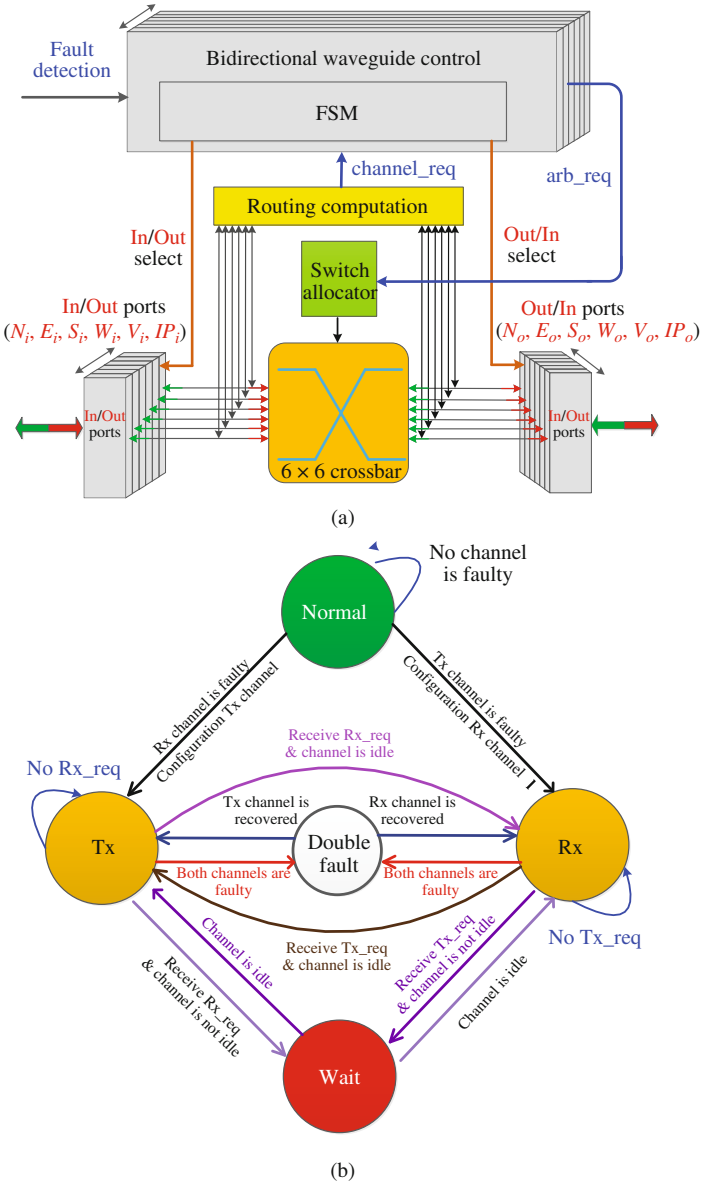

Figure 8 (Color online) (a) Control structure of our extended OR; (b) finite state machine.

uide channel, routing computation unit, switch allocator unit, and 6×6 crossbar unit. The bidirectional channel control module is realized by the Finite State Machine (FSM) shown in Figure 8(b). The detailed operation of the FSM will be discussed later. The 6×6 crossbar unit corresponds to the OR structure in Figure 7(c). As shown in Figure 8(a), each type of port has an input and an output, i.e., N_i, E_i, S_i, W_i, V_i, IP_i and N_o, E_o, S_o, W_o, V_o, IP_o by default, respectively. Each type of port can be either an input port or an output port, which is controlled by In/Out select signals generated from the control unit of the bidirectional channel. For the input optical signal in the OR, the routing path will be computed by the routing computation unit, and if there is no fault detected in the routing path, the default transmission will be in the direction of the red arrow, i.e., the signal comes into the OR from an input port (N_i, E_i, S_i, W_i, V_i, IP_i) to an output(N_o, E_o, S_o, W_o, V_o, IP_o) port through the 6×6 crossbar unit. Once the waveguide fault is detected, the input and output are reconfigured and the transmission will be in the direction of cyan arrow.

The most important part of our fault-tolerant schemes is how to dynamically reconfigure bidirectional waveguides when the fault appears. The reconfigurable mechanism can be described by the FSM in Figure 8(b). In Figure 8(b), there are five states of the OR port: 'Normal' is the default state in which

both the 'Tx' and 'Rx' channels are normal; 'Tx' has the intact channel available for transmitting data; 'Rx' has the intact channel ready for receiving data; 'Wait' is an intermediate state; 'Double fault' is the state in which both the 'Tx' and 'Rx' channels are faulty. The FSM is initially in the normal state, and it will remain in this state if no channel is faulty. Once the fault appears, the relative OR port will be ready to update the 'Tx' or 'Rx' state depending on whether the faulty channel is the 'Rx' or 'Tx' channel.

When the OR port is in the 'Tx' state and receives a reception request (Rx_req), it will transfer into the 'Rx' state if the channel is idle or it will transfer into the 'Wait' state and wait until the end of the current packet transmission before transferring to the 'Rx' state. Moreover, if not receiving the Rx_req until the next clock cycle, it will return back to the 'Tx' state.

When the OR port is in the 'Rx' state, the state transition process is similar to that of the last case. Note that if the 'Rx' and 'Tx' channels are faulty simultaneously, i.e., in the 'Double fault' state, the fault-tolerant mechanism will motivate our routing algorithm to completely abandon this disabled OR during the process of computing the restore path.

4.3 Adaptive reliable routing algorithm

On the basis of the analysis in Subsections 4.1 and 4.2, a novel adaptive reliable routing algorithm named Fault Tolerant Routing Algorithm based on Bidirectional Waveguide Link (FTRA-BL) is proposed in this section. As demonstrated in Algorithm 1, our algorithm, FTRA-BL, has two main parts: macroscopic routing and microcosmic routing. Here, we assume that the coordinates of the source, current, and destination OR nodes are (X_s, Y_s, Z_s), (X_c, Y_c, Z_c), and (X_d, Y_d, Z_d), respectively.

For Part A, the macroscopic routing in our FTRA-BL is achieved by using XYZ dimension order routing. If the current and destination OR nodes have the same coordinate, then the output of the current OR node Pout is 'IP Core' (IP for short); otherwise, we first compare the X coordinate between current and destination OR nodes: if $X_c > X_d$, Pout = 'West' (W for short); if $X_c < X_d$, Pout = 'East' (E for short); if $X_c = X_d$, we continue to compare the Y coordinate between the current and destination OR nodes: if $Y_c > Y_d$, Pout = 'South' (S for short); if $Y_c < Y_d$, Pout = 'North' (N for short); if $Y_c = Y_d$, Pout = 'Vertical' (V for short).

After deciding the macroscopic path, we utilize the fault-tolerant mechanism mentioned in Subsection 4.1 to determine the microscopic path within each OR traversed by this macroscopic path (Part B). For the input port of a certain OR node, we first check whether the default output light direction ('Tx') of the waveguide loses efficiency or not in the OR: if there is no fault, the packet is transferred by the microcosmic path along the default light direction; otherwise, the status of the candidate output light direction ('Rx') is checked: if there is no fault and it is at idle state (no communication conflict), then the direction configurator determines the candidate light direction for the packet transmission along the microcosmic restore path in the OR; if there is no fault but it is not at idle state, we will wait for a clock cycle, and then the direction configurator determines the candidate light direction for the packet transmission along the microcosmic restore path in the OR; and finally, if Rx also has fault, we will utilize the traditional fault-tolerant routing algorithm for the selection of the restore path.

4.4 Simulation results and discussion

In this subsection, we first evaluate the network-level insertion loss of our proposed FTRA-BL and traditional fault-tolerant scheme called FTRA-XYZ. In FTRA-XYZ, if the OR node breaks down, it completely abandons this OR node during the process of computing the restore path. Then, we compare these two fault-tolerant schemes in terms of transmission latency.

4.4.1 *Network-level insertion loss*

We first analyze the insertion loss once faulty ORs exist in a 3D ONoC architecture. Fault-tolerant schemes can be used to provide a certain reliability method to properly maintain network performance.

Algorithm 1 FTRA-BL Algorithm

Part A: Macroscopic routing algorithm.

Require: IP: IP Core, E: East, S: South, N: North, W: West, V: Vertical.

Ensure: **Input**: X_s, Y_s, Z_s, X_c, Y_c, Z_c, X_d, Y_d, Z_d.
Output: P_{out}.

if $X_c = X_d$, $Y_c = Y_d$, $Z_c = Z_d$ **then**
  P_{out} ⇐IP;
else if $X_c > X_d$ **then**
  P_{out} ⇐W;
else if $X_c < X_d$ **then**
  P_{out} ⇐E;
else if $Y_c > Y_d$ **then**
  P_{out} ⇐S;
else if $Y_c < Y_d$ **then**
  P_{out} ⇐N;
else
  P_{out} ⇐ V.
end if

Part B: Microcosmic routing algorithm.

Require: Tx_{normal} and Rx_{normal}: status of Tx and Rx.channels '1': no fault, '0': faulty; $data_{path}$: data transmission path; Rx_{idle}: '1': no communication conflict, '0': communication conflict;

Ensure: **Input**: Tx_{normal}; Rx_{normal}.
Output: $data_{path}$.

if Tx_{normal} = '1' **then**
  $data_{path}$ ⇐ Tx;
else if Rx_{normal} = '1' **then**
  if Rx_{idle} = '0' **then**
    $data_{path}$ ⇐ Rx;
  else
    Wait for a clock cycle;
    $data_{path}$ ⇐ Rx;
  else if Rx_{normal} = '0' **then**
    adopt the traditional fault-tolerant routing algorithm to compute data path;
  end if
end if

In our simulations, we will analyze the ratio of maintaining insertion loss as follows:

$$\text{MaintainRatio} = \left(1 - \frac{\text{IL}_{\text{existfault}} - \text{IL}_{\text{nofault}}}{\text{IL}_{\text{nofault}}}\right) \times 100\%, \tag{27}$$

where $\text{IL}_{\text{existfault}}$ and $\text{IL}_{\text{nofault}}$ are the values of insertion loss when faults exist and when no faults exist in the network, respectively. When the OR has disabled waveguides, FTRA-BL will guarantee that the remaining internal function can still maintain the normal work of the disabled OR; however, FTRA-XYZ completely abandons the disabled OR node during the process of computing the restore path, which increases the transmission distance and insertion loss. The corresponding simulations are executed under four different sizes of 3D torus topology, and the simulation results are shown in Figure 9.

As shown in Figure 9 (a)–(d), when the number of faulty ORs is 0, i.e., the network has no faulty ORs, the insertion loss maintain ratio of two fault-tolerant methods is equal, and their values are both 100%. In other words, both fault-tolerant methods can maintain the best network performance in this case. However, when the number of faulty ORs is greater than 0 as shown in Figure 9 (a)–(d), i.e., there are OR faults in the network, the insertion loss maintain ratio of our FTRA-BL is higher than that of FTRA-XYZ. More specifically, as shown in Figure 9(a), in the $3 \times 3 \times 3$ network, the maintain ratios are 97.3%, 94.6%, and 91.9% for FTRA-BL, while 77.3%, 76.9%, and 73.4% for FTRA-XYZ when the number of disabled ORs is 1, 2, and 3, respectively. The improvement ratios of our FTRA-BL are 25.8% (one fault), 23.1% (two faults), and 25.2% (three faults) over FTRA-XYZ when the topology size is $3 \times 3 \times 3$. Similarly, the improvement ratios are 6.8%, 59.48%, and 96.8% for the $4 \times 4 \times 3$ network (Figure 9(b)); 58.1%, 57.1%, and 87.0% for the $5 \times 5 \times 3$ network (Figure 9(c)); and 24.73%, 42.38%, and 63.49% for the $6 \times 6 \times 3$ network (Figure 9(d)). Thus, simulation results show that the network-level insertion loss for our FTRA-BL performs better than FTRA-XYZ under arbitrary network scale and fault OR numbers.

4.4.2 *Transmission latency*

In this subsection, we analyze transmission latency. According to [23], transmission latency T can be obtained as follows:

$$T = T_p + T_s + T_r, \tag{28}$$

where T_p is the propagation latency, and $T_p = d/ve$. Here, d is the physical distance between source and destination OR nodes, while ve is the light speed. As d is far smaller than ve for on-chip communications,

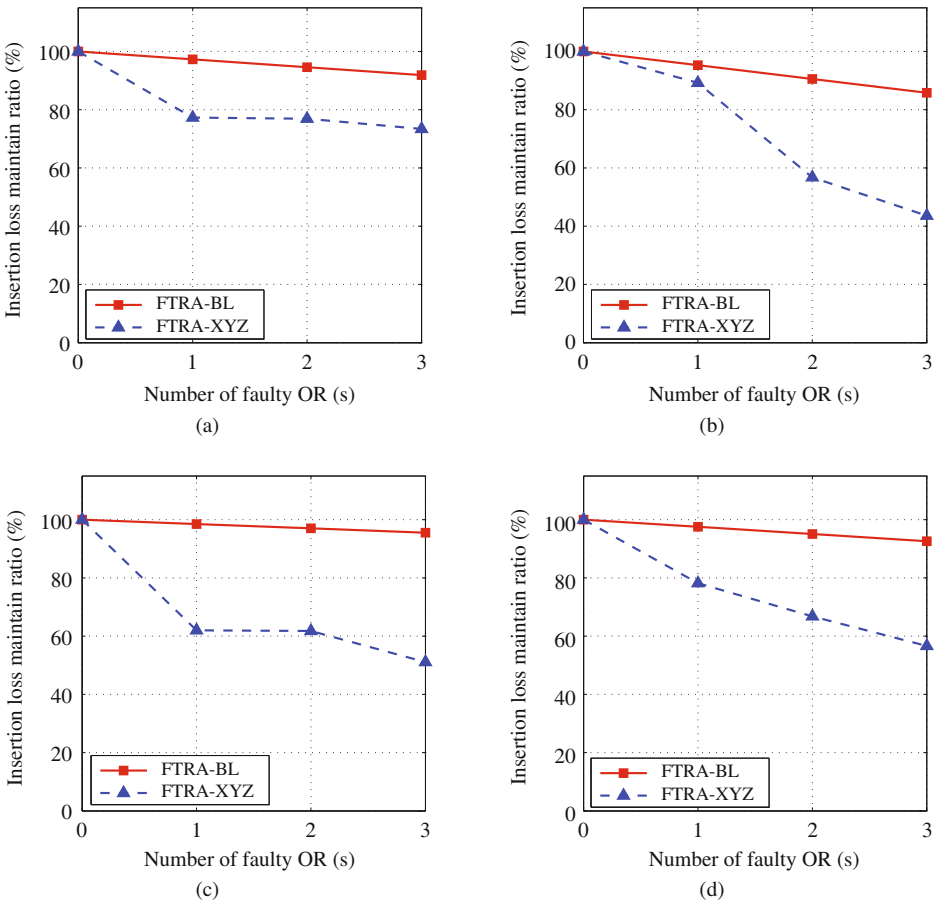

Figure 9 (Color online) The simulation results of the ratio of maintaining insertion loss with different network sizes. (a) Topology size is $3 \times 3 \times 3$; (b) topology size is $4 \times 4 \times 3$; (c) topology size is $5 \times 5 \times 3$; (d) topology size is $6 \times 6 \times 3$.

T_p can be neglected; the packet sending latency T_s is represented as l/B. Here, l is the packet length and B is the channel bandwidth; the routing process latency T_r is obtained as $2 \cdot t \cdot h$. Here, t is the latency produced through an OR and h is the total number of ORs along the path. Considering the routing process latency in path setup of the request and the acknowledgement, the $t \cdot h$ term is double in (28).

According to [24], the average number of routing hops h for the $m \times n \times k$ ONoC is

$$\text{hop} = \frac{mnk(m+n+k) - k(m+n) - mn}{3(m \times n \times k - 1)}. \tag{29}$$

Next, if the current ONoC has no fault, the total number of ORs along the path $h = \text{hop}$. If there exist disabled OR nodes in the current ONoC (given the number j of concurrently invalid ORs in the current ONoC), we have $h = \text{hop}$ for FTRA-BL, because the path will occupy the same number of ORs with fault-free, i.e., in Figure 7(c), for the packet transmission from the 'East' port to 'North' port, whether fault-free or an existing fault, it only occupies one OR. For the original OR structure, the restore path will detour around disabled ORs, i.e., the disabled OR node will be discarded and replaced by another backup one, which will consume two OR nodes. Thus, if there are j disabled ORs, we have $h = (\text{hop} + 2 \cdot j)$.

According to [23], we assume $t = 0.01$ s, $l = 8$ GHz, $B = 12.5$ GHz. The simulation results of the transmission latency discussed above are shown in Figure 10. Figure 10 (a)–(d) demonstrate the transmission latency in the cases of one OR fault, two OR faults, three OR faults, and four OR faults, respectively. The number in the horizontal axis denotes the topology size. In our simulations, we assume $m = n$ (where n varies from 3 to 10), and $k = 3$. From the simulation results, we can see that the transmission latency of our FTRA-BL is lower than that of FTRA-XYZ. With an increasing number of disabled ORs, this advantage becomes more obvious.

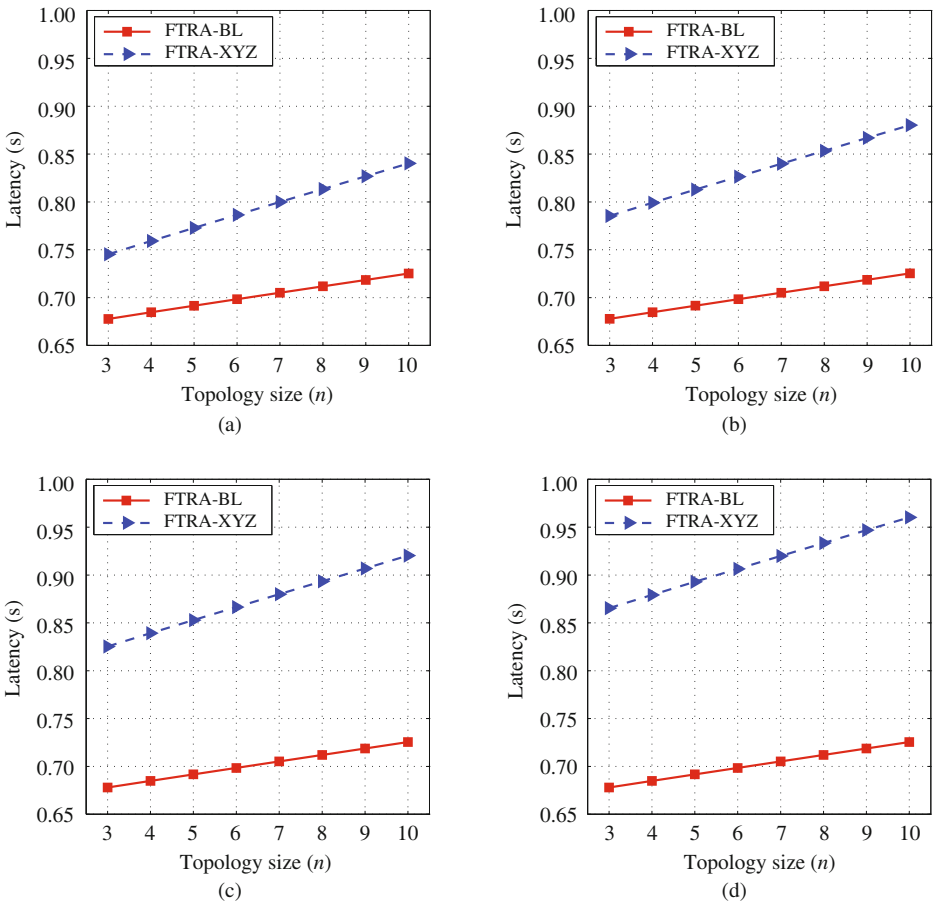

Figure 10 (Color online) The simulation results of transmission latency with different fault OR numbers. (a) One fault OR; (b) two fault ORs; (c) three fault ORs; (d) four fault ORs.

5 Conclusion

In this study, we first designed the low insertion loss and high scalable OR structure. Next, we designed a novel fault-tolerant OR structure for 3D torus ONoCs that utilizes bidirectional waveguides, in order to guarantee that the remaining internal functions can still maintain the normal work of the disabled OR. Based on new OR structures, our adaptive reliable routing algorithm improves the transmission latency and reliability more efficiently than benchmarks.

Acknowledgements This work was supported in part by Fundamental Research Funds for the Central Universities (Grant Nos. N130817002, N140405005, N150401002), Foundation of the Education Department of Liaoning Province (Grant No. L2014089), and National Natural Science Foundation of China (Grant Nos. 61302070, 61401082, 61471109, 61502075).

Conflict of interest The authors declare that they have no conflict of interest.

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