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A yield-enhanced global optimization methodology for analog circuit based on extreme value theory

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Abstract The challenge in variation-aware circuit optimization with consideration of yield is the trade-off between optimized performance, yield and optimization runtime. This paper presents a practical variation-aware circuit global optimization framework named GOYE, which shows the advantages on performance, yield and runtime. It uses an approach called constraint violation elimination (CVE) in global search phase to prune initial starting points and uses the gradient-based method in local search to locate optimum. The worst-case analysis (WCA), which is necessary for variation-aware circuit optimization, is nested in the local optimization process. The efficiency is significantly improved by a novel method based on extreme value theory (EVT). Our EVT-based method is also the first one that allows users to control the target yield such that under-design or over-design can be avoided. A design example in TSMC 65 nm technology is illustrated in the paper where all performance achieves three-sigma yield with consideration of environmental and inter-die/intra-die process variations.

Keywords global optimization, yield enhancement, analog design automation, extreme value analysis (EVA), sequential quadratic programming (SQP), worst-case analysis

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1 Introduction

As the consumer-driven, high-volume IC market continues to grow, the pressure on design teams to deliver new and improved products is greater than ever. The competitive edge is usually derived from time-to-market. To maximize the profit, it is desirable to minimize the design cycle. For system-on-chip (SoC), the portions of analog and mixed-signal circuitry increase significantly compared with the past that SoC contains mostly digital circuitry [1], which indicates more design time and effort is devoted to analog and mixed-signal design than ever. Aside from design time, designers are also seeking potential performance gains, power savings, and area reductions. On the other hand, as geometries shrink, variations challenge designers more than ever. To reduce the risk of re-spins, designers are more willing to

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trade some performance and area used, leaving more design margin to keep circuit performance stand against variations.

Designers are spending more time on simulating and verifying the circuits due to the variations. Therefore, the challenge for designers is how to deliver high-performance design considering variations before deadlines to keep the competitive advantage for their products.

Analog design optimization provides efficient solutions for the challenge mentioned above. It is able to accelerate time-to-market by reducing design time significantly while delivering higher performance gain, lower power consumption, and less overall area without compromising design margins or decreasing reliability. Analog design optimization tools take topology-fixed un-sized analog circuits, translate them into optimization problems, and solve them with efficient optimization algorithms. Research works of analog design optimization at earlier years are focused on performance optimization without considering variations. Many of these works chose algorithms that are belonging to the class of evolutionary algorithms (EA). EA includes: genetic algorithm (GA) [2], the most popular type of EA that mimics the process of natural selection; differential evolution (DE) [3], which optimizes a problem by iteratively improving a candidate solution based on vector differences; and imperialist competitive algorithm (ICA) [4], which simulates human social evolution and can be thought of as the social counterpart of GA. Another widely studied class of algorithm is swarm intelligence (SI). Ref. [5] presents the SI-based algorithms particle swarm optimization (PSO) and ant colony optimization (ACO) on optimizing analog circuits. These kind of algorithms mimic the intelligent behavior of decentralized, self-organized systems. Simulated annealing (SA) is used in [6]. The disadvantage of SA is that it is computation-intensive [7]. Analog circuitry is getting more and more complex in order to implement more functionalities. As such, from numerical optimization perspective, the objective function is becoming more complicated, which introduce more local optima. Due to the increasing complexity of the circuitry, transistor sizes are increased as well, which creates a higher dimensional problem for circuit performance optimization. Therefore, the first challenge is how to find an efficient global optimization method to overcome the increasing complexity of circuitry while still able to deliver high optimized performance.

As geometries shrinking, the negative impacts on the circuit performance from variations are not negligible. Therefore, some latest methods aim at yield-aware optimization, which is able to deliver optimized performance while keeping high yield. Such methods require yield estimation or to find performance worst-case during the optimization process. Ref. [8] obtained performance worst-case from the traditional three-corner analysis. However, it is no longer sufficient at advanced technology nodes. More corners are required to find out the worse-case scenario of the design. Refs. [9–12] present methods for yield estimation by linearizing the performance in worst-case scenarios, which could introduce errors. Refs. [13–15] use improved sampling-based methods (LHS, QMC) for yield estimation. The overall simulation counts are high, preventing them from being used in practice. Refs. [16,17] developed the analytical yield model to improve the efficiency of optimization. For advanced technology process, the more detailed model is required to maintain the accuracy. The response surface modeling technique is used to determine the worst-case parameter in [18, 19], and the boundary integral method that formulates yield itself as a surface integral on the boundary of acceptability region is given in [20]. The computational cost of these methods is increased by the increase of dimensionality, which is not suitable for modern complex circuit design. Ref. [21] applies the worst-case distance to estimate the boundary of the acceptable region which could be too conservative, and could bring inaccurate estimation for the non-convex scenario. Ref. [21] defines an ellipsoid-shaped region for process variation, and make an assumption that within the region is Gaussian distributed. Literature that study efficient worst-case analysis (WCA) are presented in [22–25]. Refs. [22, 23, 25] linearize circuits in the frequency domain and apply Kharitonov's function to obtain the performance bounds under variations. Ref. [24] applies optimization algorithm on the transfer function of the circuit to find the maximum or minimum of the transfer function value, and obtain the performance worst-case thereby. These methods are heavily relying on the accuracy of the small signal model, which requiring extra effort to derive such model. It is applicable in the frequency domain, but hard to extend to the time domain. In summary, the second challenge is how to obtain the performance worst-case value accurately and efficiently. The performance with respect to variations is not single minima region. It

cannot be simplified considered as an ellipsoid-shaped region. The increasing number of transistors consequently increases the number of process parameters. The dimensional increment makes the modeling method, such as Kriging, ineffective and loss of accuracy. From the distribution perspective to perform WCA, one cannot be over-simplified consider process variation with respect to nominal design is Gaussian distributed.

Therefore, we propose a very efficient and practical circuit performance Global Optimization with Yield Enhancement framework named GOYE as a solution for above-mentioned challenges. The features and innovations of this work are including as follows.

(1) This work proposes a hybrid global optimization framework for analog circuits. At global search phase, it utilizes the multi-start (MS) strategy and combine with a method named constraint violation elimination (CVE) to prune the starting points. The probability of finding global optimum is improved by such strategy. As local search phase, WCA is nested at each iterate of the gradient-based algorithm, to ensure the worst-case performances are within specifications.

(2) The most significant contribution of this work is to propose an efficient yet very accurate worst-case estimation method based on extreme value theory (EVT). It does not require of knowing or making the assumption of the probability density function of performance parameter with respect to process variations. Our approach is a statistical-based method, which can make success predictions when parameter space is not a single optimum region. Our work is first one, to our best knowledge, that provides the controllability of the yield value for performance parameters. It can optimize the circuit with performance parameters to meet any user-defined yield value. Even in one circuit optimization, different parameters can have different yield values. This is an important improvement, which will benefit different applications. For performance parameters that do not require a high-yield value (i.e., 3σ), users can set the target yield as a lower yield value (i.e., 2σ) in the exchange of better performance. And for performances that require high-yield (i.e., $\geqslant 4\sigma$), such as data retention voltage in SRAM [26], our approach is still able to accurately estimate the value of performance high-sigma point. Another feature of this EVT-based method is the nearly dimensional independence, which has the advantage of scalability. Our experimental results in the following section will show good estimation accuracy on a circuit with over 100 statistical parameters.

(3) The framework of GOYE is hierarchical and each phase can be fully run in parallel, which makes it more efficient and attractive in the multi-core or multi-node platform.

The rest of the paper is organized as follows: Section 2 introduces the fundamentals of yield optimization. Section 3 describes the framework of GOYE with algorithms/approaches used in GOYE. Section 4 illustrates worst-case analysis by EVA based method. Section 5 shows an example of yield-aware circuit optimization by GOYE and Section 6 concludes the paper.

2 Yield optimization

2.1 Yield optimization formulation

Circuit design automation and optimization (circuit optimization in short) are the process of finding the design parameters d that optimized the performances. When this process is taken place at nominal PVT condition, we denote it as the performance optimization. However, when environmental variation (temperature t and supply voltage v) e and process variation p are taken into account, we denote such optimization process as yield optimization or performance optimization with yield enhancement. The optimization problem is normally constrained problem, where performance specifications, specs for short, are the constraints c of the optimization. The target yield γ is the percentage of manufactured circuits that meet the specifications. For circuit optimization, since it is at pre-silicon phase, we redefine γ as the probability of performance parameter, at a given set of design parameters, that within the specification due to the variations. The relationship of γ and specs is illustrated in Figure 1. High yield circuit optimization is normally more challenging because it requires adequate margin between the centering of

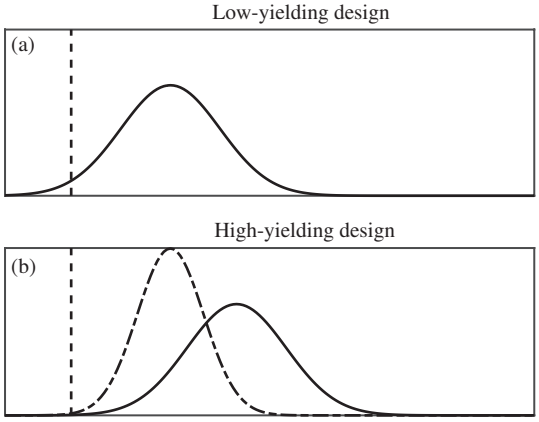

Figure 1 The low-yield design could have a large portion of its PDF out of spec (a). A robust design with high-yield could keep nominal value move away from spec to leave more design margin for variation (solid curve, (b)) or have narrow PDF such that little portion is out of spec. The shifting of nominal value and performance sensitivity could happen at the same time.

the design and the spec, or finds d such that the design is less sensitive to variations. Together, the yield optimization problem is formulated as

$$\min \quad f(d,t,v,p,\gamma) \qquad \text{s.t.} \quad \begin{cases} c_{\text{ieq},i}(d,t,v,p,\gamma) \leqslant 0, & i=1,\ldots,n_{\text{ieq}}, \\ c_{\text{eq},i}(d,t,v,p,\gamma) = 0, & i=1,\ldots,n_{\text{eq}}, \end{cases} \tag{1}$$

where $f(d,t,v,s,\gamma)$ is the circuit performance parameter (power, delay, etc.) that should be minimized, and $c_{\text{ieq},i}(d,t,v,s,\gamma) \leqslant 0$ and $c_{\text{eq},i}(d,t,v,s,\gamma) = 0$ are inequality and equality constraints respectively. Conventionally, this standard form is defined as a minimization problem. Due to the complexity of circuit, the cost function that combines objective function with constraints contains multiple local minima. Hence, yield optimization problems are known as global optimization problems.

2.2 Global and local optimization with consideration of variations

An analog circuit usually has tens or hundreds of transistors; despite the fact that some transistor sizes are matched, there are still many transistors to be sized. In the optimization, these transistor sizes are treated as variables, and form multidimensional space on each performance parameter. It is not difficult to understand that within such variable spaces, the performance parameters will have multiple local optima (maxima or minima), which leads to the existence of multiple qualified designs with different sizing. In order to show this, we run a set of local optimizations from different starting points on a single-stage folded-cascode circuit. The specifications that used as constraints of the optimization problem are given in Table 1. Five feasible solutions after local optimizations are selected, and all of them satisfy specifications strictly. In Table 2, three out of six performance parameters as well as 3 out of 13 variables are shown. The last column is the normalized distances (ND) towards the first set of parameters,

$$\text{ND}_i = \sqrt{\frac{\Sigma(x_i - x_1)^2}{n}}, \tag{2}$$

where x_i is normalized variable value. The greater the ND is, the more distance there is between these two local optima. If ND=1, it means two optima are located at opposite corners. As we can see from the table, the normalized distances are not small enough, which suggests all sets of variables could have located in different local regions. Note that, we only show 10 set of optima in the table, and more local optima exist for this circuit. Hence, we show that the circuit optimization problem belongs to global optimization, and global optimization algorithms should be implemented to improve the efficiency of finding the global optimum. There are generally two types of methods for solving global optimization algorithm. One is to use pure global optimization methods such as genetic algorithms (GAs), simulated

Table 1 The specification of test bench circuit

	Gain	GBW	PM	$\mathrm{SR}_{\mathrm{avg}}$	$1\%Ts_{\mathrm{avg}}$	I_Q
Spec.	$>$ 50 dB	$>$ 70 MHz	$>80^\circ$	$>$ 40 V/μs	$<$ 10 ns	$<$ 800 μA

Table 2 The optimized performance from 10 different starting points with the normalized distances

No.	Performance			Variables (3/13)			ND
	I_Q	Gain	Ts	W_1(μm)	$W_{3,4}$(μm)	$W_{11,12}$(μm)	
1	0.68	62.50	6.90	171.12	198.90	40.20	0
2	0.59	53.72	9.50	191.68	120.04	20.04	0.23
3	0.61	60.15	8.34	193.70	108.24	22.54	0.18
4	0.67	62.21	6.98	186.78	172.42	20.07	0.12
5	0.60	61.89	8.16	183.47	191.96	36.03	0.33

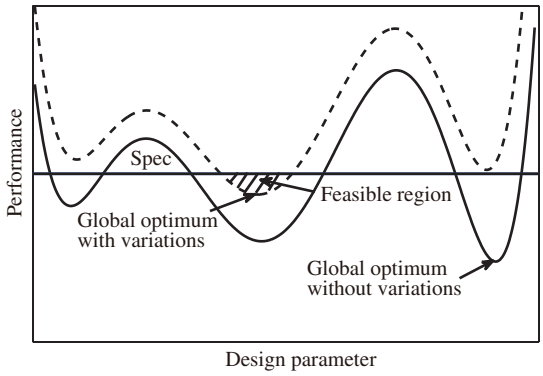

Figure 2 An illustration of performance global optimum with and without consider of variations. The solid line is the performance from nominal condition while the dashed line represents the worst-case scenario once variations are considered. The horizontal line represents the spec.

annealing (SA), and direct search (DA). These methods are normally derivative-free. They have the advantages of searching the global optimum but have the efficiency disadvantages on their convergence, which means a large amount of cost function evaluations are required to reach the optimum. Another type of method is called hybrid optimization. These kinds of methods perform a global search at the beginning to provide good candidate starting points and then use derivative-based optimization methods to find local optima. If the choice of starting points is good enough, one of the local optima may end up as a global or near global optimum. Due to the fast convergence, the hybrid optimization methods have the advantages of simulation cost over pure global optimization methods.

Variations, including environmental and process variations, bring about performance degradation that complicates the optimization problem. As illustrated in Figure 2, a global optimal design under nominal condition does not necessarily be the global optimal design once PVT variations are considered. The true yield-aware global optimum could shift to other local optimal where such optimum is less sensitive to variations. Sometimes, when design specs are tight, "global optimum" from nominal condition could have a large portion out of spec. Therefore, the robust design should have all performances worst-cases within specs, and this is the objective of our GOYE.

3 GOYE methodology

In this section, we introduce the framework and optimization flow of GOYE, and present detailed algorithms and techniques used in GOYE. Numerical experiments are conducted to verify the efficiency and accuracy of approaches and techniques.

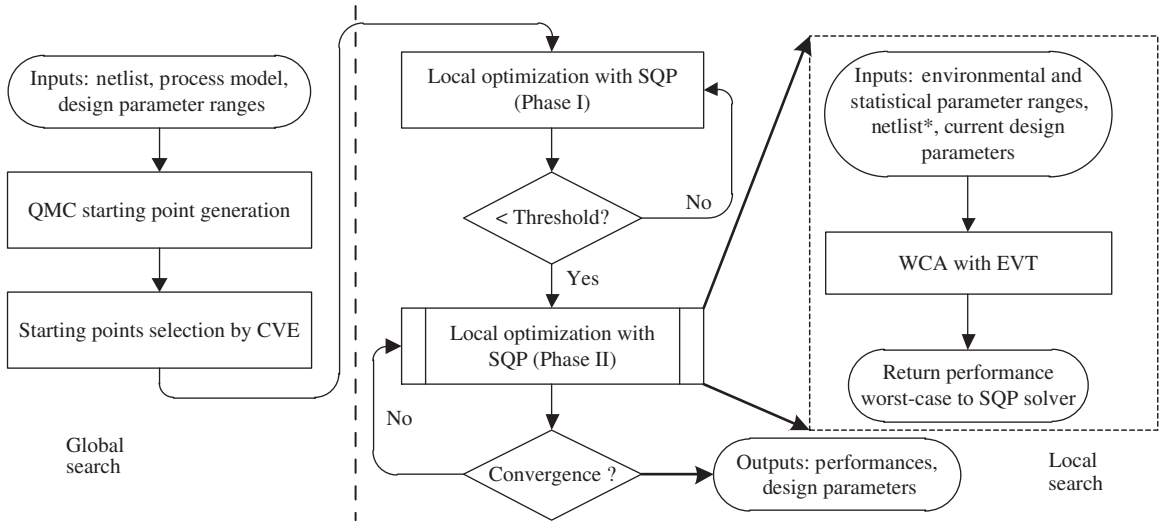

Figure 3 GOYE framework.

3.1 GOYE framework

GOYE uses the hybrid optimization strategy multi-start (MS) as the circuit performance global optimization algorithm. The basic MS method generates uniformly distributed starting points in design parameter space, and starts local optimizations from each of these. The attractive feature of MS is that it applies a "region hit" strategy compared with "point hit" strategy, where population-based evolutionary algorithms are belonging to the latter. With limited starting points, there is no guarantee MS is able to converge to the global optimum, but a significant efficiency improvement of finding the good solutions can be expected via MS method. The reason behind this is the probability of hitting the good region is much larger than that of hitting a point. As long as we choose a handful of starting points that are located in the good region (the region contains feasible solutions), by applying gradient-based local optimizations, we can effectively find one or more feasible solutions. Therefore, this MS hybrid optimization framework is chosen as our optimization flow.

GOYE starts with global search phase to select promising starting points for local search phase, the efficiency of global search is improved by an approach named constraint violation elimination (CVE). The local search applies gradient-based optimization algorithm. To enhance the yield of optimized design, the worst-case analysis (WCA) is nested at major iterate of local optimization to ensure the worst performances can still be optimized within specs. We use a metric, called the weighted constraint violation sum, to monitor the degree of convergence, and once it is less than a threshold, WCA is enabled. This could reduce the simulation cost brought about by WCA in the local optimization phase, and the efficiency of WCA is improved by the proposed approach based on the extreme value theory (EVT), which will be introduced in Section 4. Figure 3 gives an overview of GOYE framework. Details of the framework are described below.

3.2 Global search

The objective of the global search phase is to prune the starting points, which are used as initial points for the subsequent local optimizations. In the first step of global search phase, a set of random design parameters is generated in the design parameter space by using quasi-Monte Carlo (QMC) method. QMC uses low-discrepancy sequence, which is able to generate highly uniformed samples in variable space over the pure Monte Carlo (MC) method. This could avoid the scenario that two starting points are adjacent and optimizations from them will end up to the same local optima. Considering a local circuit optimization is time-consuming, eliminating such scenario via QMC could significantly improve the efficiency. Latin hypercube sampling (LHS) is also widely used for generating low-discrepancy sequence [13, 27]. However, the efficiency of QMC over LHS is shown in [28]. Hence, we apply QMC method in this paper.

Table 3 Numbers of optimized results on each performance level

	Lv.1	Lv.2	Lv.3	Lv.4
With CVE	5	5	10	30
Without CVE	0	10	5	35

Among the design parameter spaces, designs in many regions cannot make circuits operate correctly. These regions are referred as infeasible regions. For instance, considering a two-stage Miller Op-Amp design, the common practice of the second stage transistor sizes should be much larger compared with that of first stage transistors, in order to keep a good phase margin. As such, the design parameter space, where the values of first stage transistor sizes are greater than the values of the second stage should be considered as infeasible regions. Local optimizations from starting points located in the infeasible regions have little probability of finding the feasible solution. Therefore, it is necessary to eliminate these starting points. CVE method evaluates each starting point generated by QMC and calculates the weighted constraint violation sum (WVS) of each starting point:

$$\mathrm{WVS} = \sum_{i1=1}^{n1} \cdot w_{i1} \cdot \max\left(\frac{(P_{i1} - p_{i1})}{P_{i1}}, 0\right) + \sum_{i2=1}^{n2} \cdot w_{i2} \cdot \max\left(\frac{(P_{i2} - p_{i2})}{P_{i2}}, 0\right), \tag{3}$$

where n_1 is the number of performances that should be optimized greater than the specs, and n_2 is the number of performance that should be optimized less than the specs; p_{i1} or p_{i2} denotes the performance that is obtained from QMC sampling, and p_{i1} or p_{i2} denotes the target performances which are specifications. w_{i1} and w_{i2} are weights of different specifications. WVS is a non-negative number, if WVS=0, then there is no constraint violation, where all performances are in specs. By calculating the WVS of each starting point, CVE eliminates starting points that have high WVS to provide an intelligent selection of initial points for local search. Table 3 compares the success rate of finding the feasible solution from using and not using CVE on the optimizations of a single-stage folded-cascode Op-Amp. We select 50 out of 500 starting points using the CVE approach and then execute local optimization. The results are compared with local optimization results from 50 random starting points. Level one results indicate all performances meet the specs. Level two and level three results indicate all performances meet the 95% and 90% of specs respectively. And level four results are scenarios that local optimizations failed to find feasible solutions, which implies these starting points are more likely located in bad regions. We can see from the table that local optimizations that use CVE method, have the higher possibility of finding the good regions among design parameter spaces than that from the starting points without using CVE.

3.3 Local optimization

In the local optimization phase, a derivative-based local optimization algorithm is chosen. Newton's method (also known as the Newton-Raphson method), is one of the most popular derivative-based algorithms for local optimization. It approximates the problem as a quadratic function and finds the minimum in a few iterations. The proof of its convergence is given in [29]. Sequential quadratic programming (SQP), a derivative-based local optimization algorithm that is a natural extension of Newton's method, is applied in GOYE. The SQP algorithm is considered one of the most powerful nonlinear programming algorithms we know today for solving differentiable nonlinear programming problems [30]. It is an iterative procedure, which models non-linear problems at each iterate, as quadratic programming (QP) sub-problems. It solves current QP problem and takes the solution to constructing the sub-problem of the next iteration. The theory of the SQP algorithm is well discussed in [31, 32].

The starting points for local SQP optimization are chosen from global search phase. To improve the yield of the circuit optimization, WCA is nested in the iteration of local optimization to find out the worst performance values with respect to a target yield at current design parameters of the iteration. This iterative worst-case optimization method has the advantages of finding the local optimum as compared with the two-step method, such as [33], where the latter finds the local optimum vector at the nominal

condition and then maximize the yield by minimizing tolerance region around the vector. As such, the worst-case should be checked every iterate to ensure the optimization process can converge to d_{WC}.

However, considering the extra simulation cost brought about by WCA, it is not practical to perform WCA at each iterate of optimization. Hence, we set a threshold for WVS; if WVS is above the threshold, referred as local optimization phase I in Figure 3, which generally indicates the local optimization is not near to its convergence. We only perform optimization with respect to the nominal corner. Once the WVS is below a threshold, referred as phase II, the worst-case performances are checked at each iterate of the rest of optimization process, and the worst-case values are returned to the SQP solver. This idea is similar as presented in [34, 35]. Note that WVS is only an indicator; its value has no interference to the local optimization process.

4 Worst-case estimation with extreme value analysis

Circuit performance is inevitably influenced by variations. Variations due to manufacturing processes (P), and variations due to the environment such as voltage (V) and temperature (T). Process variations can be further classified as intra- and inter-die variations. Intra-die or die-level variations are comprised of systematic variations, which are strongly layout dependent; and random variations, which reflect random fluctuations of process parameters. Inter-die or wafer-level variations occur from one die to another, which means the chip performs differently from other chips of the same wafer. Foundries provide statistical variables to model process variations. In this paper, we denote statistical variables and environmental variables together as PVT variables.

The worst-case analysis (WCA) is to find out the worst-case performance value with respect to variations. Designers usually use Monte Carlo (MC) sampling to find worst-case performances by evaluating on randomly selected statistical parameter values. The worst-case of circuit performance in MC sampling is found on the tail of the performance distribution. When performance parameters are not Gaussian distributed or symmetrical distributed, which is not rare, MC method then requires thousands or more samples, making it computational inefficient and expensive, especially been used in the yield-aware circuit optimization. Literature that provides alternative WCA methods are introduced in Section 1. We briefly summarize the shortcomings from these previous works.

(1) Given a set of design parameters, the space of performance with respect to PVT variables contains multiple local minima. As such, local optimization on the variable space is not sufficient to guarantee that the worst-case can be found.

(2) Due to the multiple local minima property, the modeling of such space will show inaccuracy. As the circuit scales up, the number of statistical parameters increases as well. Modeling-based methods then suffer from the curse of dimensionality, made them computational inefficient.

(3) The distribution of performance parameter with respect to PVT variables is non-parametric. Therefore, any assumption of its type, such as Gaussian distribution, will eventually lead to huge estimation error.

In this section, we introduce a very efficient sampling-based worst-case analysis approach based on extreme value theory (EVT). EVT or extreme value analysis (EVA) [36] is used to model and estimate the behavior of rare events with extreme probability. Our application is aim to obtain the worst-case performance value, which is on the tail of the performance distribution. As such, EVT provides a natural advantage of exploiting the statistical extreme value, in this case, the worst-case value. The proposed method is able to estimate performance worst-case in handful circuit simulations while keeping high accuracy of the estimation, and the cost is able to remain almost the same as the circuit scales up (contains more statistical parameters). The proposed approach can be used either in yield-aware circuit optimization or as a standalone worst-case analysis tool.

4.1 WCA formulation

The semiconductor foundry defines process statistical parameters and their distributions for both intra-

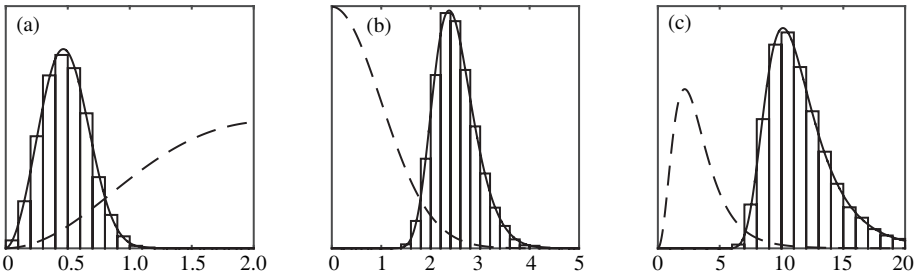

Figure 4 GEV distributions of different types of statistics. (a) Short-tailed; (b) medium-tailed; (c) long-tailed.

and inter-die variations in the process library. However, environmental variables have no available distributions. Therefore, in this section, we consider two cases for environmental variables. In each case, the environmental variables are combined with all available statistical parameters to construct performance parameter space under variations.

Case 1. Evaluating on two deterministic extreme environmental conditions: fast condition ($1.1V_{DD}$ and -40°C) and slow condition ($0.9V_{DD}$ and 125°C) while keeping process statistical parameters as random variables. The worst-case of performances can then be found on the worse one of these two conditions. This method avoids to under-weight failures at extreme environmental variations with the cost of doubling the circuit simulation count.

Case 2. Modeling both voltage and temperature variations as uniform distributions, where the range of voltage is $[0.9V_{DD}, 1.1V_{DD}]$ and the range of temperature is [-40°C, 125°C]. These two environmental variations are mixed together with statistical parameters to form PVT variables.

The purpose of Case 1 is to investigate performance distribution at extreme temperature and voltage conditions to avoid underestimate the influence brought about by temperature and voltage (VT). However, theoretically speaking, the worst-case performance may not exactly happen at the two extremes the environmental conditions. Therefore, we model VT as uniform distributions in Case 2, to further ensure that worst-case performances will not be omitted by Case 1. We will show the efficiency and accuracy of our WC estimation approach on both cases this section.

4.2 Extreme value theory

One of the approaches for EVA relies on block maxima series, which is described as follows: Let $X_1, X_2, \ldots, X_n$ be a sequence of independent and identically-distributed (i.i.d.) random variables, and $M_n = \max\{X_1, X_2, \ldots, X_n\}$, M_n then follows a generalized extreme value (GEV) distribution as $n \to \infty$ [36]. The probability density function (PDF) for the GEV distribution is,

$$f(x|k,\mu,\sigma) = \left(\frac{1}{\sigma}\right)\exp\left(-\left(1+k\frac{(x-\mu)}{\sigma}\right)^{\frac{1}{k}}\right)\left(1+k\frac{(x-\mu)}{\sigma}\right)^{-1-\frac{1}{k}}, \quad \text{for} \quad 1+k\frac{(x-\mu)}{\sigma} > 0, \tag{4}$$

where k is the shape parameter, μ is the location parameter, and σ is the scale parameter. Note that μ and σ are not the mean and standard deviation of GEV distribution. For $k > 0$, it is referred to as a Type II case, and for $k < 0$, it is referred to as a Type III case. The Type I case is when $k = 0$ and the corresponding density is

$$f(x|k,\mu,\sigma) = \frac{1}{\sigma}\exp\left(-\exp\left(-\frac{(x-\mu)}{\sigma}\right) - \frac{(x-\mu)}{\sigma}\right). \tag{5}$$

Distributions, whose tail decreases exponentially, such as normal distribution, lead to Type I [37].

Figure 4 illustrates GEV distributions of three-type of parent distributions. It is shown that regardless the type of the parent distribution, its GEV distribution can be accurately fitted with parameterized distribution. Hence, given a performance distribution that is hard to fit any known distribution, it is therefore hard to obtain worst-case value accurately on such distribution. The concept of our proposed method is to fit GEV distribution of original performance distribution firstly, and then find a value on GEV distribution that could map to the worst-case value of the original distribution.

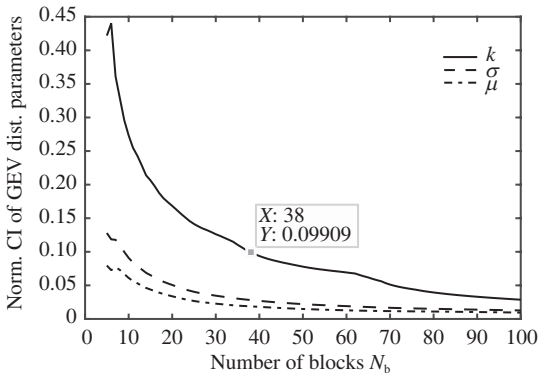

Figure 5 The normalized CI of the GEV distribution parameters k, μ, σ are improved by increasing the number of blocks. In this experiment, when N_b=38, all norm. CIs are below the threshold, T=0.1.

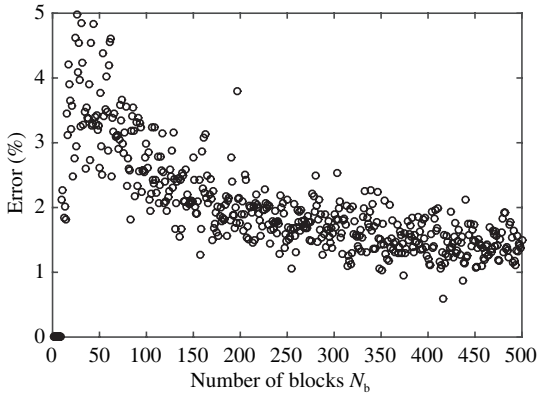

Figure 6 Prediction accuracy is improved as the number of blocks increases.

4.3 Worst-case estimation with EVA

Circuit performance $P = f(x)$ under variations, at a set of fixed design parameters, is a function of PVT parameters x. The cumulative distribution function (CDF) of P is denoted as F. Given a percentage point, $\gamma \to 1$, $F^{-1}(\gamma)$ represents the worst-case PWC when P is the less the better, and for P is the greater the better, negating the sign of P, this still applies. The percentage point can be 2-sigma, 3-sigma, or any user-defined percentage. The original distribution of circuit performance F is not known to us. However, as stated in the previous section, the GEV distribution is parametric and can be fitted through sampling. The CDF of GEV distribution is denoted as F_{GEV}.

The worst-case estimation starts with N_b times of independent generation of random samples of design parameters, with equal sample sizes N_s. $N = N_b \cdot N_s$ random sets of design parameters are generated at this point. Each set of design parameter is treated as the input of the circuit netlist, and evaluated by SPICE simulator. N_s is also referred as the blocksize, while N_b is called the number of blocks. The target circuit performances are calculated after circuit simulations. The maxima from sample blocks, denoted as the block maxima, are used to form block maxima series (BMS). BMS is used as the dataset to perform maximum likelihood estimation (MLE) on three parametric variables of the GEV distribution, F_{GEV}. The accuracy of the GEV distribution fitting is impacted by N_b. The larger N_b, the more accurate the GEV distribution is. We iteratively perform such sampling and fitting until the normalized 95% confidence interval (CI) of parameters of GEV distribution are below a threshold T, or N_b reaches a pre-defined maximum number $N_{b,\max}$. The normalized CI is defined as

$$\mathrm{CI}_{\mathrm{norm}} = \frac{\mathrm{CB}_{\mathrm{U}} - \mathrm{CB}_{\mathrm{L}}}{|\overline{\mu}| + 1}, \tag{6}$$

where CB_{U} and CB_{L} are upper and lower confidence bounds, and $|\overline{\mu}|$ is the mean of fitted parameter values. The reason CI is normalized by $|\overline{\mu}| + 1$ instead of $|\overline{\mu}|$ is to prevent $|\overline{\mu}| \to 0$ scenario. In practice, only a handful of N_b is required to achieve this. Figure 5 demonstrates a GEV distribution fitting accuracy is improved by increasing N_b. The parent distribution of this GEV distribution is a normal distribution with $\mu = 0$ and $\sigma = 1$. The accuracy improved GEV distribution will eventually help to enhance the worst-case estimation accuracy. Figure 6 shows the worst-case ($\gamma = 3\sigma$) prediction error with respect to N_b (N_b=[10, 500]), the fluctuation of the prediction error is caused by the natural of statistics but overall trade shows that the increase of N_b improves the estimation accuracy.

If $N_s \to \infty$, the location parameter $\hat{\mu}$ of GEV distribution is a good estimate of P_{WC} [38]. However, a large N_s makes such method computational inefficient, which is contrary to our initial intention. In this paper, we show our improvement by using a small deterministic N_s while still keep high accuracy of estimation. The mean of GEV distribution is pushed towards the tail of parent distribution as N_s

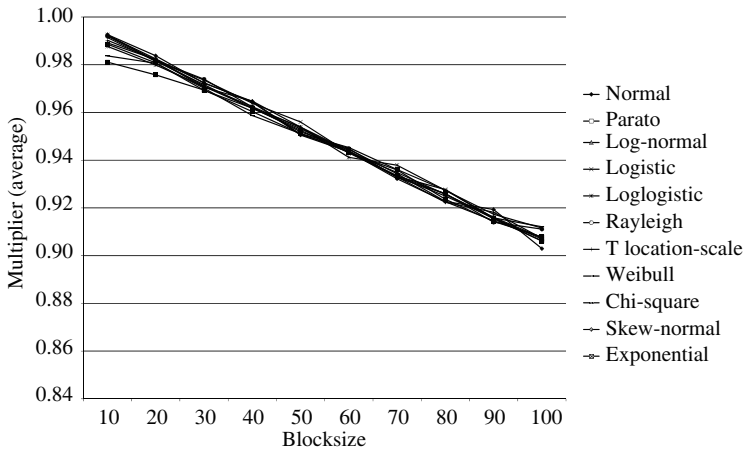

Figure 7 The mean of the multiplier with respect to blocksize $N_{\rm s}$ and percentile γ.

increases, and the variance of GEV distribution decreases. With small $N_{\rm s}$, the location parameter $\hat{\mu}$ is no longer valid for estimating $P_{\rm WC}$. Our method, instead, seeks a percentage point β of GEV distribution with respect to $N_{\rm s}$ that could accurately estimate $P_{\rm WC}$,

$$P_{\rm WC} = F^{-1}_{\rm GEV}(\beta). \tag{7}$$

The percentage point β should be a function of γ. Since they are both percentage, intuitively, a multiplier α is applied to link between them,

$$\beta = \alpha\gamma. \tag{8}$$

Therefore, $P_{\rm WC}$ can be obtained by

$$P_{\rm WC} = F^{-1}_{\rm GEV}(\alpha\gamma). \tag{9}$$

To investigate the property of this multiplier α, we design a set of experiments. We pick several well-known parametric distributions: Normal, Parato, Log-normal, Logistic, Loglogistic, Rayleigh, T location-scale, Weibull, Chi-square, Skew-normal and Exponential. For each distribution, we assign reasonable ranges for its parameters, and randomly generate 100 sets on each distribution type. Since the CDF of original distribution is known at this time, we are able to calculate the corresponding α. Figure 7 shows the mean of α from 100 sets for each type of distributions with respect to different $N_{\rm s}$ at (γ=99.9). From this figure, we can see that α is monotonically decreasing with respect to $N_{\rm s}$. The amazing phenomenon is that α is not a function of distribution type neither their parameters. It is only determined by $N_{\rm s}$ and γ. This distribution-independent property allow us to choose an accurate α for unknown distributed parent distribution to make an accurate extreme estimation. Note that, the relative standard deviation (RSD) of α, defined as the ratio of the standard deviation over the mean, increases along with the increase of blocksize. Therefore, the choice of the blocksize should not be too large to avoid large RSD, and meanwhile keeps the total simulation cost low. On the other hand, a choice on α very small also should be avoided. This is due to the reason that the extreme value theory holds true when n, in this case, the blocksize, is sufficiently large. A small blocksize would lead to the inaccuracy of the GEV distribution, and eventually enlarges the extreme estimation error.

Because of the multiplier is distribution-independent, we are able to fit the function of α with respect to $N_{\rm s}$ and γ by using the normal distribution. Below gives the empirical function fit by a polynomial with the coefficient of determination R^2=0.9998,

$$\alpha = 0.83 + 0.35\gamma - 0.001N_{\rm s} - 0.18\gamma^2 + 3.5{\rm e}^{-7}N_{\rm s}^2 + 6.8{\rm e}^{-5}N_{\rm s}\gamma. \tag{10}$$

4.4 Experimental results of WCA and EVA

In this subsection, we show estimation results of our approach on two circuits: a two-stage miller Op-Amp (C1) and a folded-cascode Op-Amp (C2), and compare the results with that from other estimation

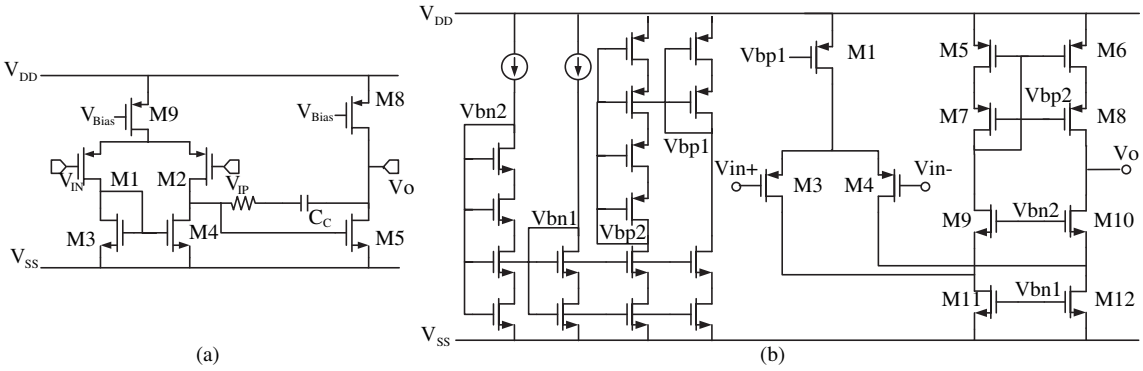

Figure 8 (a) Two-stage miller Op-Amp (C1) and (b) folded-cascode Op-Amp (C2).

Table 4 Comparison of estimation errors (%)

		Method 1			Method 2			Method 3			Proposed		
		Case 1		Case 2	Case 1		Case 2	Case 1		Case 2	Case 1		Case 2
		Fast	Slow		Fast	Slow		Fast	Slow		Fast	Slow	
C1	Gain (dB)	6.20	2.50	8.97	4.14	6.12	1.01	13.90	10.97	14.74	0.44	6.03	3.76
	V_{OS} (μV)	10.10	13.70	41.97	5.79	6.63	15.11	8.89	11.65	9.00	3.13	0.79	0.86
	SR (V/μs)	6.70	8.60	27.71	4.79	3.05	2.93	17.08	12.55	9.30	0.47	1.52	0.71
	Power (μW)	16.60	12.80	55.46	3.97	17.91	6.87	12.72	11.35	10.15	2.88	0.94	0.98
C2	Gain (dB)	3.70	2.10	13.71	10.68	1.17	6.40	8.53	16.35	10.67	5.65	3.76	4.97
	V_{OS} (μV)	5.70	9.80	3.90	6.61	2.95	7.09	11.76	7.48	9.30	0.87	0.86	2.05
	SR (V/μs)	10.20	12.50	73.43	3.56	3.20	8.14	4.43	10.16	16.16	1.97	0.71	0.29
	Power (μW)	9.70	10.70	4.95	3.97	24.50	24.54	13.46	12.50	12.17	1.90	0.98	3.05
Avg.Error		15			8			11			2.1		

methods, to verify the accuracy and efficiency of proposed method. Schematic views of C1 and C2 are given in Figure 8. Both circuits are simulated with TSMC 65 nm process technology. The design parameters are fixed. The numbers of statistical variables for C1 and C2 are 32 and 59 respectively. We perform our experiment on two extreme environmental variation cases: fast condition and slow condition. The block size N is 10 and we keep to increase the number of blocks $N_{\rm b}$ until normalized CIs are all below 0.2. We also simulate these test-benches by MC method with sample size equal to 100000, from which the 3σ value of each performance are used as the reference for the following comparison. Three MC-based methods are used to compare with, which are described as follows.

Method 1. Considering the performances are normal distributed, and calculating the mean and standard deviation from the same number of MC samplings.

Method 2. Fitting probability distribution function by using maximum likelihood estimation [39] on over ten common known parametric. The three sigma values are then calculated based on the PDF of best fitted distribution.

Method 3. Use kernel density estimation (KDE) to estimate the PDF of circuit performances.

Table 4 provides the estimation error comparison of these methods. The estimation error is defined as

$$\text{Estimation Error} = \left|\frac{P_{\rm est} - P_{\rm true}}{P_{\rm true} - P_{\rm avg}}\right|, \tag{11}$$

in which $P_{\rm est}$ is the estimated three sigma value, $P_{\rm avg}$ is the average value, and $P_{\rm true}$ is the true three sigma value. The average $N_{\rm b}$ for these two experiments is 44. However, we can further decrease the T to achieve less $N_{\rm b}$ by trading off the estimation accuracy.

Columns under Case 1 show estimation errors for fast and slow extreme environmental conditions, and columns under Case 2 show that when environmental variations are modeled as uniforms. For both cases, our approach is able to estimate performance three sigma worst values accurately. Furthermore, it shows good scalability on the complexity of circuits. C2 that contains more statistical parameter does not show

Table 5 Estimation errors with different number of blocks (%)

	$N_b = 20$		$N_b = 50$		$N_b = 100$	
	Case 1	Case 2	Case 1	Case 2	Case 1	Case 2
Gain (dB)	4.80	3.45	2.62	2.25	1.71	1.61
V_{OS} (μV)	3.04	3.58	1.84	2.39	1.10	1.35
SR (V/μs)	3.87	4.12	1.37	1.96	1.91	1.62
Power (μW)	2.77	2.80	2.05	1.78	1.56	0.77
Avg.Error	3.55		2.03		1.46	

Table 6 Estimation errors on different yield (%)

		2σ	3σ	4σ
C1	Gain (dB)	1.35	3.76	6.03
	V_{OS} (μV)	0.77	0.86	1.07
	SR (V/μs)	0.71	0.71	1.34
	Power (μW)	0.64	0.98	1.76
C2	Gain (dB)	1.28	4.97	4.75
	V_{OS} (μV)	0.62	2.05	3.45
	SR (V/μs)	0.48	0.29	1.05
	Power (μW)	0.66	3.05	4.49

accuracy degradation compared to C1. On the other hand, method 1 treats all performances as normal distributed which is not always the case, therefore shows large estimation errors on some performances. This inaccuracy becomes more obvious in Case 2, as shown in Table 4, that performance distributions are further diverted from normal distributions. The inaccuracy of methods 2 and 3 is caused by two aspects. The first aspect is the limited number of samplings that statistically only a few samplings are located at the tail of the distribution which makes the distribution fitting accuracy, especially at the edge of the distribution, deteriorated. The second aspect is that the performance variation distribution may not belong or similar to any of known distribution, therefore, deviates from fitted distribution that cause inaccuracy.

The overall estimation accuracy is influenced by the value of N_b, Table 5 shows the estimation accuracy on the performances of C1 with different N_b. The total number of samplings required increases proportionally as N_b increases, but shows better estimation accuracy.

The comparisons shown in Table 4 are at 3σ target yield. However, our method can be used on any target yield. Table 6 shows estimation results of Case 2 on C1 and C2 with different target yields. The estimation performance at high-sigma yield has slightly drop compared with the low-sigma case; however, the overall accuracy is still promising, which shows the attractive of our method for circuits require high-yield.

5 Circuit design with yield optimization

In this section, yield optimization experimental results are demonstrated on a Gain-boosted (GB) Op-Amp. The schematic view is shown in Figure 9. The complexity of this circuit made it not easy to be designed, even for experienced designers. The number of transistors including bias circuits and CMFB circuits up to 120, and it has as many as 253 PVT parameters for WCA. It is implemented in TSMC 65 nm technology node. The number of design parameters is 24. The distributions of process parameters are extracted from the technology library provided by the foundry, and voltage and temperature are modeled as uniform distribution. The block size for EVA is 10. The specifications are defined as follows: Gain $>$ 65 dB, Slew-rate (SR) $>$ 30 V/μs, Settling time $<$ 30 ns and Current Consumption (Idd) $<$ 600 μA. The experiment is conducted on a 4-core CPU system with 16 GB of RAM. The code is implemented in MATLAB and the Synopsys HSPICE is used as the simulator.

We perform five independent runs of yield optimization on this GB Op-Amp. The yield optimization

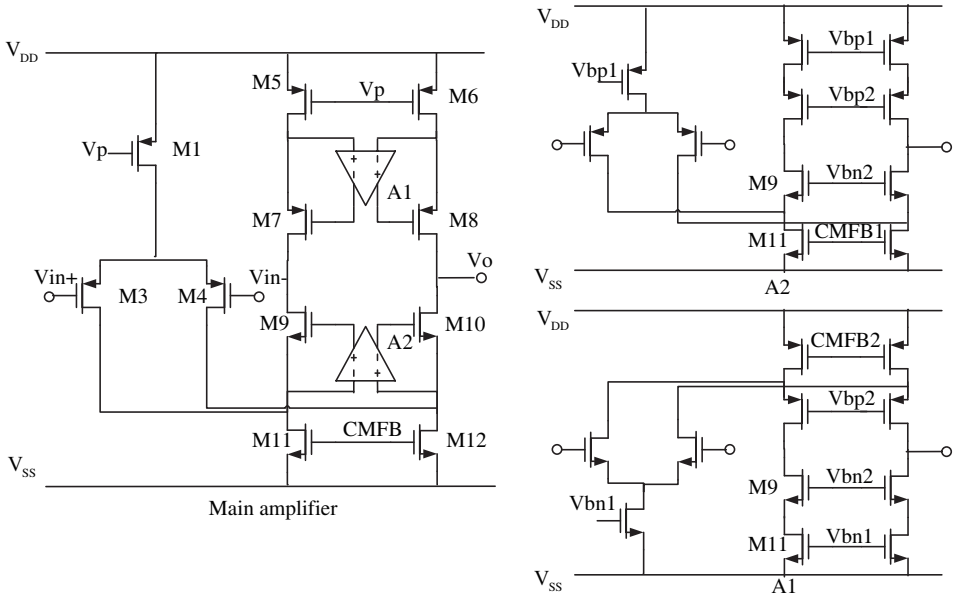

Figure 9 Fully differential gain-boosted amplifier.

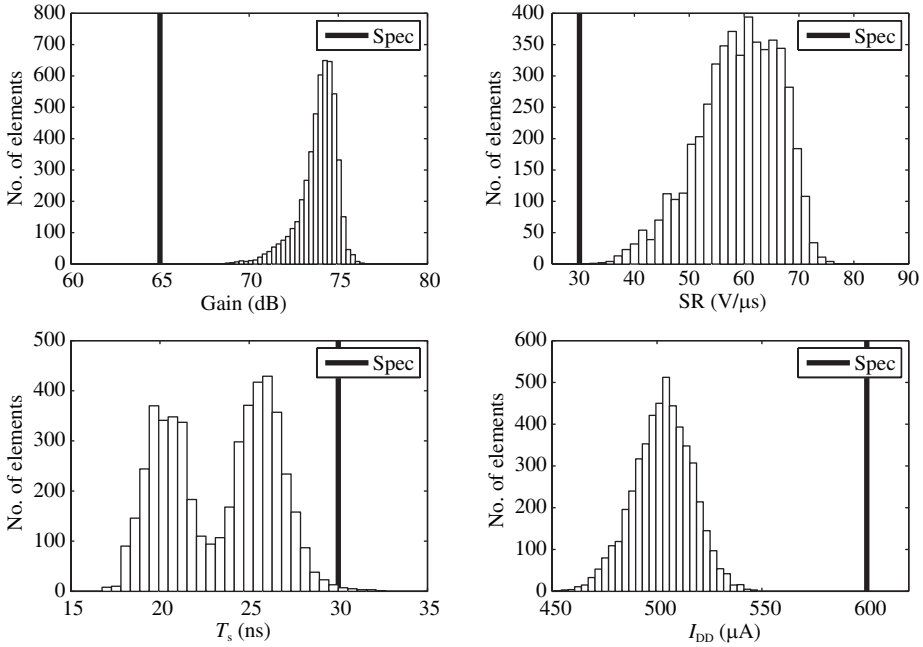

Figure 10 Experimental results.

Table 7 Yield optimization results (verified by 5000 MC samplings)

	Worst	Best	Average
Yield	98.5%	100%	99.6%
# of simulations	6327	2526	4677
Runtime (hour)	2.5	1.2	1.8

results are given in Table 7. They are verified by 5000 MC samples. The average performance yield from five runs is 99.6%. The worst yield (98.5%) occurs on the performance of settling time, which is less than the target yield (99.7%), this is caused by the estimation error. The histograms of one-run are shown in Figure 10. The average simulation count is less than 5000, and the yield optimization cost only 2 hours of runtime on average.

6 Conclusion

In this paper, a global performance and yield optimization framework, GOYE, has been proposed for analog circuits with the consideration of environmental variation and inter- and intra-die process variations. GOYE shows ultra-low computation cost without losing accuracy or compromising the optimized performance. The efficiency is achieved by several techniques/approaches, stated as follows.

(1) GOYE uses hybrid global optimization framework that combines global search phase and local optimization phase. A starting point selection technique called CVE is proposed and used in global search phase, which can select better promising initial points for local search. The state-of-art nonlinear optimization algorithm SQP is used as a local solver and a metric WVS is used during the local optimization to determine if the worst-case analysis is needed.

(2) Inspired by the extreme value theory, a novel worst-case analysis approach is proposed. In this approach, we convert the problem of finding the worst extreme value on original distribution to the problem of calculating the extreme value on its generalized extreme value distribution whose distribution is much easier to model from a handful of samples. This approach greatly enhances the efficiency for worst-case analysis without losing accuracy. Furthermore, this method is able to estimate worst-case performance for different target yield while keeping the same accuracy.

(3) Each stage of the framework is suitable for parallel computing which makes this framework more attractive in many-core and multi-node computing platform.

The proposed EVT-based method not only can be used in our optimization flow, it can also be used as standalone WCA tool, to fast estimate accurate n-sigma performance worst-case values. Beyond this, the innovation of this estimation method can be further extended to assess the extreme performance values with respect to design parameters. This application is able to help fast determination of topology selection, whether it is feasible to meet all design requirements before put effort onto the design.

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Conflict of interest The authors declare that they have no conflict of interest.

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