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Design for manufacturability and reliability in extreme-scaling VLSI

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Abstract In the last five decades, the number of transistors on a chip has increased exponentially in accordance with the Moore's law, and the semiconductor industry has followed this law as long-term planning and targeting for research and development. However, as the transistor feature size is further shrunk to sub-14nm nanometer regime, modern integrated circuit (IC) designs are challenged by exacerbated manufacturability and reliability issues. To overcome these grand challenges, full-chip modeling and physical design tools are imperative to achieve high manufacturability and reliability. In this paper, we will discuss some key process technology and VLSI design co-optimization issues in nanometer VLSI.

Keywords design for manufacturability, design for reliability, VLSI CAD

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1 Introduction

Moore's law, which is named after Intel co-founder Gordon Moore, predicts that the density of transistor on integrated circuits (ICs) roughly doubles every two years. In the last five decades, the transistor number on a chip has increased exponentially in accordance with the Moore's law. The semiconductor industry has followed this law for guiding research and development [1]. However, as the transistor feature size is further shrunk into extreme scaling (e.g., 10 nm and beyond), the industry is facing tremendous challenges in achieving high manufacturability and reliability.

The first key challenge comes from lithography limits and manufacturability. For a long time, the optical lithography has been utilized as the main driving force in shrinking transistor/interconnect feature size. However, the continued scaling of the minimum feature size has pushed the 193 nm wavelength lithography to its resolution limit, and the gap between the manufacturing capability and the design expectation becomes more and more critical. Therefore, new advanced lithography techniques have to be used to enable further pitch scaling beyond the single exposure with 193 nm wavelength lithography [2,3].

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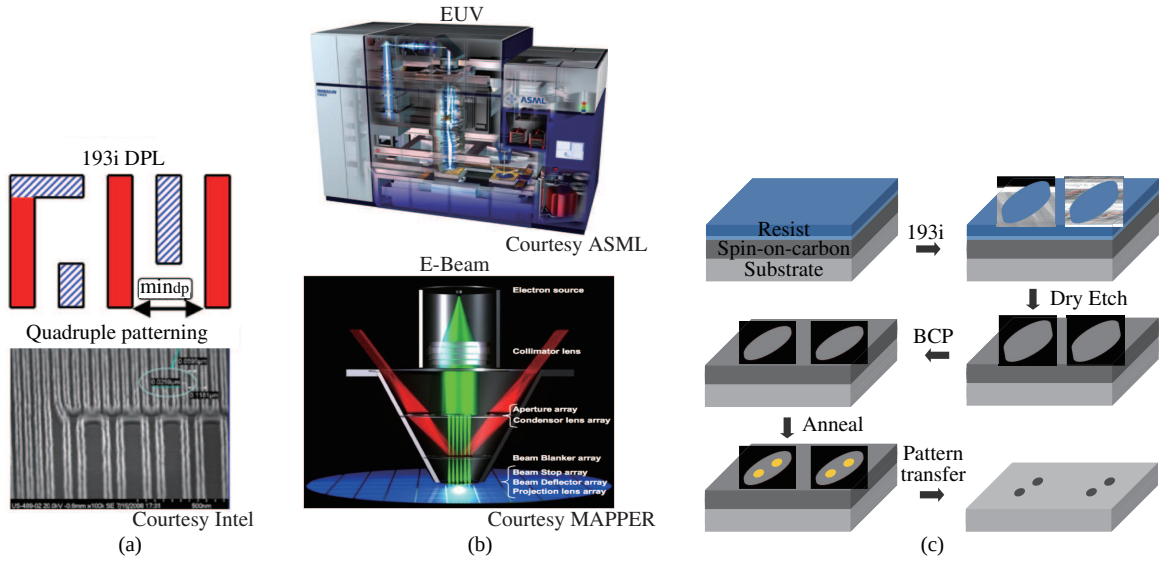

Figure 1 (Color online) Advanced lithography techniques. (a) Double patterning and quadruple patterning with 193 nm wavelength lithography; (b) extreme ultra violet (EUV) and electron beam lithography (EBL); (c) directed self-assembly (DSA) with pattern transfer.

In the near term, multiple patterning lithography (MPL) has become the most viable lithography technique. As illustrated in Figure 1(a), MPL splits target patterns into several masks so that the coarser pitches on each mask can be single patterned using the 193 nm wavelength lithography. Then patterns on different masks are combined to obtain finer pitches. According to different processes, MPL can be classified into LELE-type MPL and spacer-type MPL. LELE-type MPL includes double patterning lithography (DPL), triple patterning lithography (TPL) and quadruple patterning lithography (QPL), while spacer-type MPL includes self-aligned double patterning (SADP) and self-aligned quadruple patterning (SAQP). For the LELE-type MPL, it introduces complex coloring/stitching constraints and the overlay among multiple masks needs to be optimized to reduce the timing impact. For the spacer-type MPL, it provides better overlay control but prefers regular layout patterns due to more complicated coloring constraints. In particular, LELE-type DPL has been widely adopted in industry for 20/14 nm technology nodes. LELE-type TPL/QPL and spacer-type SADP/SAQP are promising and competitive candidates for 10 nm node and beyond due to the delay of other emerging lithography techniques.

In the longer term, next-generation emerging lithography technologies, including extreme ultra violet (EUV) lithography, electron beam lithography (EBL), and directed self-assembly (DSA), are under intensive research and development. EUV has very short wavelength (13.5 nm) to provide finer printing resolution compared to the 193 nm wavelength lithography as shown in Figure 1(b). However, tremendous challenges, such as power sources, resists and defect-free masks, have notably delayed the adoption of EUV for volume production. EBL directly uses the charged particle beam to pattern target layout features, as shown in Figure 1(b). As a maskless technology, EBL avoids the light diffraction from the mask, thus has been widely used in mask manufacturing and low-volume test chips. However, its throughput is still too low for electron beam direct-write on wafer for IC volume production. DSA enables sub-lithographic printing as shown in Figure 1(c). The guiding templates are first printed using the 193 nm wavelength lithography, and then they are filled with special chemical material such as block copolymer. After the annealing process, cylinders will be formed and transfered to substrate patterns with sub-lithographic pitches.

Another key nanometer IC challenge comes from reliability, which usually refers to how robust a chip is after manufacturing. The reliability issue profoundly impacts all aspects of circuits performance and may cause significant deviations from the prescribed specifications of a chip [4]. It can be soft error, or hard error due to aging, such as bias temperature instability (BTI), electromigration (EM), and so on. With continued feature size shrinking and increased transistor density, reliability issue is more and more severe.

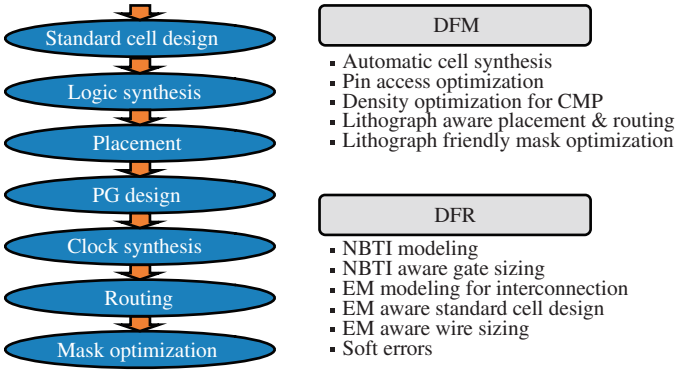

Figure 2 (Color online) Physical design flow and challenges for both DFM and DFR.

That is, reliable circuit operations cannot be guaranteed over the expected product lifetime. In addition, new materials and novel device architectures (e.g., FinFET) introduce new reliability threats [5].

To overcome these issues, full-chip modeling and CAD tools are imperative to achieve high printability and high reliability. Figure 2 shows a typical physical design flow, with related manufacturability and reliability concerns. On one hand, the advanced patterning techniques aforementioned impose additional physical design constraints, and call for new design-for-manufacturability (DFM) schemes across different design stages. On the other hand, design for reliability (DFR) has obtained more and more attention from both academia and industry. The conventional reliability aware design may force designers to use large design margins, which may limit circuit performance, and yet the circuit lifetime uncertainty still remains. How to model the variation or uncertainty, as well as how to intelligently balance circuit performance and reliability is key in DFR process.

In this paper, we will survey recent developments in design for manufacturability and reliability in extreme-scaling VLSI, including challenges, solutions, results, and future research directions. The rest of this paper is organized as follows. In Section 2 we will discuss the design for manufacturability issues. In Section 3 we will cover the design for reliability issues, followed by conclusion and future directions in Section 4.

2 Design for manufacturability (DFM)

In emerging technology nodes, manufacturability becomes a more and more severe issue, even with various resolution enhancement techniques, e.g., optical proximity correction (OPC), phase shift mask (PSM), and sub-resolution assist feature (SRAF) insertion. To overcome the manufacturing problem and improve circuit yield, several early design stages should be aware of the manufacturing constraints. In this section, we discuss how manufacturability can be seamlessly considered in four physical and mask design stages: standard cell design, placement, routing, and mask optimization.

2.1 DFM in standard cell design

As the foundation for the back-end design flow, the standard cell library design plays an important role in the physical design closure. Due to the ever-increasing DFM challenges in advanced technology nodes, standard cell designers spend huge amount of efforts to achieve manufacturing friendliness [6–8]. The complex DFM constraints introduce undesirable interactions across neighboring standard cells during the placement and routing stages. This means that designers not only need to improve the manufacturability for each individual standard cell, but also need to consider the lithographic interactions across cell boundaries when cells are placed next to each other. Therefore, standard cell design and evaluation considering DFM constraints are critical to obtain a robust cell library that can be used in any design implementation.

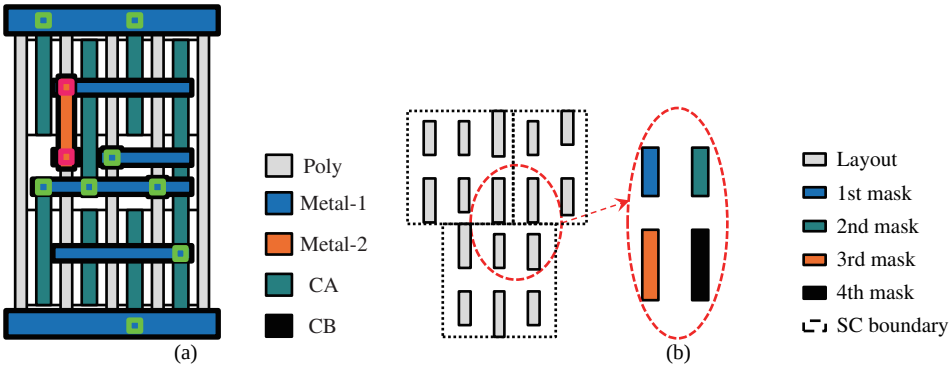

Figure 3 (Color online) (a) An standard cell with regular layout patterns; (b) 3-cell interactions under MPL-specific constraints.

For an individual standard cell design, regular layout styles have been extensively used across various layers, such as the middle-of-line (MOL) layers, to obtain lithography-friendly layout. An example for regular layout patterns is shown in Figure 3(a), where layout patterns for intra-cell connections are unidirectional. Although manual standard cell designs are still widely used to get the best performance/area/power, etc. [7, 8], automatic standard cell synthesis has been actively studied to achieve comparable design quality and shorter turnaround time [9–15]. Taylor et al. [9] and Maly et al. [10] have early studies on applying regular layout patterns in standard cell synthesis. Considering the simplicity and discreteness of regular layout patterns, various combinatorial optimization techniques have been proposed for standard cell synthesis while accommodating complex DFM constraints. Taylor et al. [9] and Wu et al. [13] introduce the branch and bound method with smart pruning techniques for the cell layout generation. For the regular layout towards 1-D gridded design, line-gap distributions are explicitly optimized in [11, 13] to improve the manufacturing yield. Ryzhenko et al. [12] propose the boolean satisfiability (SAT) formulation for the cell layout generation. Hougardy et al. [14] and Ye et al. [15] further propose the integer linear programming (ILP) method for the cell layout synthesis with consideration of practical DFM constraints. During library design phase, designers aim at a robust standard cell library that is applicable in any design implementation. In advanced technology nodes, MPL-specific violations may be introduced across multiple cell instances placed next to each other, which makes the robust standard cell library design ever-challenging [16]. Figure 3(b) illustrates the 3-cell interaction introduced by the MPL coloring constraints. Quadruple patterning, i.e., 4 colors, is needed to achieve color assignment for the layout patterns in the circle window. However, if triple patterning is used, it becomes an illegal cell combination due to the TPL conflict. A robust standard cell library should minimize the number of illegal cells or combinations of cells. Xu et al. [16] propose the first framework for the library robustness evaluation over MPL-specific constraints. During library design stage, a compact set of illegal cells or combinations of cells are quickly computed so that designers can improve the associated layout incrementally.

Moreover, due to the continued density and area scaling, limited number of routing tracks are available for the standard cell design. The Input/Output (I/O) pin access becomes more and more difficult because each I/O pin has limited number of access points and they interfere with each other under restrictive MPL constraints. Xu et al. [17] introduces the pin access optimization (PAO) technique considering the MPL-specific constraints for the metal and via layers. As shown in Figure 4, the line-end extensions beyond the via positions are necessary to achieve SADP-friendly Metal-2 wires for pin access. The pin access and cell layout co-optimization is further proposed to maximize the pin access flexibility for the routing stage.

2.2 DFM in placement

Traditional placement problem for physical design has been studied for almost half a century and plenty of useful techniques have been proposed to improve the placement engines. However, due to the rapid

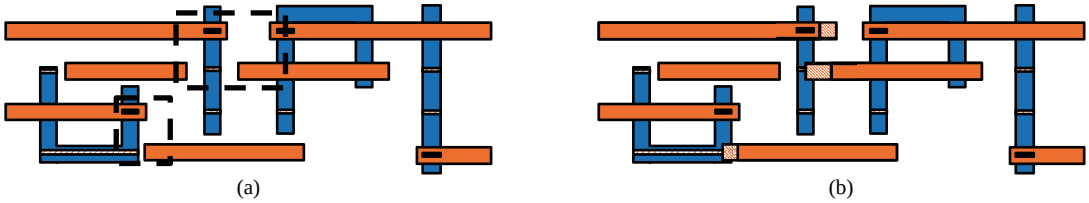

Figure 4 (Color online) PAO for one pin access candidate. (a) SADP design rule violations in the dashed rectangles; (b) optimized Metal-2 wires with line-end extensions for pin access [17].

development of technology node along with more and more complicated design rules, consideration of manufacturing effects in early design stage has become a necessity. Researches on manufacture aware placement follow the advancement of manufacturing process and try to resolve challenges for specific process technology.

Manufacturing objectives are typically formulated into cell abutting cost or constraints; i.e., there will be additional cost if two specific types of cells are placed next to each other. Due to the existence of wide horizontal power grid in row based structure, standard cells can be regarded as vertically isolated, but cells can be very close to each other in horizontal direction. Therefore, horizontal abutting often requires more attention during placement for lithography awareness.

Hu et al. [18] propose incremental placement algorithms to honor refractive effects in lithography for 45 nm technology. The lithography effects are formulated into abutting cost for each cell pair. Cell flipping and local movement are introduced to minimize total cost along each placement row. Chen et al. [19] propose the first metal-density-driven placement engine to reduce variation during chemical-mechanical polishing (CMP). They integrate a predictive CMP model into the placement algorithm and optimize metal density globally. Besides deterministic approaches, Shim et al. [20] study the property of inner-cell margin and came up with a new placement problem with defect probability minimization as the objective. It is argued in their paper that inner-cell margin is not always necessary to avoid lithography defect. They propose probability based approach along with simulated annealing algorithm to reduce defect probabilities.

With the increasing popularity of multiple patterning lithography (MPL), the placement problem related to MPL has also been studied deeply, including double patterning lithography (DPL) [21–23], self-aligned double patterning (SADP) [24], and triple patterning lithography (TPL) [25–30]. To achieve DPL friendly layout, Gupta et al. [21] study the timing model for cell layouts under DPL and a dynamic programming based algorithm is proposed to solve coloring conflicts. To further improve DPL friendliness, a new DPL design flow is proposed including cell-level design, DPL aware placement, and DPL aware routing [22]. The coloring problems are considered during placement, routing and post-routing stages so that better manufacturability is achieved. Gao et al. [24] solve decomposition conflicts for SADP at placement stage with cell flipping and spreading.

In TPL placement, the major lithography objective is to avoid coloring conflicts while minimizing number of stitches. The conflicts come from identical color assignment to vias or metal-1 wire segments at the boundary of cells. However, the color assignments remain undetermined in conventional physical design flow where layout decomposition is performed after placement and routing. Therefore, in the TPL friendly flow proposed by Yu et al. [31], standard cells are pre-colored with candidate coloring solutions and a look-up table (LUT) is constructed to store all the candidates. Although there might be large amount of coloring solutions for even a single cell, the number of pre-coloring solutions is limited due to the observation that only wire segments near cell boundary matter. Only color assignments for boundary segments need to be enumerated, which reduces the solution space to a large extent. Figure 5 shows an example of conflict between two abutting cells with specific coloring solutions, either inserting some whitespace between two cells or switching the coloring solutions will resolve the conflict. Hence, the placement problem consists of two parts: optimizing wirelength as the conventional objective, and avoiding conflicts and minimizing stitches as the lithography objective by determining the locations and coloring solutions of cells. Several graph based algorithms are proposed to determine cell locations and

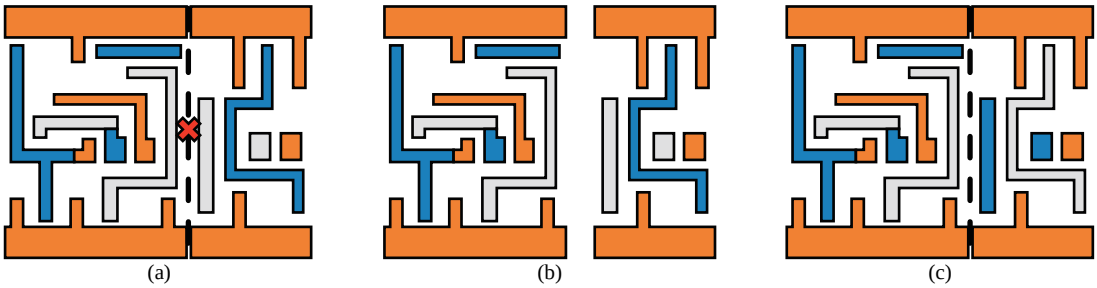

Figure 5 (Color online) (a) An example of TPL conflict; (b) conflict removal by whitespace insertion; (c) conflict removal by switching coloring solutions.

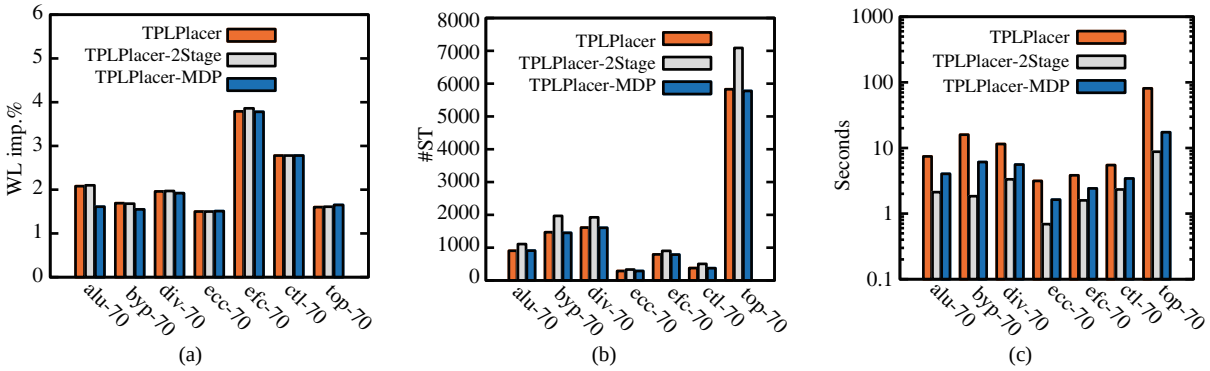

Figure 6 (Color online) Experimental results of different algorithms in TPL placer from Yu et al. [28] on benchmarks with 70% utilization. (a) Wirelength improvement, (b) number of stitches, and (c) runtime.

coloring solutions simultaneously for each placement row. Kuang et al. [26] further extend Yu's flow by predetermining coloring solution for each standard cell and try avoiding conflicts only by placement techniques. Chien et al. [29] also propose different approaches to solve detailed placement and cell decomposition problems.

Tian et al. [25] and Lin et al. [27] argue that cells of the same type should have the same color assignment for better timing variation. This additional constraint results in the NP-completeness of the problem even for ordered single row version [27]. With further shrinking of feature sizes, middle-of-line (MOL) layers are introduced for local interconnection, which is possible to cause cross-row conflicts. Lin et al. [30] study the layout patterns of MOL layer and show that it is more feasible to avoid four-way clique (K4) structure than pre-coloring MOL layer. They develop a framework to handle conflicts in both Metal-1 and MOL layers simultaneously.

Besides general lithography and MPL aware placement, there are some other researches focusing on emerging technology, like electron beam lithography (EBL), extreme ultra violet (EUV), and Directed Self-Assembly (DSA) [32–35]. For example, in EBL, due to the application of multiple electron beam lithography (MEBL) for throughput improvement, the features at boundaries of beams are susceptible to stitch errors. Therefore, it is necessary to avoid features near such regions for better manufacturability, which needs to be considered during both placement [32] and routing [36]. For this problem, Lin et al. [32] propose a linear time dynamic programming algorithm for simultaneous optimization on wirelength and stitch errors.

Figure 6 shows the performance of three algorithms in the TPL aware placer proposed by Yu et al. [28]. "`TPLPlacer`" denotes the algorithm that is able to determine cell coloring solutions and positions simultaneously with a graph model. Each cell is allowed to shift to any placement site in a row with given order of the cell sequence. The drawback for this algorithm lies in the runtime overhead from large graph size. The runtime complexity is related to product of number of cells, total number of placement sites, and amount of candidate coloring solutions for each cell. The number of placement sites in each row can be quite large, resulting in expensive computational efforts, as shown in Figure 6(c).

"`TPLPlacer-2Stage`" divides the previous strategy into two stages to overcome the speed overhead. That is, the coloring solutions are first determined; then in the second stage, cells are shifted to avoid coloring conflicts. Although it is necessary to solve graph models in both stages, these graphs turn out to be much smaller and easier to solve. The benefits in runtime can be seen in Figure 6(c), while the solution quality degrades in terms of stitch numbers, shown as Figure 6(b). The third algorithm, "`TPLPlacer-MDP`", tries to trade-off quality and runtime in another perspective by limiting the range of movement for each cell. Instead of allowing cells to be placed in any positions, it constrains cells in such a way that they can only be shifted to their neighboring sites. A dynamic programming algorithm is proposed to solve the constrained problem. Figure 6 (a) and (b) show that it can achieve almost the same solution quality as that of "`TPLPlacer`", while the runtime is reduced dramatically.

2.3 DFM in routing

In 14 nm technology node and beyond, MPL is needed for routing patterns with tight pitches on lower metal layers, such as Metal-2 and Metal-3. Novel routing strategies are crucial to obtain legal routing results while accommodating MPL-specific constraints. LELE, i.e., double patterning (DP), aware detailed routing is first studied by Cho et al. [37] with a grid-based approach, where colors of grids are assigned during the routing stage to obtain LELE-friendly routing patterns. Yuan et al. [38] further incorporate redundant-via considerations during DP aware routing with an integer linear programming (ILP) formulation. Lin et al. [39] propose the innovative conflict graph to enable efficient DP conflict detection and removal along with the sequential routing. Lin et al. [40] further introduce the comprehensive conflict graph to obtain a novel gridless routing scheme considering DP, optical proximity correction and balanced mask density simultaneously. Moreover, for the MP aware routing with more than two LE steps, such as TPL, the coloring conflict detection and removal will be much more sophisticated due to the difficulties from the color assignment and overlay control. Different from methodologies based on the conflict detection and removal, Ma et al. [41] propose a routing grid model with expanded grids to deal with the TPL constraints systematically. Due to high complexity of color assignment for TPL, Lin et al. [42] propose a token graph-embedded conflict graph to enable the TPL conflict detection and achieve TPL-friendly routing patterns in a correct-by-construction manner. A conflict pre-coloring based approach is proposed in [43] to avoid stitches in the routing patterns and improve the manufacturing yield. Liu et al. [44] argue that an iterative ripup and reroute approach can achieve TPL-friendly routing patterns with better solution qualities.

In future technology nodes, regular routing patterns towards 1-D gridded design are preferred due to better manufacturability and simplified coloring schemes [45]. The spacer-type MPL is potentially attractive for lower metal routing layers due to its better control on overlay and line edge roughness. Mirsaeedi et al. [46] present the first study on the self-aligned double patterning (SADP) aware routing with the grid-based approach. Gao et al. [47] propose prescribed layout planning schemes to obtain SADP-friendly routing patterns with better solution qualities. Kodama et al. [48] introduce simple connecting and cutting rules during grid color assignment to achieve SADP/SAQP-friendly routing results. Instead of assigning colors to grids, Du et al. [49] propose an expanded routing grid model to deal with the SADP-specific constraints, where a negotiation congestion-based routing scheme is adopted during the routing stage. Liu et al. [50] further demonstrate an overlay constrained graph to guide the router and achieved better solution qualities. Fang et al. [51] introduce a novel wire planning scheme to enable full-chip routing with cut mask optimization for general self-aligned multiple patterning. While most of the spacer-type MPL aware routers focus on the spacer which is dielectric type of manufacturing scheme, Ding et al. [52] introduce a color pre-assignment and an expanded graph model to deal with the spacer which is metal type of manufacturing scheme.

Furthermore, MPL-specific constraints have introduced complex neighboring interactions among routing patterns. The local standard cell pin access is becoming extremely difficult since the router needs to access congested I/O pins within limited number of access points while accommodating complex neighboring interactions. To improve the standard cell pin accessibility, Xu et al. [53] propose pin access

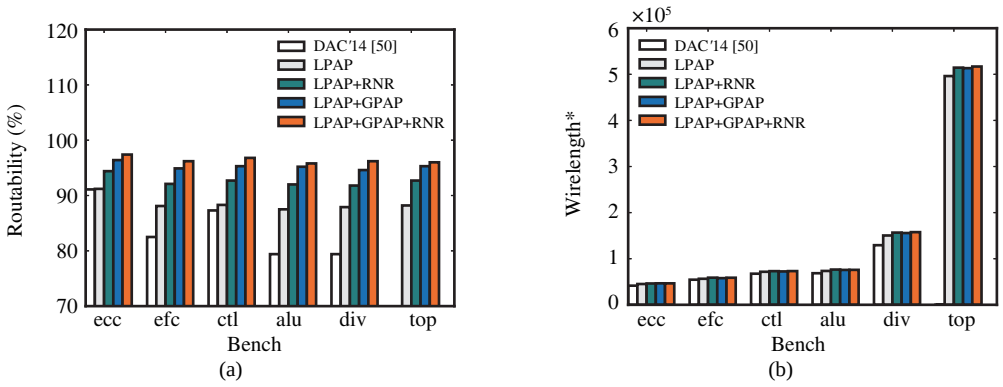

Figure 7 (Color online) SADP-friendly detailed routing with pin access planning schemes for various OpenSPARC benchmarks. Specific pin access planning schemes include local pin access planning (LPAP), global pin access planning (GPAP) and pin access driven rip-up and reroute (RNR).

planning strategies, including local pin access planning (LPAP), global pin access planning (GPAP) and pin access driven rip-up and reroute (RNR) to enable the handshake between library-level pin access and the detailed routing stage, which obtains SADP-friendly routing patterns and better solution qualities compared with a state-of-the-art SADP-aware detailed router [50]. Figure 7 demonstrates the comprehensive comparisons among various routing strategies, including the detailed router [50], "LPAP", "LPAP+RNR", "LPAP+GPAP" and "LPAP+GPAP+RNR". The solution qualities are measured by "Routability" and "Wirelength*" in Figure 7 (a) and (b), respectively. "Routability" is defined as the number of routed nets over the total number of nets in the design. It is difficult to achieve 100% routability owing to the problem complexity. For the benchmark "top", the results of DAC'14 [50] are not shown in Figure 7 (a) and (b) because the routing cannot be finished within affordable amount of runtime. "Wirelength*" is defined as the summation of routed wirelength of routed nets and half-perimeter wirelength of un-routed nets. Figure 7(a) demonstrates that the scheme of "LPAP+GPAP+RNR" achieves the highest routability compared to other schemes, including a 10% routability improvement on average over [50]. Figure 7(b) illustrates comparable "wirelength*" among different strategies. It shall be noted that, since the scheme of "LPAP+GPAP+RNR" obtains highest routability, we expect the "wirelength*" metrics of other schemes will increase significantly if similar routability could be achieved. Therefore, the proposed pin access planning schemes are critical to obtain high-quality routing solutions while satisfying complex SADP-related constraints in advanced technology nodes.

2.4 Mask optimization

2.4.1 *MPL layout decomposition*

One of the biggest challenges in multiple patterning lithography (MPL) is the mask assignment problem. Since each mask is manufactured by 193 nm optical source, there is a requirement on the distance between any two patterns belonging to the same mask. If any two patterns in a mask fail to meet the requirement, they are not able to be printed well and thus result in a conflict. The process of splitting layout into several masks is called *layout decomposition*. The requirement for layout decomposition varies from different lithograph techniques, but the major objective is to avoid conflicts.

LELE-type MPL decomposition is typically formulated into graph coloring problem, as mask assignment is very similar to vertex labeling; e.g., DPL layout decomposition corresponds to 2-coloring and TPL layout decomposition corresponds to 3-coloring. However, layout decomposition is still different from traditional graph coloring problem due to the existence of stitches; i.e., a wire segment can be split into multiple parts and assigned to separate masks to resolve conflicts. Even though stitches are able to remove conflicts, they should not be abused for the reason of overlay and misalignment issues [54]. Therefore, the typical objective in LELE-type MPL decomposition is to minimize both conflicts and stitches with higher weights of conflicts over stitches. Figure 8 shows an exmaple of DPL layout decomposition.

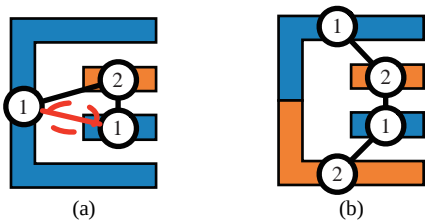

Figure 8 (Color online) An example of (a) DPL layout decomposition with conflict and (b) conflict removal by stitch insertion.

Without stitch insertion, there would be a coloring conflict shown by the red edge of Figure 8(a), but it is resolved by splitting the wire segment, shown as Figure 8(b).

For DPL layout decomposition, Anton et al. [55] study its feasibility from process windows' perspective. While it is true that 2-coloring can be solved by odd cycle detection, the problem becomes more complicated with the adoption of stitches. Kahng et al. [56], Yuan et al. [57] and Xu et al. [58] propose ILP based approaches to minimize conflicts and stitches simultaneously. Xu et al. [59] propose polynomial time optimal algorithms to solve the conflict graph when it is planar. Tang et al. [60] also take advantage of planarity and solve decomposition with min-cut based approach. Yang et al. [61] further consider lithography impact such as density control and variation reduction.

The problem of TPL and QPL decomposition for general layout has been proved to be NP-hard [62]. The first ILP formulation for TPL comes from Yu et al. [63] and a semidefinite programming (SDP) based algorithm is proposed to achieve approximate results. The SDP formulation is further extended to handle arbitrary k-coloring problem [64], shown as (1). Here k equals to 3 for TPL and 4 for QPL.

$$\begin{aligned} \min \quad & \sum_{e_{ij}\in \mathrm{CE}} \left(\vec{v_i} \cdot \vec{v_j} + \frac{1}{k-1} \right) + \alpha \sum_{e_{ij}\in \mathrm{SE}} (1 - \vec{v_i} \cdot \vec{v_j}) \\ \text{s.t.} \quad & \vec{v_i} \cdot \vec{v_i} = 1, \quad \forall i \in V; \\ & \vec{v_i} \cdot \vec{v_j} \geqslant -\frac{1}{k-1}, \quad \forall e_{ij} \in \mathrm{CE}. \end{aligned} \tag{1}$$

Several follow-up researches propose algorithms to solve the problem by trading off performance and runtime [65–67]. For row based layout structure in which rows are assumed to be separated by wide power grids, the layout decomposition problem can be solved in polynomial time [68–71].

Spacer-type MPL typically refers to SADP and SAQP. Both techniques require efficient decomposition method for layout configuration. However, they impose stricter constraints on width and spacing rules than LELE-type MPL, and stitch insertion is not allowed. The discrepancy between trim mask patterns and original layout further complicates the layout decomposition.

Mirsaeedi et al. [72] and Zhang et al. [73] propose ILP formulations to solve SADP layout decomposition. The ILP formulation is flexible that it can integrate other objectives like lithography hotspots, but the runtime is a challenge for this approach. Ban et al. [74] propose an SADP layout decomposition framework for 2D layout structures. The problem is formulated into a 2-coloring problem (see Figure 9), where a blue color denotes a pattern manufactured by the mandrel mask, while a red color represents a pattern for the trim mask. In 2D layouts, it is possible to have inherent conflicts such as B and C. Once such kind of conflicts are detected, original core masks should be merged smartly so that undesired patterns can be trimmed out by the trim mask. After the removal of all conflicts, layout decomposition can be solved with 2-coloring techniques. Xiao et al. [75] show that 2-colorability is necessary to achieve an SADP decomposition solution without any overlay. They propose a new graph formulation and solve a 2-SAT problem in polynomial time, which guarantees to return a valid solution as long as one exists. Then merging techniques are employed to explore larger solution spaces for standard cell row-structure layout [76].

Zhang et al. [77] define several geometry rules of SAQP-friendly design and introduce a method for SAQP decomposition. Kang et al. [78] introduce some methods on SAQP decomposition. Similar princi-

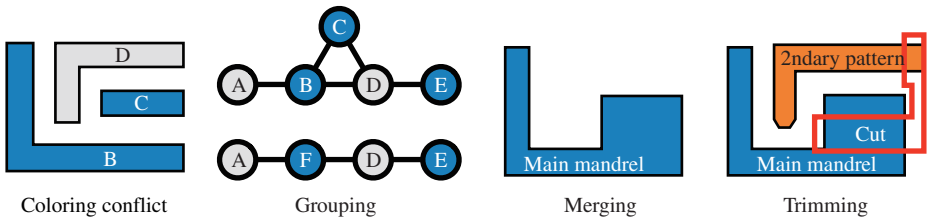

Figure 9 (Color online) Grouping and merging coloring for spacer-based multiple patterning [74].

ples in SADP can be applied to SAQP. However, SAQP decomposition for 2D layout is still challenging, and there are very limited efficient studies on self-aligned multiple pattern (SAMP). The overlay issue for space-type MPL can be mitigated by various approaches, but it cannot be completely avoided due to the misalignment of trim mask. Thus, overlay reduction and hotspot detection are still important for layout decomposition.

Directed self-assembly (DSA) is gaining strong interests from academia and industry to improve both throughput and resolution, thus it is a potential candidate for sub-7nm technology nodes [79–81]. Self-assembly is a process that block copolymer (BCP) forms organized nanoscale structures. This process usually happens during the thermal annealing when BCP phase separation occurs to generate spherical, lines, or cylinders inside a guiding template. The DSA guiding template used to guide the BCP is printed using the 193 nm optical lithography process. The size and shape of the self-assembled structures can be tuned by the composition of BCP, molecular weights, and so on. Graphoepitaxy and chemoepitaxy are two common methods to direct BCP self-assemble. DSA with topographical graphoepitaxy technique is mainly for contacts/vias layer fabrication [82–84].

Due to the phase separation property, DSA has the ability to reduce the pitch of contacts/vias, thus can reduce mask number by grouping two or more contacts/vias inside one template. The contacts/vias can be grouped in one template if their distance is within the natural pitch (L_0) and the maximum distance defined the block copolymer. There is minimum lithography distance requirement for the guiding template as it is printed by 193i lithography. However, it is necessary to take into account the pitch variation of cylinders and DSA guiding templates. Refs. [79, 84] have mentioned that for very complicated DSA patterns, the placement error of cylinders could deteriorate, and some unwanted cylinders can be formed in some extreme cases. Thus in order to have good control of variation, the shapes of DSA guiding templates are generally restricted. Besides, the pitches of DSA cylinders are the same for a certain composition of BCP materials. There are several studies targeting at the optimization of DSA-aware design. Du et al. [85] propose an SAT algorithm and bounded approximation algorithm to explore the DSA aware contact layer optimization for 1D standard cell library. Xiao et al. [86] study the DSA template determination and cut redistribution for cut mask in 1D gridded design, while Ou et al. [87] extend the problem by formulating it to an ILP problem and further propose heuristic methods. Fang et al. [88] study the post-routing redundant via insertion with DSA pattern constraints. Shim et al. [34] propose a strategy to reduce the grouping conflicts on the boundary of different standard cells during post-placement stage.

For the printing of dense distributed contacts/vias in advanced technology node, multiple patterning lithography (MPL), such as TPL and QPL, would be required [89]. MPL with DSA together can help to further reduce the cost of masks in the fabrication process, which is sometimes referred as DSA-MP hybrid lithography. It is noted that decomposition of contact/via for DSA is different from the decomposition of metal lines, as we need to assign contacts or vias to different guiding templates. How to group these contacts/vias during decomposition remains to be an open problem. Firstly, the grouping of contacts/vias and decomposition cannot be separated, instead, they should be done simultaneously in order to get the optimized result. Secondly, the mask complexity of guiding template and placement error of different DSA groups should be considered. Generally speaking, the placement error of the target and final contact may be worse when more contacts are grouped in one template. Therefore, if grouping is performed before decomposition, we may obtain more complicated guiding templates and some conflicts,

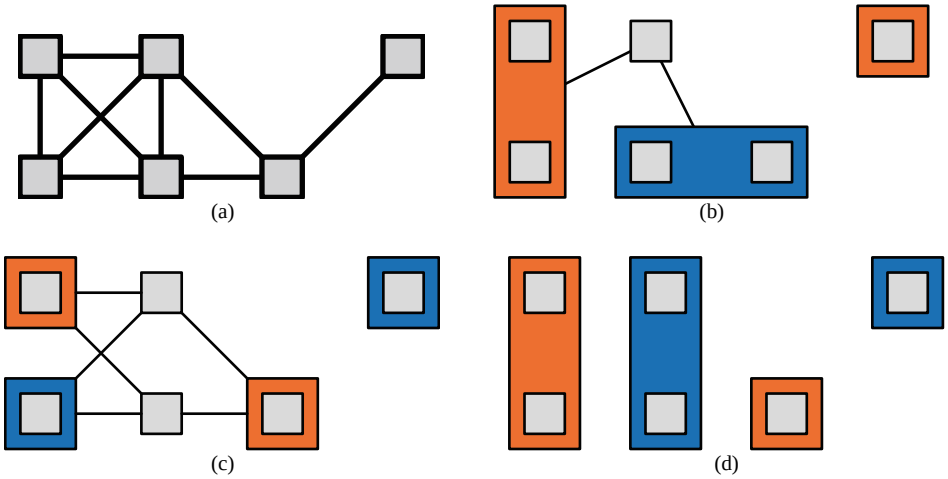

Figure 10 (Color online) (a) Original contact; (b) group first GTA; (c) decomposition first GTA; (d) simultaneous GTA.

as shown in Figure 10(b). If decomposition is performed before grouping, we may need more masks for DSA, as shown in Figure 10(c). While grouping and decomposition are considered concurrently, the optimal guiding template assignment (GTA) with minimum placement error and cost for DSA multiple patterning can be achieved, as shown in Figure 10(d). Badr et al. [90] propose a simultaneously grouping and MPL decomposition through ILP formulation, as well as a maximum matching based heuristic method to solve this problem.

2.4.2 *EBL layout fracturing*

Electron beam lithography (EBL) is a maskless technology that directly prints target patterns on wafer [91]. EBL is widely used in the fabrication of masks and it is also a promising candidate for advanced technology nodes due to the ability of accurate pattern generation. The conventional EBL system is based on variable shaped beam (VSB). In VSB, layout fracturing is a fundamental step where layout is decomposed to various non-overlapping rectangles, and the rectangles would be shot by electron beams sequentially. Thus the cost and throughput of EBL writing is directly affected by the number of fractured rectangles. However, the number of rectangles increases dramatically for highly scaled technology nodes. First, more polygons need to be fractured as the volume of layout patterns is much larger with the decrease of minimum feature size. Besides, the mask complexity is higher due to more strict optical proximity correction (OPC) complexity. Last but not least, in emerging technology nodes, more masks are required for multiple patterning lithography (MPL).

Since the low throughput and long runtime are still the bottleneck of EBL system, several methods have been proposed to improve layout fracturing in order to increase the system throughput. For the conventional rectangle fracturing, as illustrated in Figure 11(a), the electron beam passes through two shaping apertures to form the targeted rectangle patterns. Refs. [92, 93] formulate this problem to an ILP, and also propose some speed-up techniques. Ma et al. [94] present a heuristic algorithm for rectangle fracturing and sliver reduction. Compared to rectangle fracturing, the L-shape fracturing is an effective way to further reduce the number of shots [95–97]. For the L-shape fracturing strategy as illustrated in Figure 11(b), an additional shaping aperture is employed to form the L-shape shots. However, the number of L-shape shots can be reduced by 50% compared to rectangle fracturing strategy. Ref. [95] reports the L-shape fracturing can reduce about 38% shots without providing any algorithm details. Refs. [98, 99] propose several heuristic methods to decompose polygon to L-shapes. To address L-shape decomposition problem, Yu et al. [100] propose two methods, where the first one is rectangular merging (RM) algorithm to merge the rectangles to form L-shape fracturing, while the second one is direct L-shape fracturing method to directly fracture the layout pattern into L-shapes with sliver minimization.

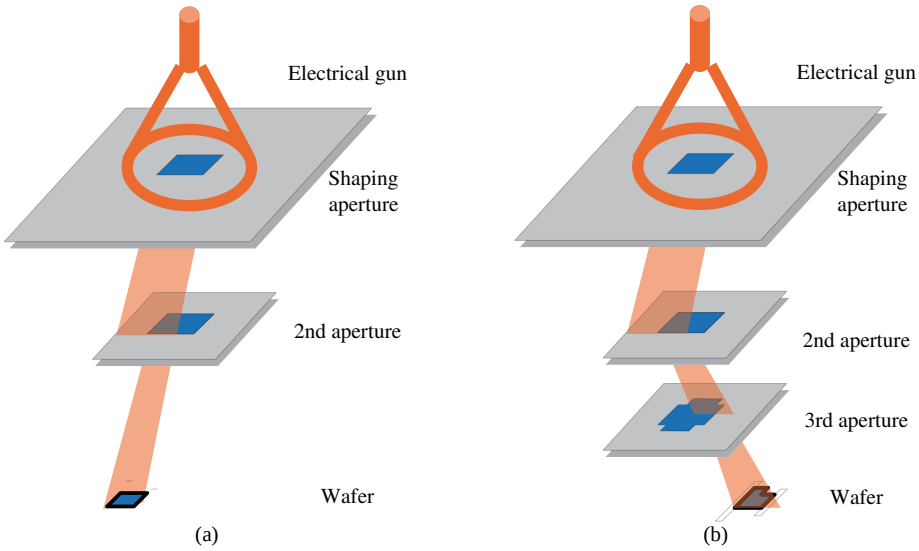

Figure 11 (Color online) (a) Traditional rectangular EBL writing process; (b) L-shape writing process with one additional aperture.

2.4.3 *Mask layout hotspot detection*

The 193 nm wavelength lithography is still the mainstream for pitch scaling in advanced technology nodes, with help from the design for manufacturability (DFM) techniques discussed in preceding sections. However, even with complex source/mask optimizations for a single exposure, lithography hotspots still exist after the patterning processes as shown in Figure 12. Therefore, in physical verification stage, detecting and fixing these lithography hotspots beforehand play an important role in improving production yield.

Lithography hotspot detection has been extensively studied in the CAD community involving various approaches, such as computational lithography simulation [101, 102], pattern matching [103–107] and machine learning [108–115]. Computational lithography simulation achieves high-accuracy hotspot detection using pattern contours simulated with lithography models [101, 102]. However, the expensive computational cost makes it unscalable to the full-chip layout. Patterning machine based approach enables the hotspot detection depending on a library of pre-stored hotspot patterns and a matching algorithm [103–107]. The library matched testing pattern is identified as a hotspot. The fuzzy pattern matching targets at matching under some similarity metrics instead of the exact matching. The pattern matching based approach may lack the capability to predict never-seen hotspots, even with the fuzzy pattern matching algorithms applied. By contrast, machine learning based hotspot detection aims at training a classification model with a set of training data, then the classification model will be used to decide whether any input layout is a hotspot or not based on the feature vector extracted from that particular layout. In other words, machine learning based approach can detect never-seen hotspots but it will also possibly generate false alarms, i.e., lithography-friendly layout is falsely identified as a hotspot. Generally speaking, machine learning based approach is susceptible to overfitting problem, which makes the training data preparation and parameter tuning particularly important. To balance the strength of the pattern matching and machine learning based approaches, some studies combines them, such as fuzzy matching with learning in [107] and meta-classifier in [112], to obtain better performance on the hotspot detection.

3 Design for reliability (DFR)

As technology scales, circuit reliability has become a prime concern in modern semiconductor industry than ever before, due to various aging and wearout effects, such as bias temperature instability (BTI),

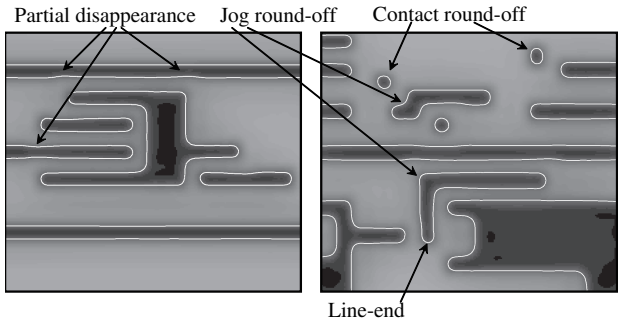

Figure 12 Examples of lithography hotspots [112].

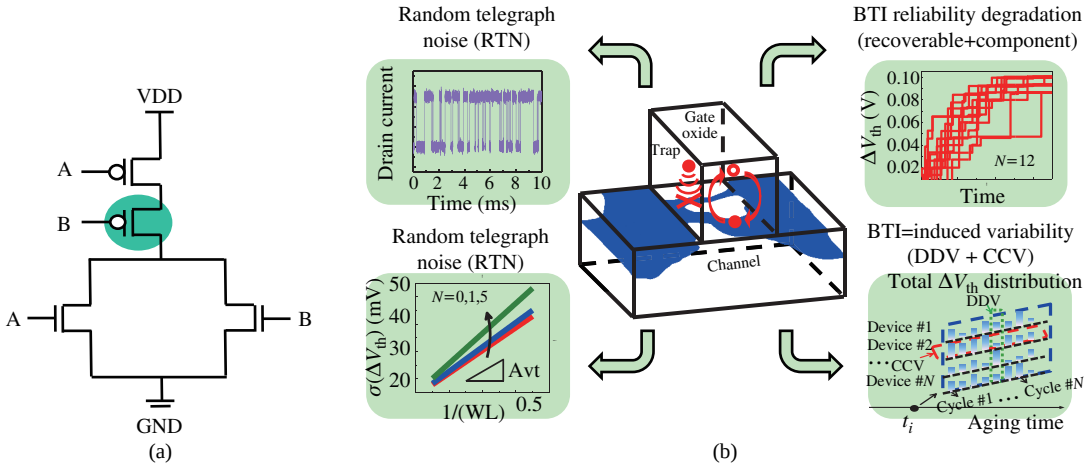

Figure 13 (Color online) (a) Stacking effect in NOR gate; (b) various reliability/variability issues induced by gate oxide traps [117].

random telegraph noise (RTN), hot carrier injection (HCI), time dependent dielectric breakdown (TDDB), electromigration (EM), etc. BTI, HCI, and TDDB would affect transistors, while EM is mainly a concern on interconnects. Therefore, in this section we discuss the design for reliability (DFR) methodologies in two sub-categories: DFR on transistor level and DFR on interconnect level. In addition, we will discuss the soft error issue.

3.1 DFR on transistors

Negative-bias temperature instability (NBTI) is one of the dominant aging phenomena in nanometer VLSI regime. NBTI occurs in PMOS devices, and the effect of NBTI is manifested by the increase in threshold voltage ($V_{\rm th}$), thereby increasing the rise delay in the digital gates. Under negative gate-to-source bias, interface traps are generated due to the crystal mismatch in the channel-gate interface. This phase is called the stress phase. However, the removal of negative gate-to-source bias helps in annealing some interface traps, thereby leading a partial recovery. This phase is called recovery phase. It is important to note that the recovery is never complete [116]. The amount of NBTI-induced degradation for a PMOS device depends on the duration of the stress phase. So NBTI is strongly dictated by the signal probabilities at the PMOS gate inputs, and the stacking effect. For instance, in a NOR gate (as shown in Figure 13(a)) the PMOS device with input 'A' is in the stress phase when the signal at input 'A' is '0', whereas for the other PMOS to be under stress phase, the signals at both the inputs 'A' and 'B' need to be '0'.

Several models have been proposed to characterize NBTI-induced delay degradation. The s-factor model in [116] is used along with HSpice simulations to develop a piecewise-linear model of delay with signal probabilities [118]. Similar models for NAND/NOR/inverters have been deployed in [119] to

optimize clock skew in NBTI-impacted gated clock tree. In [120], NBTI models have been developed for multiple operating conditions by considering the scenario percentage and the signal probabilities in the individual operating condition. NBTI-mitigation is typically performed either during technology mapping or after the technology mapping. For instance, standard cell mapping is done in [121] to reduce NBTI effects considering the signal probability values. Gate sizing [118, 122, 123] or logic restructuring with pin-reordering have been performed to combat NBTI-effects [124]. The degradation in rise slew due to NBTI is considered in [118] to build the framework of NBTI-aware timing analysis engine. Even before technology mapping, NBTI-friendly subject graph restructuring is performed in [125].

Besides the impact of NBTI on PMOS, the effect of positive bias temperature instability (PBTI) is not negligible for NMOS with high-k dielectric, and along with HCI, it can cause a shift in $V_{\rm th}$ [126]. The drift in $V_{\rm th}$ due to HCI is proportional to the square root of time, switching activity and frequency. Although the manifestation of both BTI and HCI is perceived in terms of change in $V_{\rm th}$, thereby increasing delay, the key difference is that BTI is dictated by the duty cycle of the stress period whereas HCI is decided by the switching activity. However, several studies have been performed by jointly considering both NBTI and HCI. For instance, Ref. [127] proposes a flow to improve the lifetime in presence of NBTI and HCI. A novel microarchitectural aging analysis framework to analyze NBTI and HCI is presented in [128] to predict performance, power at the early design phase.

With continued CMOS scaling, the supply voltage scales down at a slower pace in comparison to MOS dimensions, such as oxide thickness. Consequently, the electric field across the channel is progressively increasing, thereby rendering the oxide layer conducting, and current flows through the gate-oxide. This phenomenon is called oxide breakdown (OBD). It may be of 2 types, namely soft breakdown and hard breakdown. Soft breakdown is attributed to the parametric variations due to the leakage current flow through the oxide layer, whereas hard breakdown causes functional failure due to the low resistance path through the gate oxide. OBD occurs in the NMOS devices when it has positive gate-to-source bias. The probability of OBD for an NMOS device i at time t is given by the Weibull distribution [129]:

$$P^i_{\rm BD}(t) = 1 - \exp\left(- \left(\frac{\gamma^i_{\rm obd} t}{\alpha} \right)^{\beta} a_i \right), \tag{2}$$

where α is a constant and β is the Weibull shape factor. $\gamma^i_{\rm obd}$ is the OBD factor corresponding to $[1, 0, 0]$ configuration of $[gate, drain, source]$ and a_i is the effective area (scaled w.r.t. the min-sized inverter) of the device. Eq. (2) signifies that this probability increases with area, which renders oversizing to have adverse effect on OBD. It is important to note that the input stress conditions for NBTI in PMOS devices and OBD in NMOS devices are conflicting, and in addition upsizing has opposite impact as well on NBTI and OBD. In [118], a gate sizing framework is proposed to tackle these two conflicting reliability issues at the same time.

Random telegraph noise (RTN) is caused due to random capture/release of electrons by traps located in MOS oxide layer. At any instant, an oxide trap can be in one of the two possible states, filled (electron captured from inversion layer) or empty (electron released to inversion layer). The randomness of the state-transition makes this process a stochastic one, and stochastic activity of a single trap is described as a two-state time-inhomogeneous Markov chain [130]. This phenomenon is correlated to NBTI, and also increases the threshold voltage in the CMOS devices. In [131], RTN is analysed in 45 nm CMOS, and a comparison between PMOS and NMOS devices shows that PMOS device exhibits higher average number of traps and a larger variation in threshold voltage, thereby leading to larger overall impact of RTN.

In the device domain, recent studies have demonstrated that BTI and RTN, along with the random trap fluctuation (RTF), are consistently correlated with the physical trapping/detrapping effects of gate oxide traps as shown in Figure 13(b) [117]. In the nanometer scale, NBTI effects have shifted from deterministic degradations to stochastic ones due to limited number of gate oxide traps within each device [132–135]. Therefore, the stochastic nature of NBTI degradations impose new challenges on both dynamic variations (NBTI-induced) and reliability analysis in the device level. For dynamic variations, stochastic NBTI has introduced cycle-to-cycle variations (CCVs) during operation cycles of each device

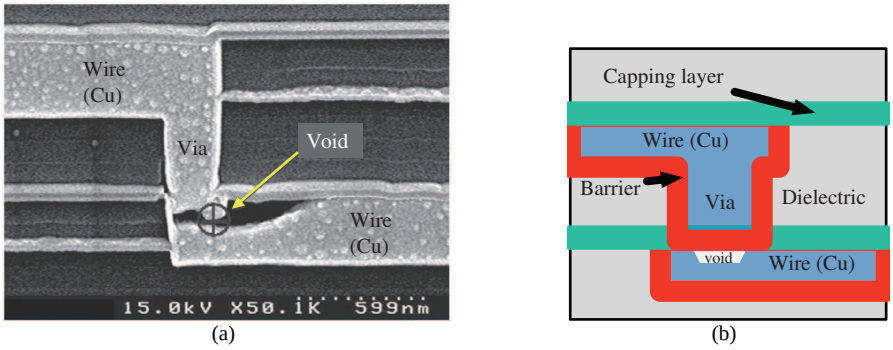

Figure 14 (Color online) (a) SEM image of via with void due to EM [143]; (b) schematic view.

because of the random trapping/detrapping of few gate oxide traps within that particular device [136,137]. For reliability analysis, the end-of-life estimation has been studied with probabilistic analysis of NBTI degradations of each device [138]. Different from the cases under DC conditions, RTN effects under AC conditions have demonstrated special features on temporal variations for each device [139, 140]. The impacts of RTN on digital circuits have been explicitly studied in [141]. Furthermore, aging effects have recently been demonstrated to be layout-dependent for the first time [142].

3.2 DFR on interconnect

On-chip interconnect layers consist of metal wire layers and via layers. The major source of reliability issues on interconnect is electromigration (EM), which is initiated by current flow and may cause open and short circuit failures over time. As IC technology advances, current density increases due to the reduction of feature sizes of both metal wires and vias, which negatively affects failure time. Reduction in the failure time from EM can be worsened even further by high temperatures and mechanical stress around the vias. We can see this phenomenon in Figure 14(a) with an SEM image of the local via and wires [143]. To be more specific, Figure 14(b) shows the schematic view of metal wires, local via structure and an EM-induced void with Cu dual-damascene process.

EM refers to the mass transport and diffusion of metal atoms because of momentum transfer between conducting electrons and atoms [144]. Once atoms migrate with electrons, voids can be formed and grow at the point where the flux diverges, while atomic accumulation takes place at the other sides. Void formation and growth increase the resistance of the metal line, and may lead open circuits eventually [144]. Korhonen's flux equation expresses vacancy movement, the summation of the current-density-driven force and the back-stress-driven force. Eq. (3) shows vacancy flux due to EM from Korhonen's model [145]:

$$\vec{J_v} = \frac{DC}{kT} Ze\rho\vec{j} - \frac{DC}{kT} f\Omega\frac{\partial\sigma}{\partial x}, \tag{3}$$

where $\vec{J_v}$ is total vacancy flux, C is vacancy concentration, $\vec{j}$ is current density vector, k is Boltzmann constant, T is temperature, and σ is hydrostatic stress. f and Ω are vacancy volume coefficient and atomic volume, respectively. Diffusivity of vacancies D is expressed as an Arrhenius equation with initial diffusivity D_0, which is an exponential function of temperature T and activation energy E_a as depicted in (4):

$$D = D_0 \cdot \exp\left(\frac{-E_a}{kT}\right). \tag{4}$$

From these equations, we can see that EM is not just a function of current density, but also of mechanical stress and temperature, as well as other characteristics of micro-structure that can affect the local diffusivity or flux divergence. Since solving basic mass transport equations relies on very slow finite element method, it can be only applied onto very small structures such as single TSV, thus look-up table has to be built for multiple TSVs or wire segments [146]. Recently, Refs. [147,148] propose more compact physical-based EM models using the hydrostatic stress diffusion equation.

Through the preceding modeling, EM violations can be detected during design stage, and then be fixed through layout modification. Lienig [149] suggests several EM inhibiting measures, such as wire sizing, short-length, and reservoir effects. Wire sizing has a key effect on EM, as usually a wider wire leads to smaller current density and greater resistance to EM. Short-length is to set interconnect length limit, due to the fact that any wire with length below some threshold length (typically on the order of 5–50 μm) will not fail by EM. Reservoir effect can significantly improve the lifetime of multiple-layer interconnects through increasing overlaps between metal layer and via layer. In addition, more attention should be paid to via or contact layers, as generally the ampacity of a via is less than that of a metal wire with the same width [149]. Redundant via is one of promising solutions on migrating EM degradation. Pak et al. [150] propose EM reliability model on redundant via structures, as well as a set of techniques on EM aware redundant via insertion. Posser et al. [151] address the problem of EM on signal interconnects within a standard cell.

Full chip level EM awareness is a must to provide reliability on interconnect layers. Due to the high current density, power supply network is one of the most vulnerable interconnect structures to EM. Xie et al. [152] propose control logics to apply balanced amount of current in both directions of power rails to mitigate the EM effects, while Li et al. [153] investigate redundancy to power grid for EM reliability. Other studies [154–156] consider EM constraints in global routing optimization stage.

3.3 Soft error related reliability

Soft error is caused when radiation-induced particles, such as alpha particles and protons, strike releasing electron-hole pair. These are absorbed by source and drain in the CMOS device, changing the state of the transistor. With technology scaling, system soft error rate (SER) has grown exponentially. At the logic level, the impact of soft error is manifested by bit flip in flip-flops or transient pulses in the combinational gates.

Several techniques have been used to mitigate the effect of SER, including circuit level design techniques and system level redundancy, but come with a penalty in performance and area/power cost [157]. For instance, one of the most common techniques is modular redundancy where the circuit under protection is replicated N times adding more logic circuitry. When $N = 2$, it is called dual modular redundancy (DMR) which can detect an error. In addition to error detection, triple modular redundancy (TMR), corresponding to $N = 3$, can also correct the error with larger cost. In [158], structural DMR is proposed which can detect soft error and correct the error significantly with lesser logic complexity in comparison to traditional TMR. Another low cost approach is presented to detect error for arithmetic data paths by performing light-weight shadow computation in modulo-3 space [159].

Since all circuit nodes are not equally susceptible to SER, SER estimation techniques are very important to balance the circuit reliability, performance and cost. In [160], a holistic approach is presented to compute SER by combining circuit level technique with architecture level analysis. Soft-Error-Tolerant design methodology is proposed in [161] to perform this balancing of power, performance and reliability.

Multi-objective genetic algorithm, based on gate sizing, is developed in [162] to optimize SER of standard cell circuits with marginal delay overhead. Recently in [163], soft error in non-core components such as memory and I/O subsystems is studied. A mixed mode simulation platform has been proposed to estimate how soft error in non-core components can affect the system level reliability. The authors also presented a recovery technique which can significantly improve the SER-induced reliability in DRAM and L2 cache controllers with very small overhead in area/power.

The effect of process variation and supply voltage on SER are studied for FinFET SRAMs [164] and logic circuits [165]. The analysis has shown that proton-induced soft errors are becoming more and more important and comparable to that induced by alpha particles for low power applications.

4 Conclusion and future directions

In this paper, we have surveyed various key aspects of design for manufacturability and reliability in nanometer VLSI, including challenges, issues and recent research results. For DFM, since EUV and other next-generation lithography technologies have not yet reached maturity for volume production, the semiconductor industry has been forced to extend the 193 nm lithography with double patterning for 22 nm/14 nm and triple or even quadruple patterning for 10 nm and 7 nm nodes. Thus many physical design/verification and mask synthesis EDA tools need to be rehauled, from standard cell design, to placement/routing, and to mask decomposition. For example, industrial EDA tools have shifted from simple layout geometry (width and spacing) oriented design rule check (DRC) to the DRC+. The key idea of DRC+ is to forbid certain layout configurations, i.e., lithography hotspots, for on-the-fly design or post-layout checking and fixing. The lithography hotspot detection is now supported by major EDA tools, e.g., Cadence Virtuoso DFM [166], Synopsys IC validator [167], Mentor Calibre Pattern Matching [168], and GlobalFoundries DRC+ flow [169]. Due to the adoption of multiple patterning in 20 nm node and below, layout decomposition and compliance have to be performed, at standard cell library design, placement and routing. Considering the unavoidable misalignment/overlay among different masks, the parasitics extraction for MPL also has to be done. Various EDA flows and tools are now available to deal with multiple patterning, e.g., from Synopsys [167], Mentor Graphics [170], and Cadence [166]. It shall be noted that as the landscape of MPL is still evolving, industry approaches are often incremental/reactive in nature, e.g., with conservative design rules and guardband, thus the solution quality may still have a lot of room for improvement.

To account for the reliability issues, conventional industry approach is to over-design the circuit, e.g., using extra margin in delay or power budgeting. However, with aggressive technology scaling, such approach is too pessimistic. Using more accurate reliability analysis tools, e.g., from MOS reliability analysis (MOSRA) in Synopsys HSpice, Eldo from Mentor Graphics or RelXpert from Cadence [171], one can predict the impact of NBTI/HCI on circuit performance either with the built-in or user-specified aging models [172]. The degradation due to device aging can be translated into model parameters (such as threshold voltage, etc.) or device characteristics (e.g., degradation in drain current), which can then be used by circuit designers or synthesis engines for optimizations. In terms of wiring reliability such as EM, certain design rules can be applied as in RedHawk from Apache design [173]), e.g., using the average or peak current density limits set by the foundries to ensure the lifetime EM safety.

While DFM and DFR have been very active research topics in recent years and industries have been incorporating some results into their EDA and design flows, many open research problems still exist to deal with emerging manufacturability and reliability issues. The following are some future research directions:

• In extreme-scaling VLSI, we expect to see more and more adoption of hybrid lithography, e.g., multiple patterning with EUV, DSA, EBL, and so on. The solution space will be huge, e.g., what hybrid lithography candidate to use, at what layer, and how to cope with design and manufacturing technology co-optimization, at what cost.

• The layout style is becoming more and more unidirectional due to the printability issue and adoption of self-aligned multiple patterning. However, such design style may conflict with other yield enhancement techniques, e.g., redundant vias insertion. New ways of wiring/via redundancy may be needed for critical nets.

• To enable cross-layer design for reliability, new compact modeling, e.g., on layout-dependent NBTI, and corresponding circuit/layout optimizations shall be developed, along with cost-effective error-detection and correction mechanism at higher level.

• Promising next-generation device structures, e.g., gate-all-around (GAA) vertical nanowire transistor, will lead to disruptive changes to the standard cell design, placement, and routing.

• It shall be noted that DFM and DFR problems shall not be considered alone, as they do affect each other, e.g., the interconnect printability and EM. Synergistic modeling and optimizations of joint manufacturability and reliability effects will be needed.

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Conflict of interest The authors declare that they have no conflict of interest.

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