SCIENCE CHINA
Information Sciences

• REVIEW •
Special Focus on Advanced Microelectronics Technology

June 2016, Vol. 59 061405:1–061405:14
doi: 10.1007/s11432-016-5559-z

Development of two-dimensional materials for electronic applications

Xuefei LI, Tingting GAO & Yanqing WU*

Wuhan National High Magnetic Field Center and School of Electrical and Electronic Engineering, Huazhong University of Science and Technology, Wuhan 430074*, China*

Received October 31, 2015; accepted December 10, 2015; published online April 22, 2016

Abstract Since the first report of promising electrical properties of Molybdenum disulfide (MoS_2) transistors in 2011, two-dimensional materials with unique properties have attracted great attention, and much research on their applications has been carried out. MoS_2 and black phosphorus are excellent candidates for advanced applications in future electronics because of their tunable bandgap, high carrier mobility, and ultra-thin bodies. In this review, recent research trends in the application of molybdenum disulfide and black phosphorus to electronic devices are examined. We mainly address mobility improvements, dielectrics engineering, radio frequency applications, and low-frequency noise, all of which are crucial for the development of electronic and optoelectronic devices.

Keywords two-dimensional materials, transistors, dielectrics, molybdenum disulfide, black phosphorus

Citation Li X F, Gao T T, Wu Y Q. Development of two-dimensional materials for electronic applications. Sci China Inf Sci, 2016, 59(6): 061405, doi: 10.1007/s11432-016-5559-z

1 Introduction

The device scaling and performance improvements required by the International Technology Roadmap of Semiconductors (ITRS) are facing a severe challenge as conventional Si complementary metal oxide semiconductor (CMOS) scaling approaches its fundamental physical limits. Over the past few years, tremendous efforts have been spent to look into some alternative channel materials "beyond Si" such as germanium, III-V compound semiconductors, and two-dimensional (2D) materials [1–5]. In particular, 2D materials have attracted considerable attention from the transistor community due to their thin bodies, allowing fabrication of shorter transistors due to superior electrostatic control which reduces short-channel effects. Graphene, the first 2D-layered material used for transistors, has been widely explored over the past decade since it was demonstrated by Novoselov et al. [6, 7] in 2004 due to its unique electronic transport properties such as a high Fermi velocity, outstanding carrier mobility, and a high carrier saturation velocity. Unfortunately, a lack of a bandgap greatly limits the performance of graphene transistors and its potential applications in electronics. A separate class of layered materials with electronics applications are the transition metal dichalcogenides (TMDs), which have a chemical formula MX_2 (M = Mo, W, Nb, Re; X = S, Se or Te) [8–10]. Molybdenum disulfide, MoS_2, one of the

* Corresponding author (email: yqwu@mail.hust.edu.cn)

Table 1 Atomic structures and properties of 2D layered material

	Graphene	Molybdenum disulfide	Black phosphorus
Bandgap (eV)	Zero	1.2–1.8	0.3–2
Mobility ($cm^2V^{-1}s^{-1}$)	$\sim$ 200000	10–200	100–1000
Electron effective mass ($/m_0$)	-	0.56	0.17 (x-direction)
Hole effective mass ($/m_0$)	-	0.64	0.15 (x-direction)
Permittivity	2–15	4.8	12.5 (x-direction)
Type	Ambipolar	N type	Ambipolar

most common TMDs, has been used to create field-effect transistors (FETs) with promising performance due to its tunable bandgap and good electron mobility [11–14]. Inspired by the study of graphene and TMDs, black phosphorus (BP) has recently been studied as a promising new 2D material due to its widely tunable direct bandgap, high carrier mobility of up to 1000 $cm^2/V{\cdot}s$ and remarkable in-plane anisotropic electrical, optical and phonon properties [15–18]. High channel mobility improves the FETs on-current, reducing the transistor switching delay. Although the potential of MoS_2 and BP in logic electronics is currently being extensively explored, achieving high-performance 2D-based field-effect transistors remains a grand challenge.

Table 1 shows the fundamental physical properties of promising 2D materials including graphene, MoS_2, and BP [17, 19, 20]. BP's comparatively high hole mobility and low hole effective mass suggest that it is promising for CMOS applications. In this review, we discuss the advances and developments of the most promising 2D-based electronic devices including MoS_2 and BP. We pay special attention to carrier transport properties, field-effect transistor devices, and high-k dielectrics integration. High-frequency transistor applications and low frequency noise are also discussed.

2 MoS_2 field-effect transistors

2.1 Mobility

MoS_2 is an n-type layered material of Mo atoms sandwiched between two layers of S atoms with a bandgap ranging from 1.2 eV for bulk MoS_2 to 1.8 eV for monolayer MoS_2. Monolayers can be exfoliated from bulk by the standard Scotch tape method [21]. Top-gated single-layer MoS_2 transistors were first demonstrated by Radisavljevic et al. [11] in 2011 with extremely high I_{on}/I_{off} (10^8), excellent subthreshold slope (74 mV/dec), and reasonable mobility at room temperature. These devices have attracted much attention and spurred wide-spread scientific research of MoS_2 transistors [22–28]. Their weakness, low drain current, can be improved by using low work function metals for contacts, such as Sc and Ti, as these metals to improve the electron carrier injection. However, a comprehensive study of other metals (Ni, Au, and Pd) on MoS_2 field-effect transistors shows that all produce n-type transistor behavior [29, 30], indicating a heavy pinning phenomenon at the MoS_2/metal interface, due to sulfur vacancies [31]. Figure 1(a) shows the Fermi-level pinning positions of different contact metals, all of which are aligned near the conduction band of MoS_2. Producing partial Fermi-level pinning, low-work function metals such as scandium are more suitable metals for source/drain contacts in n-type MoS_2 transistor [32].

The most commonly reported MoS_2-based transistor has a back-gate structure with SiO_2 as the gate dielectric layer. However, these devices have low mobility, in the range of 0.5–30 $cm^2/V{\cdot}s$ [29, 33, 34]. Figure 1(b) shows field-effect mobility as a function of channel length for back-gated MoS_2 transistors, all of which are lower than 30 $cm^2/V{\cdot}s$. Figure 1(c) shows the temperature dependence of mobility in a back-gated MoS_2 device. The mobility increases with temperature down to 200 K, due to reducing electron-phonon scattering. Below 200 K, the mobility decreases with the temperature down to 4 K, which is consistent with mobility being limited by charged impurity scattering. Theoretical studies have predicted that the intrinsic mobility at room temperature of monolayer MoS_2 is $\sim$ 400 $cm^2/V{\cdot}s$ at high carrier densities of $\sim 10^{13}/cm^2$ as shown in Figure 1(d), which is approximately 10 times greater than experimentally reported values at 300 K [35]. It is believed that the charge transport in monolayer MoS_2

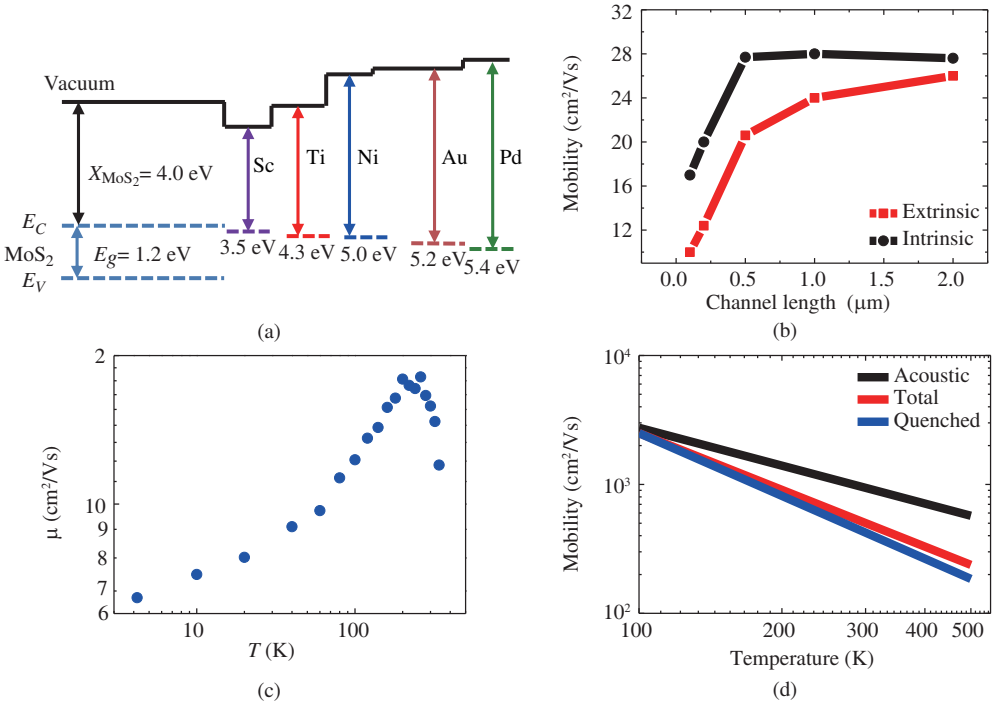

Figure 1 (Color online) (a) Band diagram showing the different workfunction pinning position of the contact metals to MoS_2; (b) channel length dependent field-effect mobility from few-layer MoS_2 transistors; (c) field-effect mobility as a function of temperature of a single-gate monolayer MoS_2 supported on SiO_2; (d) mobility versus temperature from first principles calculation [29, 30, 34, 35].

is mainly limited by extrinsic factors such as Coulomb impurities, charge traps, and defects. Much work has been devoted to investigate their roles in charge transport [36]. Jariwala et al. [37] demonstrated that three single-layer MoS_2 transistors with a mobility of ~ 110 cm^2/V·s at low temperatures exhibit band-like transport with phonon scattering dominant at $T > 100$ K, and charged impurity scattering dominant for $T < 100$ K. Based on this investigation, Baugher et al. [38] further improved the sample quality by vacuum annealing and observed the similar transport behavior in monolayer MoS_2 with mobility approaching 1000 cm^2/V·s at low temperatures.

2.2 Dielectrics

Novoselov and Geim [33] in 2005 demonstrated the first MOSFET based on single-layer MoS_2 with a mobility of ~ 3 cm^2/V·s and a relatively low on/off ratio. After that, the performance of monolayer MoS_2 transistors was greatly improved by capping them with a HfO_2 dielectric film, which reduces charged impurity scattering as well as photon scattering [11]. It has been well known that the impurities and the dielectric environment have an important impact on the electrical and optical properties of 2D materials [39]. Theoretical studies show that high-k dielectrics are able to enhance the performance of MoS_2-based FETs due to the dielectric screening effect [35, 40–43]. Figure 2 shows the effect of various dielectric environments on electron mobility for two representative temperatures, 100 K and 300 K. By using HfO_2/ZrO_2 as the dielectric instead of SiO_2/air, the room temperature mobility improves from ~ 45 to 80 cm^2/V·s. Meanwhile, a 37% enhancement in mobility can be achieved by reducing the oxide thickness from 20 to 2 nm at $n = 10^{12}$ cm^{-2} due to more effective screening of the charged impurities. In addition to the intrinsic scattering from phonons in the TMD channel, extrinsic scattering from charged impurities at the channel/substrate interface, and charge traps in the substrate, and surface optical phonon scattering originating from substrate can also play an important role in the carrier mobility of the MoS_2 device. Although a high-k dielectric may screen Coulomb scattering from charged impurities, surface polar optical scattering from SiO_2 (~ 60 meV) severely degrade electron mobility as predicted by theoretical simulations [40]. Indeed, the simulation results by a Monte Carlo method based on the analysis

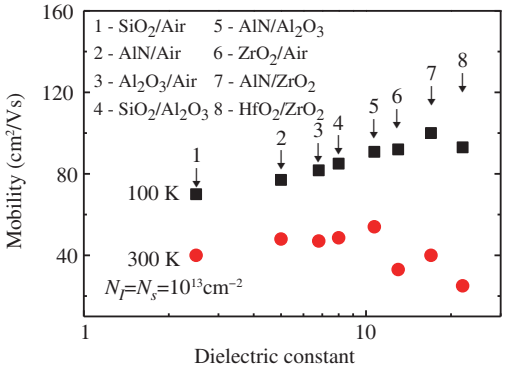

Figure 2 (Color online) Electron mobility as a function of an environment dielectric constant [40].

of remote phonon effect and charged impurity screening are in good agreement with the experimental data from low temperature Hall measurement. The further mobility improvement is achieved by using a PMMA substrate, up to 480 $cm^2/V{\cdot}s$ at room temperature for multilayer MoS_2 transistors [44]. This is mainly attributed to the reduced short range disorder and long-range disorder at the MoS_2/PMMA interface than at the MoS_2/SiO_2 interface. Recently, atomically flat hexagonal boron nitride (h-BN) has begun to attract interest as an excellent substrate with greatly reduced scattering centers for graphene duo to its atomically flat and a clean charge environment, which leads to remarkably high carrier mobility [45]. Similar to graphene, using h-BN layer in the MoS_2 transistors also reduces scattering from charged impurities and roughness and improves the mobility dramatically [46]. The Hall mobility for the 1–6 layer MoS_2 samples encapsulated within h-BN as a function of temperature, showing a record high Hall mobility reaching 34000 $cm^2/V{\cdot}s$ for 6-layer MoS_2 at low temperature. Meanwhile, Shubnikov-de Haas oscillations are also observed in MoS_2.

2.3 Channel scaling

The ultimate performance limit of MoS_2 transistors is performed by using self-consistent quantum transport simulations, showing very promising performance [47–51]. Liu et al. [29] first experimentally demonstrate the channel scaling of MoS_2 transistors with channel lengths down to 50 nm. Although high I_{on}/I_{off} ratio is achieved, drain current is less than 50 $\mu A/\mu m$, which is mainly limited by contact resistance. To realize high-performance MoS_2 short channel transistors, an important breakthrough on contact is achieved by doping Cl using 1,2 dichloroethane [52]. Figure 3(a) shows the output characteristics of the 100 nm MoS_2 transistors with and without the Cl doping at room temperature. A nearly 4.4 times decrease in on-resistance is observed. Figure 3 (b) and (c) shows well-behaved output and transfer characteristics of a MoS_2 device with a channel length of 100 nm. Excellent current saturation can be observed with a maximum drain current of 550 $\mu A/\mu m$ at room temperature. The output characteristics of a 100 nm MoS_2 device with gate voltages from 20 to 40 V at 20 K are shown in Figure 3(d). Interestingly, the drain current reaches a maximum value at a moderate V_d and then decreases when V_d increases further, exhibiting significant negative differential resistance behavior (NDR) [53]. The magnitude of NDR is very small at $V_g = 20$ V, but starts to increase as the gate voltage V_g increases. Self-heating is responsible for the NDR effect, which is demonstrated by pulsed IV measurements. The local heating of MoS_2-SiO_2 interfaces leads to poor device performance and decreased lifetimes, which could be an important issue for high-performance scaled MoS_2 transistors.

2.4 Radio frequency transistors

One of the main figures of merit to estimate the performance of radio frequency devices is the cutoff frequency f_T given by the following formula [5]:

$$f_T = \frac{g_m}{2\pi} \times \frac{1}{(C_{gs} + C_{gd})[1 + g_{ds}(R_s + R_d)] + C_{gd} g_m (R_s + R_d)}, \tag{1}$$

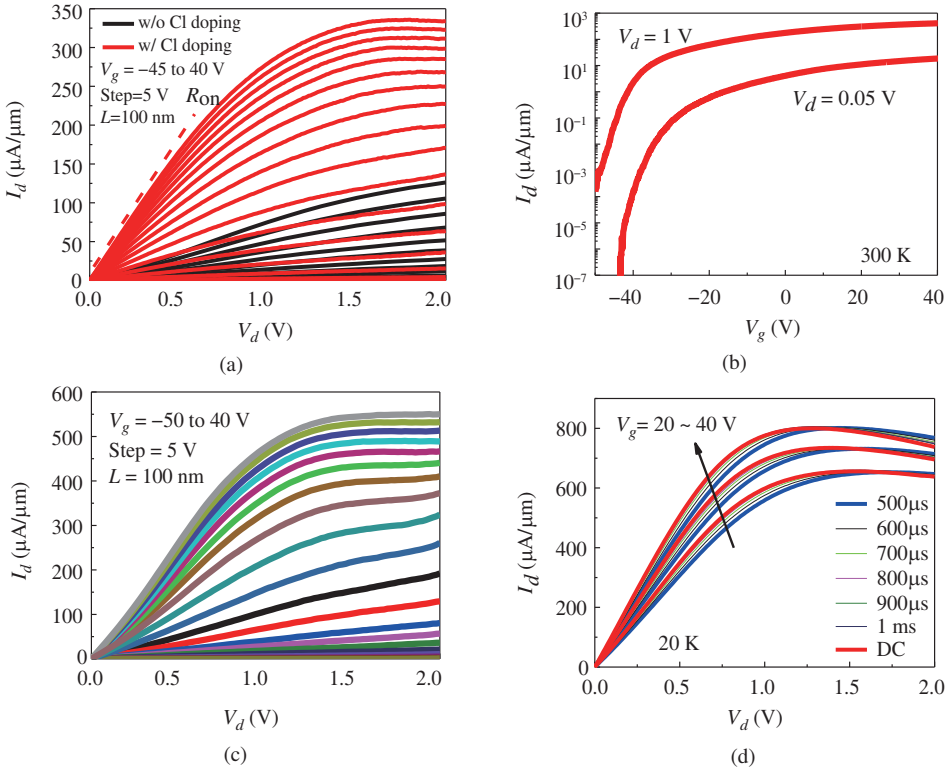

Figure 3 (Color online) (a) Output characteristics of the 100 nm MoS_2 FETs with and without the Cl doping at room temperature; (b) transfer (with V_d ranging from 0 to 2 V) characteristics of a 100 nm MoS_2 device at room temperature; (c) output (with V_g ranging from −45 to 40 V) characteristics of a 100 nm MoS_2 device at room temperature; (d) output characteristics of the same device at 20 K with 10 V steps in V_g from 20 to 40 V with comparison between dc measurement and different pulse widths (PW = 500 μs, 600 μs, 700 μs, 800 μs, 900 μs, and 1 ms) [53].

where g_m is the intrinsic transconductance, C_{gs} is the gate source capacitance, $C_{\rm gd}$ is the gate-drain capacitance, $g_{\rm ds}$ is the drain conductance, and R_s and R_d are the source and drain series resistances, respectively. As suggested by the relation $f_T = g_m/2\pi C_{\rm ox}$, to obtain a high cut-off frequency in a transistor, it is essential to retain a high carrier mobility while achieving a small channel length. In addition to f_T, $f_{\rm max}$ is also a very important parameter of RF amplifiers. The formula for $f_{\rm max}$ is shown below [54]:

$$f_{\rm max} = \frac{f_T}{2\sqrt{g_{\rm ds}(R_g + R_s) + 2\pi f_T C_g R_g}}, \tag{2}$$

where $g_{\rm ds}$ is the drain differential conductance, R_s is the source resistance, $C_{\rm gd}$ is the gate to drain capacitance, and R_g is the gate resistance. Although cutoff frequencies of 350 GHz for epitaxial graphene have been achieved [55, 56], voltage gain is low and sub-threshold current is high since graphene transistors cannot be fully pinched off due to their zero-bandgap nature. Layered MoS_2 with its tunable bandgap also has potential for analog electronics. MoS_2 RF devices have been under development since 2012 [57]. Radisavljevic et al. [58] reported a comprehensive experimental studies of the high-frequency characteristics of 1–3 layers top-gated MoS_2 transistors on SiO_2/Si in 2014. For a gate length of 240 nm, a peak f_T as high as 6 GHz was obtained for the trilayer device with 30 nm HfO_2 as gate dielectric. Further reducing the gate length and improving the channel mobility is expected to improve the cutoff frequency f_T. The work represented an important step in MoS_2-based electronics for high frequency applications. Recently, it was demonstrated that the self-aligned few-layer MoS_2 device exhibits an intrinsic cut-off frequency f_T up to 42 GHz and a maximum oscillation frequency $f_{\rm max}$ up to 50 GHz, including excellent on-off ratio, current saturation and an intrinsic gain over 30 [59]. The formation of the self-aligned source and drain electrodes can substantially reduce the access resistance and boost the field-effect mobility up to ~ 170 cm^2/V·s with a saturation velocity of 1.8×10^6 cm/s. Meanwhile, an intrinsic cutoff frequency

f_T of 13.5 GHz and maximum oscillation frequency $f_{\max}$ of 10.5 GHz are achieved in a 68 nm MoS_2 FET on flexible polyimide substrate without electrical degradation after 1000 bending cycles, showing the promising potential for highly flexible electronics. Despite significant effort, the small size of exfoliated MoS_2 flakes has limited industrial scale applications. Very recently, transistors suitable for high-frequency measurements have been fabricated on large-area MoS_2 grown by chemical vapor deposition (CVD) with a mobility of 55 $cm^2/V{\cdot}s$ [60]. The CVD MoS_2 device has achieved a f_T of 6.7 GHz and $f_{\max}$ of 5.3 GHz at a gate length of 250 nm. In spite of great progress, the RF performance of MoS_2 transistors described above is still far from ideal. To realize high-performance MoS_2 transistors, three major issues must be solved. First, the fabrication of a low-resistivity metal-MoS_2 junction. Large contact resistance strongly limits device performance, especially in short channel devices. Using graphene between MoS_2 and metal as electrode could be a promising approach, which has been demonstrated by some groups. Second, the improvement of carrier mobility. Extrinsic sources such as charged impurities on or near the substrate surface and remote optical phonons from the substrate materials are dominant scattering centers. The reduction or suppression of carrier scattering remains a big challenge. Third, deposition of a high-quality dielectric on MoS_2 is difficult. Dielectric integrations on MoS_2 are not straightforward due to the lack of dangling bonds at the MoS_2 surface. Some groups have successfully integrated high-k dielectrics onto MoS_2 by lowering atomic layer deposition (ALD) temperatures to less than $\sim 200^\circ$C, or by the insertion of an Al seeding layer before ALD dielectric deposition. To improve the dielectric quality, much more research needs to be performed.

2.5 Low frequency noise

Low frequency noise generated in the electronic devices is an important limiting factor in modern electronics which determines how small signals can be detected and resolved without error in circuits [61]. Maintaining a high signal to noise ratio becomes a big challenge for deeply scaled devices, which have narrow operating voltage requirements, along with severe short channel effects [62]. In signal amplifiers, low frequency noise up-converts to cause phase noise at operating frequencies, limiting applications [63]. In view of the scientific significance and practical applications, a thorough understanding of the low frequency noise mechanisms and assessing the potential of MoS_2 field-effect transistors are of great importance. The first study on low-frequency electronic noise in single-layer MoS_2 field-effect transistors was performed by Sangwan et al. [64]. The current noise spectral density of a single-layer MoS_2 device shows a $1/f$ dependence up to a frequency of 8 kHz. The Hooge parameter ranging between 0.005 and 2.0 in vacuum and the noise amplitude increased up to 10 times in ambient conditions, revealing the significant influence of atmospheric adsorbates on charge transport. Meanwhile, it is demonstrated that annealing is effective to improve the noise level in the bilayer MoS_2 FETs due to the decrease of trap density. Using this process, Kwon et al. [65] have investigated low frequency noise in multilayer MoS_2 FETs, showing $1/f$ noise was dominated by carrier number fluctuation. In addition, Li et al. [53] studied the $1/f$ noise of few-layer MoS_2 FETs with Cl-doping at various temperatures. Figure 4(a) plots the S_{id}/I_d^2 and transconductance to drain current squared $(g_m/I_d)^2$ as functions of drain current I_d of the MoS_2 device from 300 to 20 K and shows that the noise mechanism of few-layer MoS_2 FET is dominated by mobility fluctuation at high drain current levels in strong inversion, while number carrier fluctuation noise takes over at low drain current. Figure 4(b) gives the corresponding Hooge parameter α_H from 300 to 20 K with the minimum α_H of 3.3×10^{-4} at room temperature. This improvement is mainly attributed to the decreased contact resistance and high drain current by Cl-doping. To investigate the effect of contact resistance on noise of MoS_2 FETs, Renteria et al. [66] used a model to fit the measured noise spectral density before and after aging. It was found that the increase in the noise level of the aged MoS_2 transistors is due to the channel rather than the contact degradation, informing future reliability improvements of 2D-based devices. The same group has also reported that the relatively thick MoS_2 channels have advantages of higher electron mobility and lower noise [67]. In general, the noise level of MoS_2 FETs is larger than that of graphene, which could be due to high contact resistance and low carrier mobility in MoS_2 FETs.

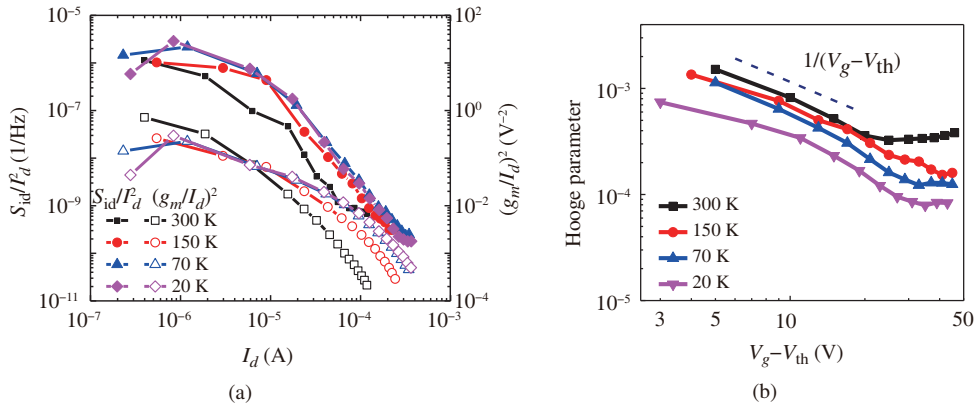

Figure 4 (Color online) (a) Normalized drain current noise spectral density (S_{id}/I_d^2) and transconductance to drain current ratio squared [$(g_m/I_d)^2$] versus drain current for the MoS_2 device from 300 to 20 K; (b) Hooge parameter versus $V_g - V_{th}$ at various temperatures from 300 to 20 K [53].

3 BP field-effect transistors

3.1 Mobility

Preceding the current interest in layered materials for electronic applications, research in the 1960's found that black phosphorus exhibits high carrier mobility with an intrinsic band gap [68,69]. Similar to graphene and MoS_2, thin layers of BP can be obtained using the mechanical exfoliation method. Li et al. [15] fabricated field-effect transistors based on few-layer black phosphorus crystals with thickness as low as 5 nm. The devices exhibit bipolar behavior with on-off ratio up to 10^6, a low off-state current, and electronic mobilities up to ~ 1000 cm^2/V·s. For field-effect mobility and Hall mobility, both decrease at temperatures higher than ~ 100 K, and saturate at lower temperatures. The behaviors of the mobility can be attributed to the electron-phonon scattering that dominates at high temperatures from ~ 100 K up to 300 K and scattering from charged impurities that dominates when $T < 100$ K, respectively. A more comprehensive work is reported by Liu et al. [16]. The ab initio band structure calculations show that the fundamental band gap depends sensitively on the number of layers from 0.3 to 1 eV. High on-current of 194 mA/mm, high hole mobility up to 286 cm^2/V·s and on/off ratio up to 10^4 was achieved with phosphorene transistors at room temperature. Meanwhile, the field-effect mobility shows a strong thickness dependence, which first reaches the maximum at ~ 5 nm and then decreases gradually with further increase of crystal thickness due to screening and interlayer coupling in layered materials. Also, a CMOS inverter with combination BP pMOS transistors and MoS_2 nMOS transistors, is demonstrated for the first time, which shows great potential for semiconducting 2D crystals in future electronic, opto-electronic and flexible electronic devices [70–72]. A unique property of BP is the strong intrinsic in-plane anisotropy due to its unique orthorhombic crystal structure [18,73–81]. Xia et al. [82] study DC conductivity and IR relative extinction measured along six directions on the BP flake. A ratio of the maximum value at the x-direction at the band edge and minimum value at the y-direction at the band edge in the angular dependent conductance measurement is extracted to be around 1.5. The mobility of the 15 nm sample is larger than that of the 8 nm sample and both of samples have the maximum mobility along the x direction. The Hall mobility exceeds 1000 cm^2/V·s at 120 K. This in-plane anisotropy provides a novel functionality to devices based on black phosphorus. Similar to MoS_2, contact resistance is a key factor in the performance of BP transistors. The contact resistance of BP transistors for both Ni and Pd contacts are extracted from the transfer length method structure as shown in Figure 5(a), which shows a strong gate-dependent behavior. The Pd contact resistance is 1.75 Ω·mm at $V_{bg} = -40$ V, which is lower than the Ni contact resistance of 3.15 Ω·mm at the same back gate voltage [83]. With introduction of 7-nm-thick HfO_2 as the back-gate dielectric, the contact resistance values is as low as 1.14 Ω·mm as shown in Figure 5(b) [84]. Interestingly, the transport type is closely related to the channel length and

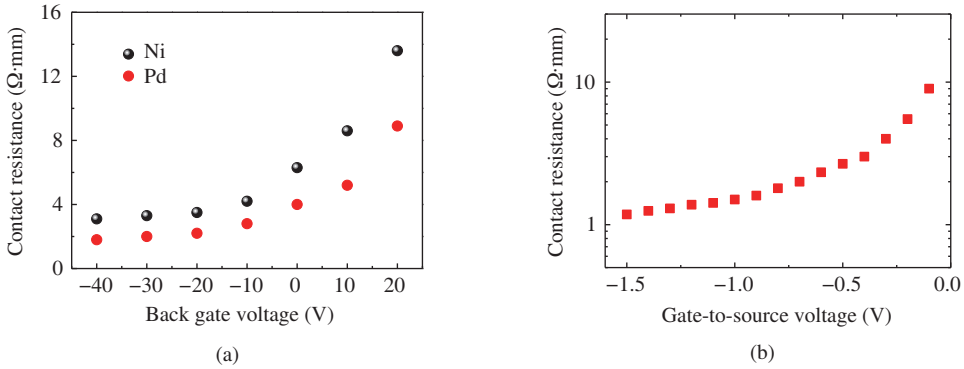

Figure 5 (Color online) (a) Contact resistance as a function of gate voltages for BP transistors with Ni and Pd; (b) contact resistance as a function of gate voltages for BP transistors with HfO_2 gate dielectric thickness of 7 nm and Ti/Au [83, 84].

metal. It presented clear ambipolar characteristics for both Ni- and Pd contacted BP FETs at shorter channel lengths [83]. This is mainly due to the narrow bandgap of BP, which allows the Fermi level to easily move to either near the valence band or the conduction band. Very recently, research interest is also moving towards BP nFETs [85–87]. Theoretical calculations by Padilha [88] also predicted that it is possible to realize ohmic contacts using graphene. It has also been demonstrated that TiO_2 interlayer could reduce the Schottky barrier [89].

3.2 Surface passivation

Despite great progress having been made in the area of BP, the lack of air-stability poses much concern for its application [90]. An effective approach to prevent BP degradation is dielectric encapsulation [91–94]. A comparison of the selected AFM line profiles at the beginning and the end of the monitoring period between two Al_2O_3 capped BP samples shows that the BP device with thick capping was stable. Thick-cap devices (25 nm ALD Al_2O_3) showed less degradation, consistent with the AFM data [95]. Figure 6(a) compares the on/off ratio of BP devices with and without AlO_x overlayer, showing that AlO_x encapsulated BP devices effectively suppress ambient degradation and maintain high on/off ratios of $\sim 10^3$ for over two weeks in ambient conditions [91]. Results also show that the photo induced degradation is activated by air or alternatively by a mixture of pure oxygen and water vapor [96]. A capping layer made of 300 nm of parylene C is effective in preventing photo induced degradation. This results indicate that the instability of BP is associated with photo, oxygen, and water vapor. Theoretical calculations also show that oxygen chemisorption onto phosphorene is exoenergetic and causes the formation of neutral defects [97]. Based on these reports, ALD of dielectrics is an effective and scalable method to passivate BP flakes and to protect them from environmental deterioration. However, deposition of a uniform high-k dielectric layer onto BP is not easy. Figure 6(b) shows the Al_2O_3 thickness as a function of ALD cycles for three different surface conditions [98]. S1 sample has native oxide. The exposure time to ambient air of S2 and S3 samples are less than 5 min and 1 min, respectively. After 40 cycles, the Al_2O_3 thickness on the S1, S2, and S3 samples are $\sim$ 2.47, 0.74, and 0.88 nm, respectively. Figure 6(c) plots the ratio of $I_{\text{P-O}}/I_{\text{P-P}}$ as a function of Al_2O_3 thickness. As expected, the S3 sample has the lowest phosphorus oxide concentration. This results suggest that surface functionalization is important for depositing a uniform film on BP and its effect on electrical property needs to be investigated further. BN is another promising capping layer. It can protect BP from environmental degradation and also the ultra-clean BN-BP interface allows for a high mobility over 1000 $cm^2/V{\cdot}s$ at room temperature [99–105]. Besides exfoliation, liquid-phase exfoliation and pulsed laser deposition have also been used to fabricate black phosphorus thin films [106–108]. However, their electrical properties are still poor. Very recently, Li et al. [109] demonstrated a method to fabricate thin-film black phosphorus on a flexible substrate with a field-effect mobility of ~ 0.5 $cm^2/V{\cdot}s$. This suggests the potential for synthesis of large-scale, high quality thin-film BP electronics, similar to MoS_2 and graphene.

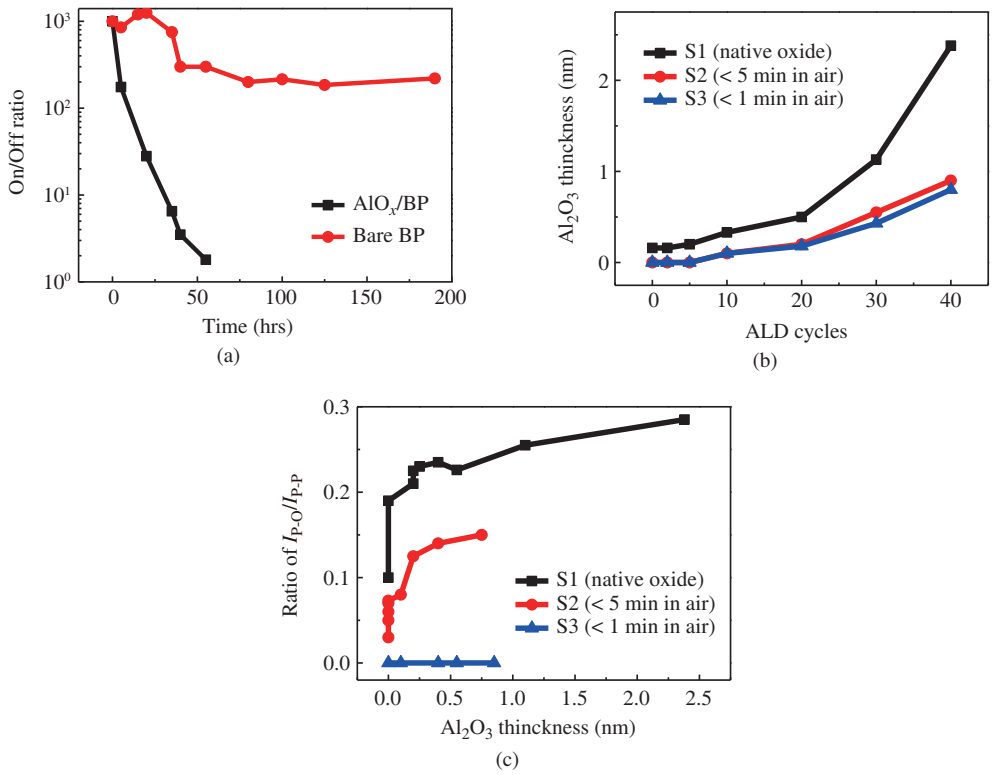

Figure 6 (Color online) (a) On/off ratio as a function of exposure time for BP transistors with and without AlO_x; (b) Al_2O_3 thickness as a function of ALD cycles for three different surface conditions; (c) ratio of $I_{P\text{-}O}/I_{P\text{-}P}$ as a function of Al_2O_3 thickness at the corresponding surface conditions [98].

3.3 Radio frequency transistors

There has also been substantial interest in using BP flakes for ultra-high speed transistors due to their high mobility and the existence of a bandgap. Wang et al. [110] recently demonstrated high-frequency operation of BP FETs based on the dual-gate geometry. 21 nm of HfO_2 deposited by ALD at 150°C was used as the gate dielectric. The thickness of the BP flake was chosen to be 8.5 nm in order to balance the mobility and on/off ratio. The transfer characteristics of BP FETs show a current density up to 270 mA/mm and DC transconductance above 180 mS/mm for hole conduction. A cutoff frequency f_T of 12 GHz and a maximum oscillation frequency $f_{\max}$ of 20 GHz for the 300 nm channel length BP transistor are obtained. While its use is in its infancy, BP offers new opportunities by virtue of high carrier mobility, excellent scaling properties, and a tunable bandgap. With these advantages and its good current saturation properties, BP has the potential to offer performance benefits in RF systems in terms of voltage and power gain.

3.4 Low frequency noise

Low-frequency noise mainly originates from the fluctuations in the number of charge carriers in the channel due to trapping/detrapping of carriers in the oxide layer and/or fluctuations in the mobility of carriers, and is a valuable indicator of dielectric quality, contact quality, and reliability evaluation [62,111]. It is important to determine the source and magnitude of the $1/f$ noise in BP transistors in order to understand the transport characteristics and physics-based properties as well as assess their potential in optoelectronics and electronics. Low-frequency noise measurements and analysis on few-layer BP transistors were reported by Na et al. [112] in 2014. With changing V_g from 0 to −40 V, the drain current spectral density increases four times. The dominant noise source was found to be carrier number fluctuation with correlated mobility fluctuation. Interface trap density values for the thermally annealed

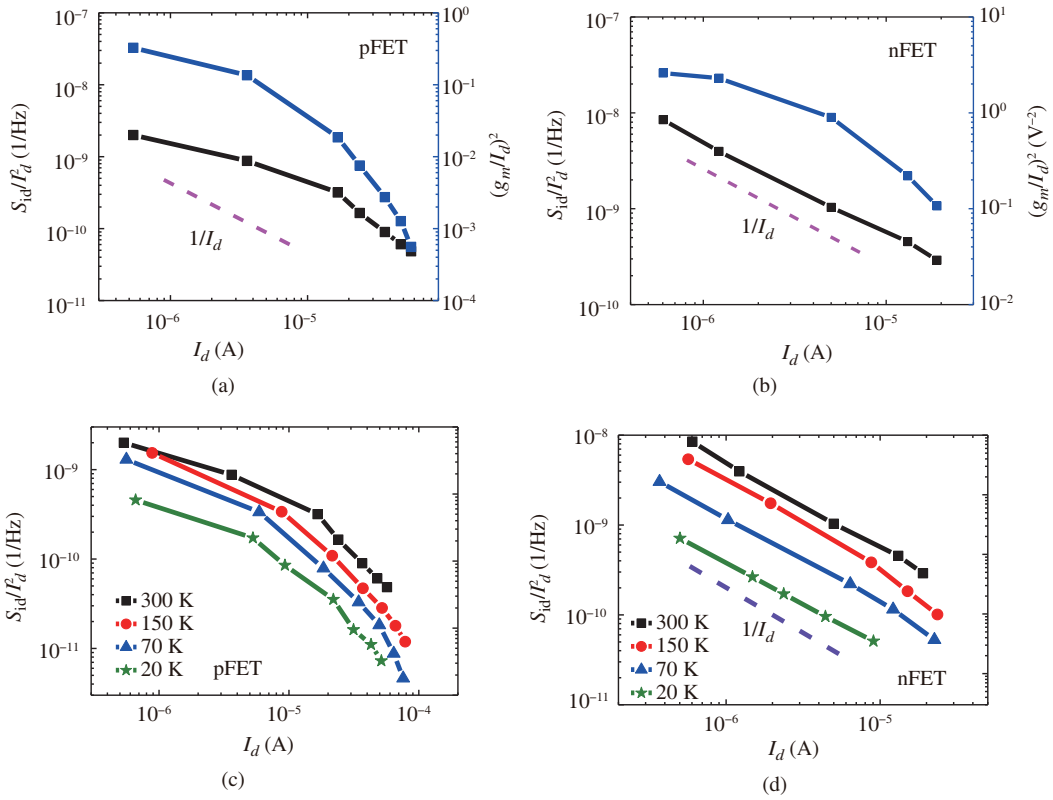

Figure 7 (Color online) Normalized drain current noise spectral density (S_{id}/I_d^2) and transconductance to drain current ratio squared [$(g_m/I_d)^2$] at $V_d = 0.2$ V and $f = 100$ Hz versus drain current at 300 K for the BP (a) pFET, (b) nFET. Normalized drain current noise spectral density (S_{id}/I_d^2) at $V_d = 0.2$ V and $f = 100$ Hz as a function of drain current from 300 to 20 K for the BP (c) pFET, (d) nFET [113].

and Al_2O_3-passivated few-layer BP transistors are $\sim 1.2\times10^{12}$ and $\sim 1.5\times10^{11}$ $cm^{-2}eV^{-1}$, respectively. Very recently, Li et al. [113] investigated the temperature dependent ambipolar operation of both electron and hole transport for BP transistors from 300 to 20 K. Figure 7 (a) and (b) show the S_{id}/I_d^2 and the corresponding $(g_m/I_d)^2$ of the BP pFET and nFET at $f = 100$ Hz as functions of drain current at 300 K. It is found that the dominated noise mechanism of multi-layer BP nFET and pFET are mobility fluctuation and carrier number fluctuations with correlated mobility fluctuations, respectively. Meanwhile, the mechanism has no dependence on temperature as shown in Figure 7 (c) and (d). These results provide fundamental insights into the electron and hole transport and related $1/f$ mechanisms at various temperatures.

4 Conclusion

In this paper, we have studied the fundamental device properties of MoS_2 and BP transistors. For MoS_2, we report on the mobility, dielectric formation, channel scaling properties, radio frequency performance, and low frequency noise in MoS_2 transistors. MoS_2 transistors show superior immunity to short channel effects. The large contact resistance is the major challenge currently in MoS_2 transistor development. Integration with high quality high-k dielectrics is highly desirable in order to boost mobility. BP shows great potential for nanoelectronic applications, especially in CMOS circuits, because of its layer-controlled bandgap, high carrier mobility, and ambipolar transport. To improve the performance of BP transistors, doping to reduce contact resistances and integration with high quality dielectrics are important. Meanwhile, the highly anisotropic structural, electronic, and transport properties of BP have been largely unexplored, and this points to new opportunities for future research and development activities.

For practical electronics applications, development of process to grow large scale, high quality BP thin films is needed. 2D-based transistors are currently a highly-researched area, and we expect to see great improvements in their design, and consequently their usage in practical circuits in the near future.

Acknowledgements This project was supported by National Natural Science Foundation of China (Grant Nos. 11404118, 61390504).

Conflict of interest The authors declare that they have no conflict of interest.

References

1 Xuan Y, Wu Y Q, Ye P D. High-performance inversion-type enhancement-mode InGaAs MOSFET with maximum drain current exceeding 1 A/mm. IEEE Electron Dev Lett, 2008, 29: 294–296
2 Del Alamo J A. Nanometre-scale electronics with III-V compound semiconductors. Nature, 2011, 479: 317–323
3 Zhang R, Huang P C, Lin J C, et al. High-mobility Ge p- and n-MOSFETs with 0.7-nm EOT using $HfO_2/Al_2O_3/GeO_x$/Ge gate stacks fabricated by plasma postoxidation. IEEE Trans Electron Dev, 2013, 60: 927–934
4 Wu H, Si M W, Dong L, et al. Germanium nMOSFETs with recessed channel and S/D: contact, scalability, interface, and drain current exceeding 1 A/mm. IEEE Trans Electron Dev, 2015, 62: 1419–1426
5 Schwierz F. Graphene transistors. Nat Nanotechnol, 2010, 5: 487–496
6 Novoselov K S, Geim A K, Morozov S V, et al. Electric field effect in atomically thin carbon films. Science, 2004, 306: 666–669
7 Geim A K, Novoselov K S. The rise of graphene. Nat Mater, 2007, 6: 183–191
8 Koski K J, Cui Y. The new skinny in two-dimensional nanomaterials. ACS Nano, 2013, 7: 3739–3743
9 Miro P, Audiffred M, Heine T. An atlas of two-dimensional materials. Chem Soc Rev, 2014, 43: 6537–6554
10 Chhowalla M, Shin H S, Eda G, et al. The chemistry of two-dimensional layered transition metal dichalcogenide nanosheets. Nat Chem, 2013, 5: 263–275
11 Radisavljevic B, Radenovic A, Brivio J, et al. Single-layer MoS_2 transistors. Nat Nanotechnol, 2011, 6: 147–150
12 Wang Q H, Kalantar-Zadeh K, Kis A, et al. Electronics and optoelectronics of two-dimensional transition metal dichalcogenides. Nat Nanotechnol, 2012, 7: 699–712
13 Butler S Z, Hollen S M, Cao L, et al. Progress, challenges, and opportunities in two-dimensional materials beyond graphene. ACS Nano, 2013, 7: 2898–2926
14 Ganatra R, Zhang Q. Few-Layer MoS_2: a promising layered semiconductor. ACS Nano, 2014, 8: 4074–4099
15 Li L K, Yu Y J, Ye G J, et al. Black phosphorus field-effect transistors. Nat Nanotechnol, 2014, 9: 372–377
16 Liu H, Neal A T, Zhu Z, et al. Phosphorene: an unexplored 2D semiconductor with a high hole mobility. ACS Nano, 2014, 8: 4033–4041
17 Du H W, Lin X, Xu Z M, et al. Recent developments in black phosphorus transistors. J Mater Chem C, 2015, 3: 8760–8775
18 Tran V, Soklaski R, Liang Y, et al. Layer-controlled band gap and anisotropic excitons in few-layer black phosphorus. Phys Rev B, 2014, 89: 235319
19 Ling X, Wang H, Huang S X, et al. The renaissance of black phosphorus. Proc Natl Acad Sci, 2015, 112: 4523–4530
20 Santos E J G, Kaxiras E. Electric-field dependence of the effective dielectric constant in graphene. Nano Lett, 2013, 13: 898–902
21 Mak K F, Lee C, Hone J, et al. Atomically thin MoS_2: a new direct-gap semiconductor. Phys Rev Lett, 2010, 105: 136805
22 Fiori G, Bonaccorso F, Iannaccone G, et al. Electronics based on two-dimensional materials. Nat Nanotechnol, 2014, 9: 768–779
23 Jariwala D, Sangwan V K, Lauhon L J, et al. Emerging device applications for semiconducting two-dimensional transition metal dichalcogenides. ACS Nano, 2014, 8: 1102–1120
24 Schwierz F, Pezoldt J, Granzner R. Two-dimensional materials and their prospects in transistor electronics. Nanoscale, 2015, 7: 8261–8283
25 Yazyev O V, Kis A. MoS_2 and semiconductors in the flatland. Mater Today, 2015, 18: 20–30
26 Lopez-Sanchez O, Lembke D, Kayci M, et al. Ultrasensitive photodetectors based on monolayer MoS_2. Nat Nanotechnol, 2013, 8: 497–501
27 Radisavljevic B, Whitwick M B, Kis A. Integrated circuits and logic operations based on single-layer MoS_2. ACS Nano, 2011, 5: 9934–9938
28 Late D J, Huang Y-K, Liu B, et al. Sensing behavior of atomically thin-layered MoS_2 transistors. ACS Nano, 2013, 7: 4879–4891
29 Liu H, Neal A T, Ye P D. Channel length scaling of MoS_2 MOSFETs. ACS Nano, 2012, 6: 8563–8569
30 Du Y C, Yang L M, Liu H, et al. Contact research strategy for emerging molybdenum disulfide and other two-dimensional field-effect transistors. APL Mater, 2014, 2: 092510
31 Liu D, Guo Y, Fang L, et al. Sulfur vacancies in monolayer MoS_2 and its electrical contacts. Appl Phys Lett, 2013, 103: 183113

32 Das S, Chen H-Y, Penumatcha A V, et al. High performance multilayer MoS_2 transistors with scandium contacts. Nano Lett, 2012, 13: 100–105
33 Novoselov K S, Jiang D, Schedin F, et al. Two-dimensional atomic crystals. Proc Nat Acad Sci, 2005, 102: 10451–10453
34 Radisavljevic B, Kis A. Mobility engineering and a metal–insulator transition in monolayer MoS_2. Nat Mater, 2013, 12: 815–820
35 Kaasbjerg K, Thygesen K S, Jacobsen K W. Phonon-limited mobility in n-type single-layer MoS_2 from first principles. Physl Rev B, 2012, 85: 115317
36 Kaasbjerg K, Thygesen K S, Jauho A-P. Acoustic phonon limited mobility in two-dimensional semiconductors: deformation potential and piezoelectric scattering in monolayer MoS_2 from first principles. Phys Rev B, 2013, 87: 235312
37 Jariwala D, Sangwan V K, Late D J, et al. Band-like transport in high mobility unencapsulated single-layer MoS_2 transistors. Appl Phys Lett, 2013, 102: 173107
38 Baugher B W H, Churchill H O H, Yang Y F, et al. Intrinsic electronic transport properties of high-quality monolayer and bilayer MoS_2. Nano Lett, 2013, 13: 4212–4216
39 Jena D, Konar A. Enhancement of carrier mobility in semiconductor nanostructures by dielectric engineering. Phys Rev Lett, 2007, 98: 136805
40 Ma N, Jena D. Charge scattering and mobility in atomically thin semiconductors. Phys Rev X, 2014, 4: 011043
41 Zeng L, Xin Z, Chen S W, et al. Remote phonon and impurity screening effect of substrate and gate dielectric on electron dynamics in single layer MoS_2. Appl Phys Lett, 2013, 103: 113505
42 Singh A K, Hennig R G, Davydov A V, et al. Al_2O_3 as a suitable substrate and a dielectric layer for n-layer MoS_2. Appl Phys Lett, 2015, 107: 053106
43 Ong Z-Y, Fischetti M V. Mobility enhancement and temperature dependence in top-gated single-layer MoS_2. Physl Rev B, 2013, 88: 165316
44 Bao W Z, Cai X H, Kim D, et al. High mobility ambipolar MoS_2 field-effect transistors: substrate and dielectric effects. Appl Phys Lett, 2013, 102: 042104
45 Dean C, Young A, Meric I, et al. Boron nitride substrates for high-quality graphene electronics. Nat Nanotechnol, 2010, 5: 722–726
46 Cui X, Lee G-H, Kim Y D, et al. Multi-terminal transport measurements of MoS_2 using a van der Waals heterostructure device platform. Nat Nanotechnol, 2015, 10: 534–540
47 Yoon Y, Ganapathi K, Salahuddin S. How good can monolayer MoS_2 transistors be? Nano Lett, 2011, 11: 3768–3773
48 Alam K, Lake R K. Monolayer MoS_2 transistors beyond the technology road map. IEEE Trans Electron Dev, 2012, 59: 3250–3254
49 Liu F, Wang Y, Liu X, et al. A theoretical investigation of orientation dependent transport in monolayer MoS_2 transistors at the ballistic limit. IEEE Electron Dev Lett, 2015, 36: 1091–1093
50 Liu L T, Lu Y, Guo J. On monolayer MoS_2 field-effect transistors at the scaling limit. IEEE Trans Electron Dev, 2013, 60: 4133–4139
51 Chang J, Register L F, Banerjee S K. Atomistic full-band simulations of monolayer MoS_2 transistors. Appl Phys Lett, 2013, 103: 223509
52 Yang L M, Majumdar K, Du Y C, et al. High-performance MoS_2 field-effect transistors enabled by chloride doping: record low contact resistance (0.5 kohm* μm) and record high drain current (460 μA/μm). In: Proceedings of 2014 Symposium on VLSI Technology: Digest of Technical Papers, Honolulu, 2014. 192–193
53 Li X F, Yang L M, Si M W, et al. Performance potential and limit of MoS_2 transistors. Adv Mater, 2015, 27: 1547–1552
54 Wu Y Q, Farmer D B, Xia F N, et al. Graphene electronics: materials, devices, and circuits. Proc IEEE, 2013, 101: 1620–1637
55 Wu Y Q, Lin Y-m, Bol A A, et al. High-frequency, scaled graphene transistors on diamond-like carbon. Nature, 2011, 472: 74–78
56 Wu Y Q, Jenkins K A, Valdes-Garcia A, et al. State-of-the-art graphene high-frequency electronics. Nano Lett, 2012, 12: 3062–3067
57 Wang H, Yu L L, Lee Y-H, et al. Large-scale 2D electronics based on single-layer MoS_2 grown by chemical vapor deposition. In: Proceedings of the 2012 International Electron Devices Meeting, San Francisco, 2012. 4.6.1–4.6.4
58 Krasnozhon D, Lembke D, Nyffeler C, et al. MoS_2 transistors operating at gigahertz frequencies. Nano Lett, 2014, 14: 5905–5911
59 Cheng R, Jiang S, Chen Y, et al. Few-layer molybdenum disulfide transistors and circuits for high-speed flexible electronics. Nat Commun, 2014, 5: 5143
60 Sanne A, Ghosh R, Rai A, et al. Radio frequency transistors and circuits based on CVD MoS_2. Nano Lett, 2015, 15: 5039–5045
61 Hooge F. 1/f noise sources. IEEE Trans Electron Dev, 1994, 41: 1926–1935
62 Von Haartman M, Mikael Ö. Low-frequency Noise in Advanced MOS Devices. Berlin: Springer, 2007
63 Razavi B. A study of phase noise in CMOS oscillators. IEEE J Solid-State Circ, 1996, 31: 331–343
64 Sangwan V K, Arnold H N, Jariwala D, et al. Low-frequency electronic noise in single-layer MoS_2 transistors. Nano Lett, 2013, 13: 4351–4355
65 Kwon H-J, Kang H, Jang J, et al. Analysis of flicker noise in two-dimensional multilayer MoS_2 transistors. Appl

Phys Lett, 2014, 104: 083110
66 Renteria J, Samnakay R, Rumyantsev S L, et al. Low-frequency 1/f noise in MoS_2 transistors: relative contributions of the channel and contacts. Appl Phys Lett, 2014, 104: 153104
67 Rumyantsev S L, Jiang C L, Samnakay R, et al. 1/f noise characteristics of MoS_2 thin-film transistors: comparison of single and multilayer structures. IEEE Electron Dev Lett, 2015, 36: 517–519
68 Keyes R W. The electrical properties of black phosphorus. Phys Rev, 1953, 92: 580–584
69 Morita A. Semiconducting black phosphorus. Appl Phys A, 1986, 39: 227–242
70 Buscema M, Groenendijk D J, Blanter S I, et al. Fast and broadband photoresponse of few-layer black phosphorus field-effect transistors. Nano Lett, 2014, 14: 3347–3352
71 Buscema M, Groenendijk D J, Steele G A, et al. Photovoltaic effect in few-layer black phosphorus PN junctions defined by local electrostatic gating. Nat Commun, 2014, 5: 4651
72 Zhu W N, Yogeesh M N, Yang S X, et al. Flexible black phosphorus ambipolar transistors, circuits and AM demodulator. Nano Lett, 2015, 15: 1883–1890
73 Fei R X, Yang L. Strain-engineering the anisotropic electrical conductance of few-layer black phosphorus. Nano Lett, 2014, 14: 2884–2889
74 Hong T, Chamlagain B, Lin W Z, et al. Polarized photocurrent response in black phosphorus field-effect transistors. Nanoscale, 2014, 6: 8978–8983
75 Ong Z-Y, Cai Y Q, Zhang G, et al. Strong thermal transport anisotropy and strain modulation in single-layer phosphorene. J Phys Chem C, 2014, 118: 25272–25277
76 Ong Z-Y, Zhang G, Zhang Y W. Anisotropic charged impurity-limited carrier mobility in monolayer phosphorene. J Appl Phys, 2014, 116: 214505
77 Qiao J S, Kong X H, Hu Z-X, et al. High-mobility transport anisotropy and linear dichroism in few-layer black phosphorus. Nat Commun, 2014, 5: 4475
78 Ge S F, Li C K, Zhang Z M, et al. Dynamical evolution of anisotropic response in black phosphorus under ultrafast photoexcitation. Nano Lett, 2015, 15: 4650–4656
79 Jiang J-W. Thermal conduction in single-layer black phosphorus: highly anisotropic? Nanotechnology, 2015, 26: 055701
80 Lu W L, Ma X M, Fei Z, et al. Probing the anisotropic behaviors of black phosphorus by transmission electron microscopy, angular-dependent Raman spectra, and electronic transport measurements. Appl Phys Lett, 2015, 107: 021906
81 Wang X M, Jones A M, Seyler K L, et al. Highly anisotropic and robust excitons in monolayer black phosphorus. Nat Nanotechnol, 2015, 10: 517–521
82 Xia F N, Wang H, Jia Y C. Rediscovering black phosphorus as an anisotropic layered material for optoelectronics and electronics. Nat Commun, 2014, 5: 4458
83 Du Y C, Liu H, Deng Y X, et al. Device perspective for black phosphorus field-effect transistors: contact resistance, ambipolar behavior, and scaling. ACS Nano, 2014, 8: 10035–10042
84 Haratipour N, Robbins M C, Koester S J. Black phosphorus p-MOSFETs with 7-nm HfO_2 gate dielectric and low contact resistance. IEEE Electron Dev Lett, 2015, 36: 411–413
85 Das S, Demarteau M, Roelofs A. Ambipolar phosphorene field effect transistor. ACS Nano, 2014, 8: 11730–11738
86 Perello D J, Chae S H, Song S, et al. High-performance n-type black phosphorus transistors with type control via thickness and contact-metal engineering. Nat Commun, 2015, 6: 7809
87 Liu H, Neal A T, Si M W, et al. The effect of dielectric capping on few-layer phosphorene transistors: tuning the schottky barrier heights. IEEE Electron Dev Lett, 2014, 35: 795–797
88 Padilha J E, Fazzio A, da Silva A J R. van der Waals heterostructure of phosphorene and graphene: tuning the schottky barrier and doping by electrostatic gating. Phys Rev Lett, 2015, 114: 066803
89 Kamalakar M V, Madhushankar B N, Dankert A, et al. Low schottky barrier black phosphorus field-effect devices with ferromagnetic tunnel contacts. Small, 2015, 11: 2209–2216
90 Joshua O I, Gary A S, Herre S J v d Z, et al. Environmental instability of few-layer black phosphorus. 2D Mater, 2015, 2: 011002
91 Wood J D, Wells S A, Jariwala D, et al. Effective passivation of exfoliated black phosphorus transistors against ambient degradation. Nano Lett, 2014, 14: 6964–6970
92 Boukhvalov D W, Rudenko A N, Prishchenko D A, et al. Chemical modifications and stability of phosphorene with impurities: a first principles study. Phys Chem Chem Phys, 2015, 17: 15209–15217
93 Wang Z H, Islam A, Yang R, et al. Environmental, thermal, and electrical susceptibility of black phosphorus field effect transistors. J Vac Sci Technol B, 2015, 33: 052202
94 Saito Y, Iwasa Y. Ambipolar insulator-to-metal transition in black phosphorus by ionic-liquid gating. ACS Nano, 2015, 9: 3192–3198
95 Kim J-S, Liu Y N, Zhu W N, et al. Toward air-stable multilayer phosphorene thin-films and transistors. Sci Rep, 2015, 5: 8989
96 Favron A, Gaufres E, Fossard F, et al. Photooxidation and quantum confinement effects in exfoliated black phosphorus. Nat Mater, 2015, 14: 826–832
97 Ziletti A, Carvalho A, Campbell D K, et al. Oxygen defects in phosphorene. Phys Rev Lett, 2015, 114: 046801
98 Zhu H, McDonnell S, Qin X Y, et al. Al_2O_3 on black phosphorus by atomic layer deposition: an in situ interface study. ACS Appl Mater Interface, 2015, 7: 13038–13043

99 Cai Y Q, Zhang G, Zhang Y-W. Electronic properties of phosphorene/graphene and phosphorene/hexagonal boron nitride heterostructures. J Phys Chem C, 2015, 119: 13929–13936

100 Chen X L, Wu Y Y, Wu Z F, et al. High-quality sandwiched black phosphorus heterostructure and its quantum oscillations. Nat Commun, 2015, 6: 7315

101 Doganov R A, Koenig S P, Yeo Y, et al. Transport properties of ultrathin black phosphorus on hexagonal boron nitride. Appl Phys Lett, 2015, 106: 083505

102 Doganov R A, O'Farrell E C T, Koenig S P, et al. Transport properties of pristine few-layer black phosphorus by van der Waals passivation in an inert atmosphere. Nat Commun, 2015, 6: 6647

103 Gillgren N, Wickramaratne D, Shi Y M, et al. Gate tunable quantum oscillations in air-stable and high mobility few-layer phosphorene heterostructures. 2D Mater, 2015, 2: 011001

104 Li L K, Ye G J, Tran V, et al. Quantum oscillations in a two-dimensional electron gas in black phosphorus thin films. Nat Nanotechnol, 2015, 10: 608–613

105 Tayari V, Hemsworth N, Fakih I, et al. Two-dimensional magnetotransport in a black phosphorus naked quantum well. Nat Commun, 2015, 6: 7702

106 Yasaei P, Kumar B, Foroozan T, et al. High-quality black phosphorus atomic layers by liquid-phase exfoliation. Adv Mater, 2015, 27: 1887–1892

107 Kang J, Wood J D, Wells S A, et al. Solvent exfoliation of electronic-grade, two-dimensional black phosphorus. ACS Nano, 2015, 9: 3596–3604

108 Yang Z B, Hao J H, Yuan S G, et al. Field-effect transistors based on amorphous black phosphorus ultrathin films by pulsed laser deposition. Adv Mater, 2015, 27: 3748–3754

109 Li X S, Deng B C, Wang X M, et al. Synthesis of thin-film black phosphorus on a flexible substrate. 2D Mater, 2015, 2: 031002

110 Wang H, Wang X M, Xia F N, et al. Black phosphorus radio-frequency transistors. Nano Lett, 2014, 14: 6424–6429

111 Vandamme L, Li X S, Rigaud D. 1/f noise in MOS devices, mobility or number fluctuations? IEEE Trans Electron Dev, 1994, 41: 1936–1945

112 Na J H, Lee Y T, Lim J A, et al. Few-layer black phosphorus field-effect transistors with reduced current fluctuation. ACS Nano, 2014, 8: 11753–11762

113 Li X F, Du Y C, Si M W, et al. Mechanisms of current fluctuation in ambipolar black phosphorus field-effect transistors. Nanoscale, 2016, 8: 3572–3578