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# Fully depleted SOI (FDSOI) technology

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**Abstract** Fully depleted SOI (FDSOI) has become a viable technology not only for continued CMOS scaling to 22 nm node and beyond but also for improving the performances of legacy technology when retrofitting to old technology nodes. In this paper, we provide an overview of FDSOI technology, including the benefits and challenges in FDSOI design, manufacturing, and ecosystem. We articulate that FDSOI is potential cornerstone for China to catch up and leapfrog in semiconductor technology.

**Keywords** FDSOI, design, foundry, variability, low power, strain engineering, IoT

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## 1 Introduction

Semiconductor technology has become vital in almost all areas from consumer electronics such as personal computers (PC), smartphones, tablets, to enterprise applications such as servers, networks, healthcare, finance, and security. The worldwide semiconductor revenue is estimated to be $333 billion in 2014 according to the Semiconductor Industry Association (SIA) [1]. The recent surge of Internet-of-things (IoT) is the new driving force to fuel the further growth of semiconductor technology that is largely built on the seemingly endless advance of CMOS technology. The primary mission of CMOS scaling is to provide smaller and faster transistors from one node to the next, best described by Moore's Law [2]. Historically CMOS technology advanced to next node every 1.5–2 years. It has become clear that such a node advancement has slowed down to about 2.5–3 years in recent years. The slowdown is partly due to the inherent challenges in manufacturing and yielding 3D FinFET [3], and partly due to the increasing design and patterning difficulties with shrinking ground rules. Mainstream CMOS devices have been fabricated on bulk silicon substrates owing to the universal availability and low cost of bulk silicon wafers. Unfortunately, scaling bulk CMOS transistors (Figure 1(a)) beyond 22 nm node face tremendous challenges, particularly for low-power applications. According to Dennard's scaling theory [4], which prescribes the recipe for the transistor miniaturization, the channel doping (or halo doping) concentration has to increase to suppress the short-channel effects due to gate length scaling. Unfortunately, increasing halo doping causes two major issues: First, high doping concentration leads to the increase of the electrical

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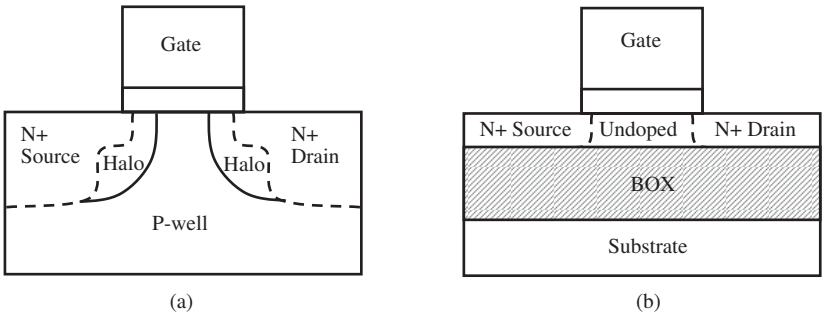


**Figure 1** A schematic cross-section of (a) bulk MOSFET and (b) FDSOI MOSFET. Bulk MOSFET scaling relies on increase of halo and well doping, resulting in increase of GIDL leakage current and device variability. In contrast, FDSOI has undoped thin SOI channel to achieve short-channel control.

field across the PN junction and thus the increase of the gate-induced-drain-leakage (GIDL) current due to enhanced band-to-band tunneling [5]. The total transistor leakage current may go up when the increase of GIDL current outweighs the reduction of subthreshold leakage. Second, increasing channel/halo doping increases device variability due to increased random dopant fluctuation (RDF) [6].

Fully depleted SOI (FDSOI) is a viable device architecture to continue CMOS scaling without relying on channel or halo doping (Figure 1(b)). In fact, the channel of FDSOI transistors is typically undoped to eliminate the RDF while achieving superior short-channel control when SOI channel thickness is about 1/4 of the gate length. GIDL leakage current is also minimized thanks to the reduced electrical field across the PN junction. FDSOI has been extensively studied [7–40] and it is impossible to include all references in this paper. Besides FDSOI, other terminologies used in the literature to depict FDSOI include ultra-thin body (UTB) [7–9], ultra-thin body and BOX (UTBB or UT2B) [13–16], silicon on thin BOX (SOTB) [17, 18], ultra-thin SOI (UTSOI) [19–22], extremely thin SOI (ETSOI) [27–34], and depleted substrate transistor (DST) [35]. In textbook FDSOI transistor is defined as a transistor with a fully depleted channel in contrast to partially depleted SOI (PDSOI). To render FDSOI a viable technology, however, the actual SOI thickness needs to be substantially thin to achieve good electrostatics. A rule of thumb is that the FDSOI channel thickness needs to be about 1/4 of the gate length. Figure 2 illustrates the unique advantages of FDSOI over other device architectures. In addition to the superior electrostatics, inherent low device variability, the planar structure of FDSOI avoids the additional manufacturing challenges associated with the 3D device architectures such as fins and nanowires. Compared with PDSOI technology that has been used for high performance applications since 180 nm node [41], FDSOI with a channel thinner than about 12 nm does not exhibit the history effect [42], thus avoiding the associated design complexity. FDSOI channel is isolated from the substrate by a (usually thin) buried oxide (BOX). The use of a thin BOX layer, typically 25 nm or less, provides a reasonable body factor in the order of 100 mV/V or so [10–18]. This means that by applying a voltage to the wells placed under the BOX it is possible to modulate the transistor $V_T$ in the same manner it has been practiced in bulk planar CMOS for many years. To reduce the access resistance to the thin SOI layer, typically raised source/drain (RSD) structures are needed and formed using selective epitaxial growth [12, 14, 26–31].The TEM image in Figure 3 shows an FDSOI transistor with 5 nm SOI channel thickness, 20 nm gate length, gate-first high-k/metal gate (80 nm gate pitch), and epitaxial RSD.

## 2 FDSOI device design

At a high level FDSOI device design is not different from the conventional CMOS design in which the primary goal is to achieve the optimal tradeoff among three competing factors, *performance, power, and density*. The figure of merit of DC performance is typically measured by the drive current (effective drive current $I_{\mathrm{EFF}}$) at a given off current ($I_{\mathrm{OFF}}$) and operating voltage ($V_{\mathrm{DD}}$). FDSOI improves the MOSFET electrostatics [40], i.e., reduces the subthreshold swing (SS) and drain-induced-barrier-lowering (DIBL). For a given off current target, FDSOI can have a lower threshold voltage ($V_T$) than bulk MOSFET.

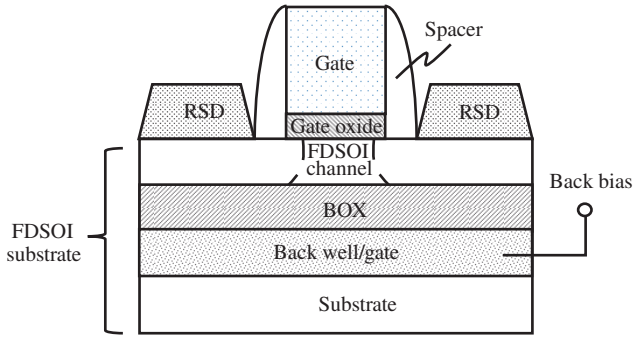


**Figure 2** A schematic cross-section of FDSOI MOSFET. The unique feature of FDSOI is the back gate underneath the buried oxide (BOX) layer. The back gate can be doped and/or biased and enables $V_T$ tuning to boost device performance or reduce standby power. The raised source/drain (RSD) is needed to reduce S/D and contact resistances. Undoped channel eliminates RDF-induced device variability.

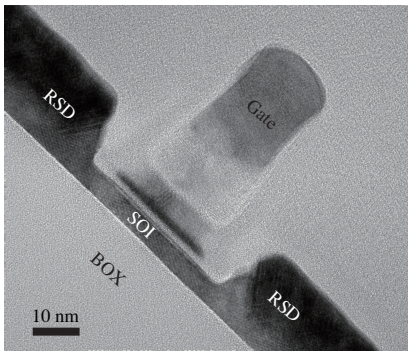


**Figure 3** TEM cross-section of an FDSOI transistor with 5 nm SOI channel thickness, 20 nm gate length, gate-first high-k/metal gate, and raised source/drain (RSD).

The lower $V_T$ translates to higher over drive $(V_{\rm GS} - V_T)$ and thus higher drive current, as indicated by Eqs. 1–3 [44] and illustrated in Figure 4. Alternatively, one can tradeoff the drive current with power consumption. In other words, FDSOI can provide the same drive current at lower $V_{\rm DD}$, resulting in reduction in both active power (proportional to $V_{\rm DD}^2$) and standby power (proportional to $V_{\rm DD}$).

$$I_D \propto C_{\rm inv}(V_{\rm GS} - V_T)\ v, \tag{1}$$

$$V_T = {\rm SS}\log(I_{\rm REF}/I_{\rm OFF}) = \alpha\,{\rm SS}. \tag{2}$$

Substituting (2) into (1) results in

$$I_D \propto C_{\rm inv}(V_{\rm GS} - \alpha\,{\rm SS})v, \tag{3}$$

where $I_D$ is the saturation drive current, $C_{\rm inv}$ is the inversion capacitance, $v$ is the effective carrier velocity, $I_{\rm REF}$ is the drain current at $V_{\rm GS} = V_T$, and $\alpha = \log(I_{\rm REF}/I_{\rm OFF})$.

For a given $I_{\rm OFF}$ target, FDSOI has lower threshold voltage ($V_T$) and thus provides higher overdrive $(V_{\rm GS} - V_T)$ and higher drive current.

### 2.1 Multi-$V_T$ options in FDSOI

Availability of a variety of transistors with a large range of threshold voltage ($V_T$) is essential for designing high performance/low power chips. In conventional bulk CMOS, multi-$V_T$ is achieved by using different channel doping and/or different gate lengths. However, these approaches have drawbacks when used in advanced nodes. Channel doping increases device variation due to RDF. In future technologies different gate lengths requires additional masks and processes. In FDSOI, however, multiple $V_T$ can be achieved by using different doping underneath the BOX layer [12–15] while keeping the FDSOI channel undoped, essentially resulting in ideal super-steep retrograde well (SSRW) transistors without RDF. Furthermore, since the back doping layer is isolated from the source/drain by BOX layer in FDSOI structure, one has the freedom to choose the well polarity (even the same polarity of dopants can be used in the well and in S/D). There is no S/D to well junction leakage or short in FDSOI devices. For typical BOX thickness of 20–25 nm, swapping the well polarity, as shown in Figure 5, results in a $V_T$ shift of about 100 mV [12–15]. In addition, transistor $V_T$ can be further tuned by applying different well bias. A constant well bias results in a fixed $V_T$ while a dynamic bias based on workload can be used for power management.

Figure 6 depicts a possible multi-$V_T$ scenario in FDSOI starting with regular $V_T$ (RVT) devices formed on conventional wells and low $V_T$ (LVT) devices on flipped wells. Flipped wells are forward biased to get super low $V_T$ (SLVT) devices and conventional wells are reverse biased to get high $V_T$ (HVT) devices. Furthermore, the adoption of strained channel SiGe (cSiGe) in high performance FDSOI PFET provides an additional knob to achieve multi-$V_T$. Compared with Si PFET, SiGe PFET with 23% Ge

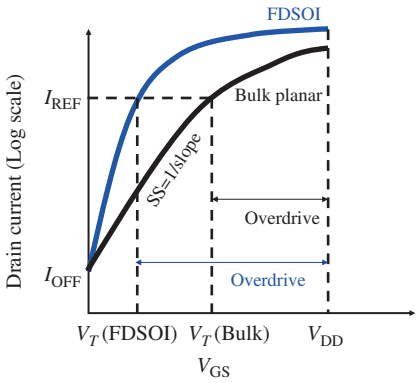


**Figure 4** (Color online) Illustration of how steeper subthreshold swing (SS) of FDSOI translates to higher performance over bulk planar MOSFET. For a given $I_{OFF}$ target, FDSOI has lower threshold voltage ($V_T$) and thus provides higher overdrive ($V_{GS} - V_T$) and higher drive current.

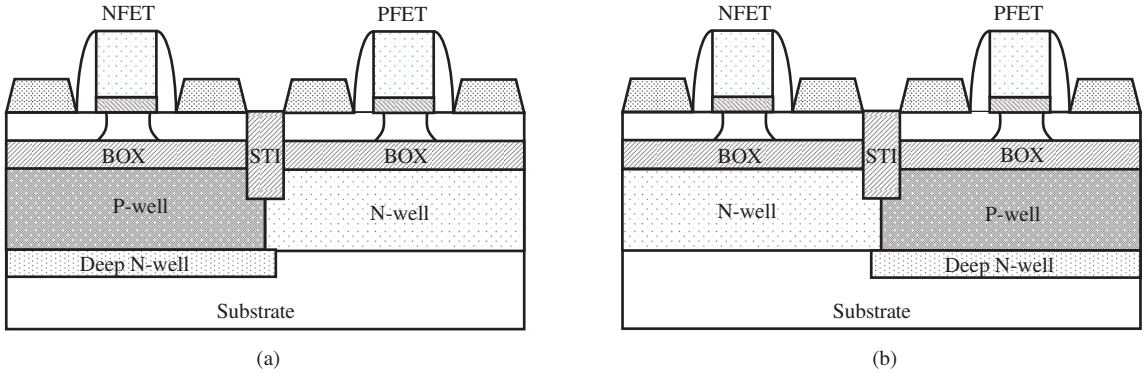


**Figure 5** FDSOI transistors formed on (a) conventional and (b) flipped wells.

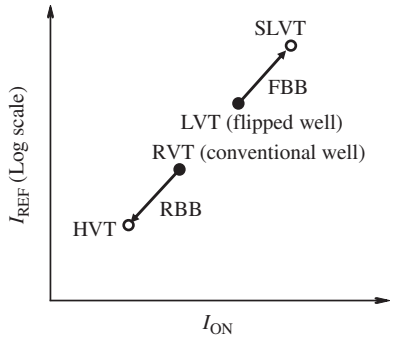


**Figure 6** A possible multi-$V_T$ FDSOI scheme. Starting with RVT devices formed on conventional wells (NFET on p-well and PFET on n-well) and LVT devices on flipped wells (NFET on n-well and PFET on p-well). Flipped wells are forward biased (FBB) to get SLVT devices and conventional wells are reverse biased (RBB) to get HVT devices. RVT = regular $V_T$, LVT = low $V_T$, SLVT = super low $V_T$, HVT = high $V_T$.

results in 250 mV $V_T$ reduction [32]. Therefore, one can use SiGe transistors for high performance (low $V_T$) applications such as critical logic path and use Si transistors channel for low leakage (high $V_T$) applications such as SRAM as shown in Figure 7. Only two workfunction (WF) metal gates are needed to produce all types of NFET and PFET transistors.

## 2.2 SRAM

Low operating voltage SRAM is highly desired for both high performance (HP) and high density (HD) applications. Device variation is a critical factor gating the implementation of low voltage SRAM. Device

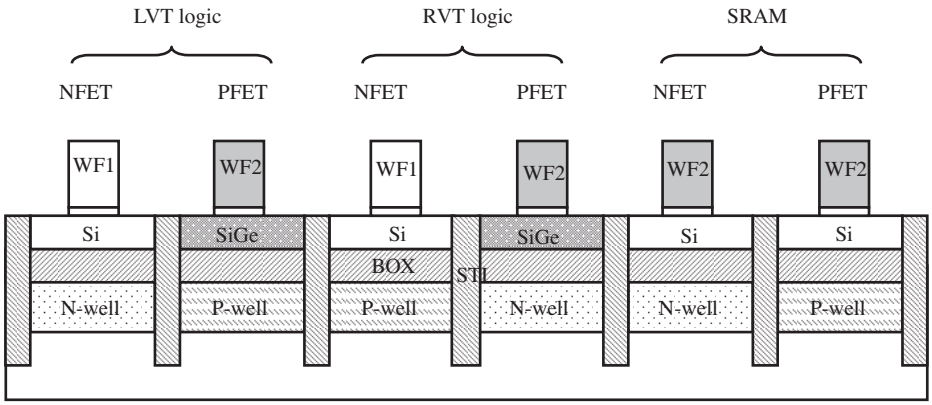


**Figure 7** Schematics showing a multi-$V_T$ scheme for FDSOI technology with cSiGe [32]@ Copyright 2012 IEEE.

variability can be classified as global variation and local variation. Global variations are mainly due to the across wafer and/or across chip non-uniformity of CMOS manufacturing processes, such as pattern dependent etching, deposition, implantation doses, and temperature gradients. Global variation can typically be minimized by process optimization. In contrast, local variation in bulk CMOS technology is much more difficult to minimize. This is due to the fact that bulk CMOS relies on channel doping to set transistor $V_T$. Consequently, device variation due to random dopant fluctuation (RDF) becomes inevitable for bulk CMOS. FDSOI has intrinsically low variability simply because it does not need channel doping to set transistor $V_T$ as discussed earlier. Even with the back gate doping below BOX, FDSOI $V_T$ is mainly set by doping polarity, not doping concentration. As a result, undoped channels are maintained in FDSOI and local variability is minimized. In fact, record low device variability has been achieved in FDSOI transistors with $A_{\rm VT}$ of 1.25 mV·μm or below [25,31], substantially lower than any $A_{\rm VT}$ that has been reported with bulk planar and FinFET transistors. $A_{\rm VT}$ is the slope of the Pelgrom plot (standard deviation of $V_T$ mismatch of paired transistors vs. square root of the product of transistor gate length and width) [45]. Detailed comparison of device variability of FDSOI, bulk planar, and FinFET is summarized in the literature (see References [46, 47] for example). Although in principle FinFETs can be made with undoped or lightly doped channels, in practice FinFET SRAM transistors still require channel doping to achieve high $V_T$, leading to significant RDF and thus high device variability. Furthermore, global $V_T$ variability can be compensated in FDSOI by applying proper body bias. FDSOI SRAM with operation voltage down to 0.37 V has been reported without any assisting techniques [48]. It is also worth noting that since the well is isolated from the channel, FDSOI NFETs and PFETs can have the same well doping/bias and a single metal gate, opening further opportunity for high density SRAM.

### 2.3 Analog and RF

Designing analog and RF circuits requires low transistor mismatch, high intrinsic device gain ($g_m/g_{\rm ds}$ ratio), low noise, and flexibility in $V_T$ tuning. FDSOI is the only device architecture that meets all those requirements. Bulk planar CMOS suffers from large transistor mismatch due to RDF and low device gain due to poor electrostatics. FinFET improves electrostatics but it lacks the back bias capability. The ability to tune $V_T$ to compensate for process mismatch or drift and to offer virtually any $V_T$ desired by analog designers is a unique feature. In fact, near zero $V_T$ can be readily achieved in FDSOI without compromising other device characteristics, providing a great opportunity for low voltage analog design. The superior electrostatics of FDSOI over bulk CMOS enables scaling of analog devices while maintaining a high transistor gain ($g_m/g_{\rm ds}$ ratio). As shown in Figure 8, to achieve a gain of 40, the gate length can be reduced from over 300 nm in bulk planar CMOS to 100 nm in FDSOI [31]. Gate length scaling further benefits transistor performance as the drive current increases and $L_G$ decreases. An $f_T$ of 300 GHz has been already demonstrated in FDSOI technology for both NFET and PFET [49] showing its competitiveness for analog and RF applications.

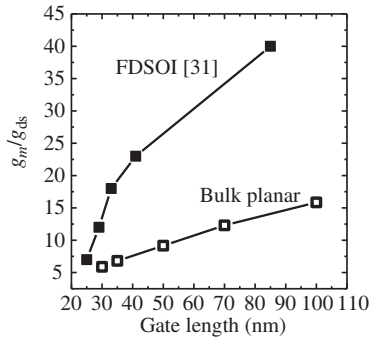


**Figure 8** Transistor gain ($g_m/g_{ds}$) as a function of gate length in FDSOI and bulk planar technologies.

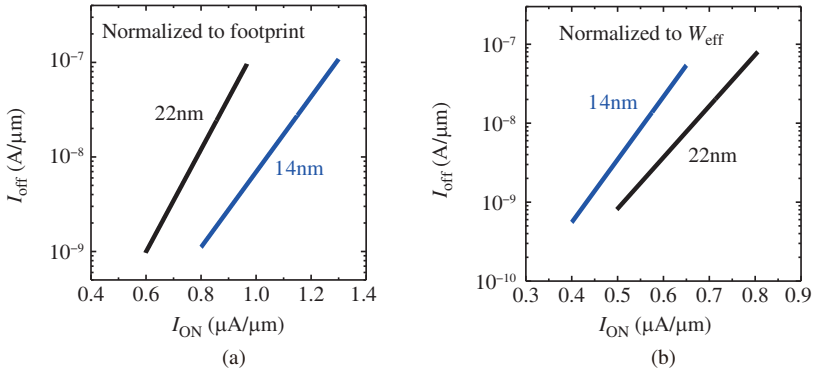


**Figure 9** (Color online) (a) FinFET NFET performance, when normalized to layout footprint, increases from 22 nm node to 14 nm node. (b) The intrinsic transistor performance, when normalized to the actual transistor width (fin width plus 2 times the fin height), however, decreases from 22 nm node to 14 nm node. Fin pitch: 60 nm and 42 nm for 22 nm node and 14 nm node, respectively; Fin height: 34 nm and 42 nm for 22 nm node and 14 nm node respectively. Data from [56, 58].

### 2.4 High performance FDSOI

Strain engineering has become essential for improving CMOS performance since 90 nm node. The classic strain engineering techniques in bulk CMOS include embedded source/drain stressors (eSiGe for PFET [50–52] and Si:C for NFET [52]), dual stress contact etch liner (tensile liner for NFET and compressive liner for PFET [53]), and stress memorization technique (SMT) for NFET [54,55]. The thin SOI in FDSOI structure prevents embedded S/D stressors and SMT. The lack of the conventional strain technique in FDSOI structure leads to the common misconception that the performances of FDSOI devices are inferior to that of bulk planar and FinFET. It should be noted, however, that the conventional strain techniques start to run out of steam when contact gate pitch (CPP) is scaled to 100 nm and below. The entire device pitch is occupied by the essential device elements (gate, spacers, S/D contacts), leaving no room for stress liners regardless of the device architecture. Furthermore, embedded S/D stressor and SMT becomes less and less effective for FinFET and as the volume available for stressors shrinks. Although it has been boasted that FinFET transistor performance for a given layout footprint keeps increasing by shrinking fin pitch and increasing fin height (Figure 9(a)), the intrinsic FinFET transistor performance, when normalized to the effective transistor width (fin width plus 2 times the fin height), actually decreases from 22 nm node [4, 56] to 14 nm node [57, 58] (Figure 9(b)). The degradation of the intrinsic FinFET transistor performance should not be surprising due to diminishing effectiveness of strain and increase of parasitic resistance in highly scaled FinFET.

Contrary to the common misconception, high performance FDSOI devices have been demonstrated by using *intrinsically strained channels*, i.e., tensily strained silicon for NFET and compressively strained SiGe for PFET [30, 32, 59]. As shown in Figures 10 and 11, at $V_{DD}$ = 0.9 V and $I_{OFF}$ = 100 nA/μm, $I_{EFF}$ is 820 μA/μm and 615 μA/μm for NFET and PFET, respectively. Unlike the conventional strain

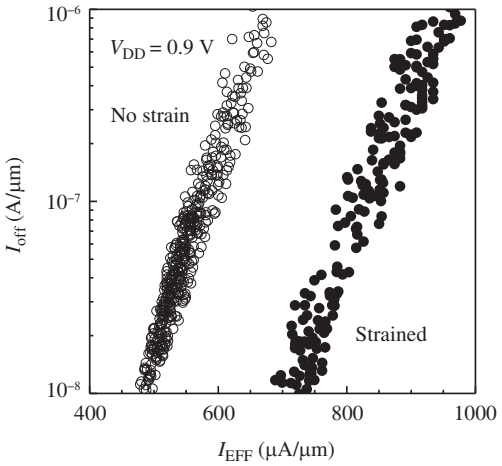


**Figure 10** $I_{EFF}$-$I_{OFF}$ plot of strained Si vs non-strained Si NFET transistors. $I_{EFF}$ of 820 μA/μm is achieved for tensily strained NFET $V_{DD}$ = 0.9 V and $I_{OFF}$ = 100 nA/μm.

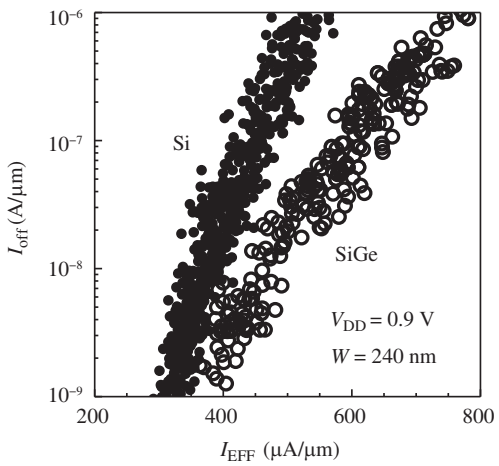


**Figure 11** $I_{EFF}$-$I_{OFF}$ plot of Si vs SiGe FDSOI PFET transistors. $I_{EFF}$ of 615 μA/μm is achieved for compressively strained SiGe PFET. $V_{DD}$ = 0.9 V and $I_{OFF}$ = 100 nA/μm [32]@ Copyright 2012 IEEE.

engineering techniques that have diminishing benefits as CPP decreases, channel strain engineering is highly effective and its benefit actually increases from node to node due to the reduction of device width. This is due to the fact that the channel strain configuration transitions from biaxial in wide transistors to uniaxial in narrow transistors. Uniaxial strain is more effective than biaxial strain in enhancing device performances as shown in Figure 12 [32].

### 2.5 Body biasing in FDSOI

Body bias has been used in bulk planar CMOS for many generations [60] and it has been identified as a key technology enabler [61]. With the desire to reduce $V_{DD}$ below 0.8 V in order to reduce active power, managing the device variability becomes increasingly important. A primary application of body bias is to manage device variation. The reduction in active power by body bias is equivalent to scaling CMOS by one node [62, 63]. Another application of body bias is to dynamically adjust transistor speed by adjusting transistor $V_T$ based on the workload. Body bias can be used in conjunction with or in lieu of dynamic voltage and frequency scaling (DVFS). Unlike DVFS in which the voltage source delivers the current to the entire circuit block, body bias applies voltage only to wells. The current drawn to bias the wells is significantly smaller than the current supplied to $V_{DD}$ of the circuit and thus relatively small charge pump and/or voltage regulator circuits can be used to generate the body bias. Unfortunately, the effectiveness of body bias diminishes in highly scaled bulk CMOS and it is completely vanished in FinFET technologies. FDSOI technology not only restores the ability of body biasing, but also extends the range of body bias by allowing forward back bias (FBB) thanks to the isolation of back gates (wells) from FDSOI channel by buried oxide layer (BOX). It has been demonstrated that 28 nm FDSOI can deliver performances exceeding 20 nm bulk technology [64] when FBB is used.

The next driver of semiconductor technology is Internet-of-Things (IoT) which requires ultra-low voltage (ULV) design to enable energy harvesting or lifetime battery operations. Reducing the operating voltage to 0.5 V or less is essential for ultra-low power IoT applications. In ULV designs transistors are operated near threshold voltage or in subthreshold region and both standby power and circuit speed depend exponentially on $V_T$. Minimizing $V_T$ variability is thus crucial for improving circuit speed and reducing standby power. The typical performance of bulk CMOS circuits operating at low voltages such as 0.4 V is considerably low (less than a MHz). In contrast, FDSOI for the first time enables performance numbers in the range of hundreds of MHz at 0.4 V [65]. The significant performance improvement in FDOSI comes from the wide range of FBB capability which enables lowering of $V_T$ at low $V_{DD}$ in conjunction with reducing the $V_T$ variability by intrinsically undoped channels.

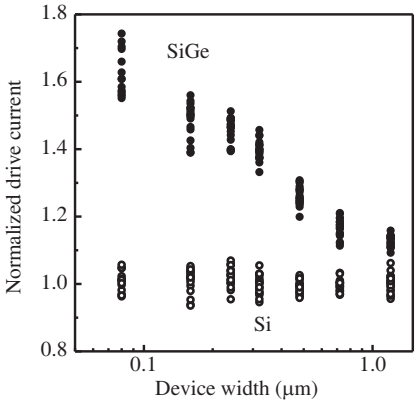


**Figure 12** Drive current vs. device width showing the drive current enhancement of SiGe PFET by reducing the device width as a result from stress transformation from biaxial in wide devices to uniaxial in narrow devices. The drive current of non-strained Si PFET is independent of device width [32]@ Copyright 2012 IEEE.

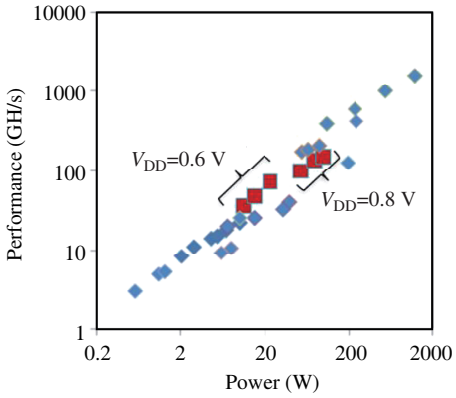


**Figure 13** (Color online) Performance vs. power for SHA-256 mining ASIC chips implemented in 28 nm node. FDSOI data [69] is marked in red and are achieved by applying FBB (0, 0.6 V, and 1.1 V) for each $V_{DD}$ of 0.6 V and 0.8 V. Other data points are taken from [70].

### 2.6 Energy efficient computing in FDSOI: a case study from China

Several publications have already demonstrated the merits of the FDSOI technology to improve energy efficiency of CMOS circuits at 65 nm [66] and 28 nm [67,68]. However, the general belief is that advantage of FDSOI and its body biasing capability is only limited to low-power, low-performance applications.

Recent announcement of the new cryptocurrency ASIC chip by SFARDS [69] is yet another testimony that clearly shows the advantages of FDSOI and body biasing for high performance, energy-efficient, applications. Several companies have already designed mining ASICs at 28 nm node with virtually the same goal, i.e., executing SHA-256 hashing algorithm at the minimum energy and Si cost. Therefore, even though mining ASICs is not a high-volume segment of the CMOS industry, it provides an ideal benchmark to understand the advantages of forward body biasing (FBB) for high performance computing.

As a benchmark, Figure 13 plots the performance (GH/s) as a function of power for a set of 28 nm mining chips based on the data published [69,70]. The power over performance ratio in units of (W/GH/s) or equally (J/GH) is a measure of the energy efficiency of the chip and is often reported by ASIC vendors along with the maximum performance in terms of (GH/s). These two metrics are actually important for the end user; the former determines the electricity cost per operation, while the latter determines, albeit indirectly, silicon cost to deliver a target performance.

A few observations can be made based on the data in Figure 13. First of all, like any other CMOS circuit, the FDSOI ASIC is more energy efficient when operating at lower $V_{DD}$ [71]. Energy per operation is roughly 0.55 J/GH at 0.8 V and drops to about 0.3 J/GH at 0.6 V. At 0.45 V (not shown) it further drops to 0.19 J/GH. The improved energy efficiency at lower $V_{DD}$, of course at the expense of lower performance, is well understood and is often referred to "under-clocking" by the mining community. In any CMOS circuit, active energy per operation is simply proportional to $V_{DD}^2$. Leakage energy per operation, however, increases as $V_{DD}$ is lowered, simply because it takes longer to deliver a given task. The net effect is that the total energy reaches its minimum at a relatively low $V_{DD}$, which depending on the circuit and technology, happens to be near or even lower than the threshold voltage of the transistors.

As stated earlier, energy efficiency achieved by operating at lower $V_{DD}$ comes at the expense of reduced performance. To meet a desired performance, e.g., a target GH/s, one can increase the number of cores in a chip or number of chips on a board. This "throw-more-silicon-at-it" strategy has been practiced by some of the major vendors of mining ASIC chips. In fact, many of the data points in Figure 13 are from chips (or even multi-chip in package) implementations that use many cores operating at 0.6 V, which is lower than the nominal operating voltage of the high performance 28 nm technology they used. Increasing the Si area to compensate for the lower performance at low $V_{DD}$, of course, increases the system cost,

which is not desirable to the end user.

FDSOI technology can be used to address the above concerns. By keeping the channel undoped and hence eliminating random dopant fluctuation (RDF), FDSOI offers record low $V_T$ variability [25, 31]. Global $V_T$ variations can be compensated fairly easily by applying a body bias. Furthermore, wide range body biasing that is unique to the FDSOI technology, can be used to break the trade-off between performance and energy efficiency. At a given $V_{\rm DD}$, it is possible to increase the performance of the FDSOI chip by applying FBB without compromising the energy efficiency. The advantage of lowering $V_T$ by applying a FBB to improve energy efficiency has been known for a long time [72]. However, in a bulk technology, maximum FBB voltage that can be applied to the wells without causing excessive junction leakage is limited to about 0.4 V [72]. FDSOI implementation at 28 nm employs flipped-well structure for LVT transistors, i.e., n-well under NFETs and p-well under PFETs, which allows up to 2 V of FBB without leakage concerns. The ASIC chip above uses a maximum FBB of 1.1 V, which is conservative compared to what is achievable with FDSOI. By increasing FBB voltage even further, one might be able to increase the performance at 0.6 V to reach the numbers available at 0.8 V and still keep energy efficiency at 0.3 J/GH.

Contrary to the common belief that FDSOI technology only holds promise in niche low-power applications, the results of the above ASIC chip demonstrate its benefit for mid- and high-performance applications. Any application that is concerned about active power, whether an always-on IoT/wearable or a high performance server/networking chip, should consider the implications of FBB and low voltage operation offered by FDSOI.

## 3 FDSOI technology

FDSOI has become a viable technology thanks to the significant improvements in all fronts, from device performance, SOI substrate uniformity, design ecosystem, and foundry acceptance. In this session we highlight key solutions enabling high volume FDSOI production.

### 3.1 FDSOI substrates

Like other fully depleted transistors, the variation of SOI thickness has an impact on FDSOI device characteristics such as $V_T$. For short channel transistors with $L_G$ around 25 nm, $V_T$ increase is about 25 mV for 1 nm decrease of SOI thickness [33]. The $V_T$ sensitivity drops to about 9 mV/nm for long channel transistors. All major SOI substrate suppliers (Soitec, SEH, and SunEdison) have announced the capability of providing 300 mm FDSOI wafers [21, 73–75] with wafer-to-wafer and within wafer SOI thickness variation less than $\pm 5$ Å, meeting the FDSOI substrate requirement [21]. When back bias is used, it is equally important to control the uniformity of the buried oxide (BOX). Fortunately, BOX is formed by thermal oxidation that is one of the most mature semiconductor processes. Furthermore, the processes and tooling for making FDSOI wafers are fully compatible with the standard CMOS technology. If a chip manufacture wishes to completely secure wafer supply, it has the option to license the SOI wafer technology and insert the processes at the beginning of CMOS flow. Therefore, there is no supply issue in FDSOI substrates.

Higher cost of SOI substrates than bulk Si substrates is another commonly cited reason for rejecting FDSOI technology. Typically the price difference between a 300 mm SOI and bulk Si wafers is about $300 which was significant for old technology nodes with relatively low design and chip manufacturing costs. However, both design and chip manufacturing costs have kept increasing from node to node while the price of Si wafer remains flat or even decreases slightly, the price delta between FDSOI and bulk Si wafers becomes less and less significant as illustrated in Figure 14. The cost increase of design/chip manufacturing comes from the increasing complexity of circuits and patterning. Multiple patterning has become the new norm since 20 nm node for any critical lithography level. FDSOI provides the opportunities for simplifying the manufacturing process and thus reducing manufacturing cost. Fewer

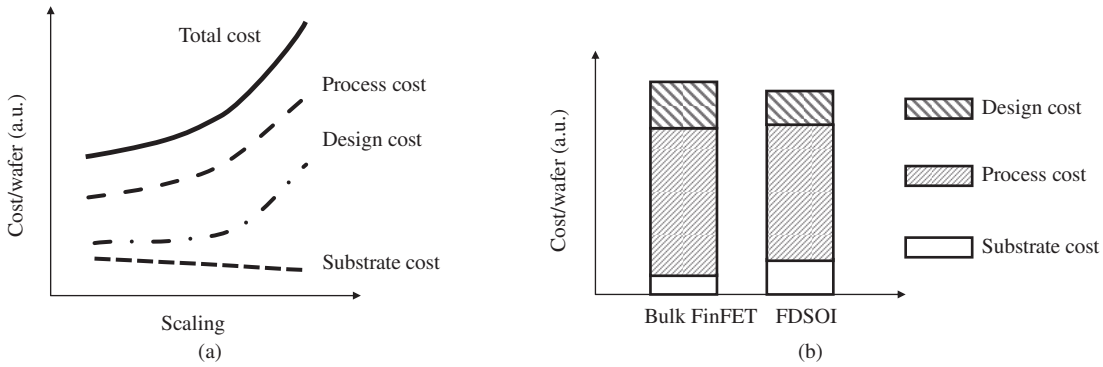


**Figure 14** Schematic showing (a) Process and design costs per wafer increase while substrate cost decreases as technology advances. Substrate cost becomes a small fraction of the total cost of the state-of-the-art technology nodes. (b) Cost comparison of a typical bulk FinFET and FDSOI. FDSOI has higher substrate cost which is offset by the lower process and design costs.

process steps typically lead to higher chip yield. Therefore, the FDSOI device/yield benefits outweigh the SOI wafer cost.

### 3.2 FDSOI manufacturing

Even though the superior electrostatics of FDSOI over bulk MOSFET has long been recognized, the performances of FDSOI had been hindered by high external resistance due to the lack of effective doping technique to form low resistance extensions. The conventional ion implantation tends to amorphize the entire thin SOI layer. Raised source/drain is needed for FDSOI to reduce source/drain and contact resistance. However, it is very challenging to grow high quality epitaxy on heavily implanted thin SOI. This issue has been resolved by an implant-free technique [29]. After forming gate and thin spacers, an in-situ doped epitaxy performed to form raised source/drain (RSD) to reduce S/D resistance. A thermal anneal is performed to drive dopants from RSD to SOI and towards channel. The entire SOI remains single crystalline and low resistance extensions are formed with high active dopant concentrations. It is worth noting that in FDSOI the junction depth is solely determined by the SOI thickness. Diffusing dopants from RSD to form extension does not increase the junction depth and thus good electrostatics is maintained.

A typical system-on-chip (SoC) design requires a variety of devices. While most devices benefit from FDSOI structure, certain devices such as vertical bipolar junction transistors (BJT) and vertical diodes need to be on a bulk silicon substrate. To accommodate this requirement, a hybrid SOI-bulk structure is offered by FDSOI technology as illustrated in Figure 15. The bulk silicon region is obtained by etching away the thin FDSOI and BOX layers and optional epitaxy to eliminate the resulting topography [26,37].

## 4 FDSOI scalability and global landscape

Unfortunately, most of the discussions about the technology scaling simplify the problem to the ability of a given transistor architecture to scale the gate length. This was in fact the focus of many studies in early 2000s to demonstrate aggressively scaled gate length in bulk, FinFET, and nanowire structures. The fact that the gate length scaling is only required to the extent that the transistor gate, contacts and spacers fit the required contacted gate pitch to follow the density requirement, is often overlooked. The sole purpose of technology scaling is to drop the cost per transistor on one hand and to reduce power consumption while maintaining performance (or equally increasing performance while maintaining power) by reducing the total capacitance of the circuit and/or reducing the operating voltage, on the other hand. For highly scaled CMOS transistors, FEOL capacitance is dominated by the parasitic components [43], and scaling of the gate length is not as effective as it used to be in older nodes other than to allow enough space between the gate and contacts.

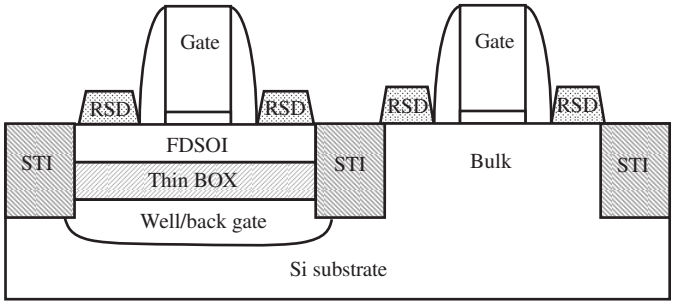


**Figure 15** Schematics showing hybrid integration of FDSOI and bulk devices on the same chip.

**Table 1** FDSOI scaling to 14 nm and 10 nm nodes

| Technology feature | 14FDSOI | 10FDSOI |
|---|---|---|
| Contacted gate pitch (nm) | 90 | 64 |
| Mx pitch (nm) | 64 | 48 |
| Gate length (nm) | 20–24 | 20–24 |
| Self-aligned contact | No | Yes |
| Gate stack | Gate-first high-k/metal gate | Gate first (full metal gate) |
| PFET channel | Strained SiGe (∼25%) | Strained SiGe (∼40%) |
| NFET channel | Relaxed Si | Strained Si |
| SOI thickness (nm) | 5 | 5 |
| BOX thickness (nm) | 20 | 15 |

Table 1 lists the main technology elements of 14 nm FDSOI along with a proposed 10 nm scenario. Gate and metal pitch numbers are based on competitive FinFET technologies [76]. Note that FDSOI technology did not use self-aligned contact (SAC) at 14 nm ground rules. For 10 nm FDSOI, the gate length can remain the same as 14 nm node in view of unlikely scaling of the equivalent oxide thickness (EOT) of the gate dielectric. SAC needs to be adopted in the same manner as that FinFET technology is implemented [57, 58, 76] to accommodate the CPP scaling. Although FDSOI can use the popular replacement metal gate (gate-last) similar to FinFET, we believe a gate-first process with tungsten metal gate [77] with an insulator cap is easier to implement. FDSOI channel thickness can be kept around 5 nm because the gate length remains the same. The BOX thickness can be reduced to 10–15 nm to take greater advantage of back biasing,

One of the main criticism to the FDSOI technology has been that it is a one-node solution and is not scalable to the future. This was based on the "gate-length-scaling" assumptions of early 2000s, which do not capture the past and current trends of CMOS technology. As we discussed earlier, a 28 nm FDSOI technology has been already developed and multiple complex circuits demonstrated the advantage of the technology over 28 nm bulk CMOS. A 14 nm technology is under R&D with the elements shown in Table 1. As argued above, the technology is scalable to 10 nm. Strain engineering elements have been already demonstrated, while self-aligned contacts, both to active and gate regions, are still needed. Alternatively, one can conceive a possible 22 nm implementation with the performance elements of the 14 nm, while keeping metal pitch above 80 nm to avoid need to double patterning and reduce cost. This is in fact what IBM-ST-Leti had used as the test vehicle for the majority of the technology development that led to the 14 nm FDSOI technology and interestingly very much what GLOBALFOUNDRIES announced as their 22FDX platform. The above example is a good instance of FDSOI as a "multi-node platform" technology. The planar nature of FDSOI allows the FEOL to be independent of the BEOL. In the above example, the same FEOL elements were initially developed with a single-patterning BEOL test chip, then transferred to a double-patterning BEOL technology, and finally transferred back to a single-patterning technology, while keeping FEOL almost unchanged throughout this process (with the exception of slight change in gate pitch). This is a very important concept and has been practiced multiple times in the

past CMOS technologies whenever a "shrink node" was developed. What was done here, however, is somewhat in the opposite direction; placing a "better MOSFET" at an older node than it was initially intended for, to take advantage of a depreciated foundry process (Fab 1 in Dresden in this example).

One might argue why the same concept cannot be used with FinFET. Assuming that the FinFET cost-adder is only 2–3% (at 22 nm), and it delivers 50% or more active power reduction, why none of major foundries offer a FinFET technology with 28 nm ground rules? This would be a much better alternative than various 28 nm versions that TSMC is advertising. Cost argument aside, there is a technical problem: FEOL and BEOL are linked together through the choice of fin and metal pitch. Taking the case of TSMC's 16 nm technology as an example and assuming that with a 64 nm metal pitch the optimum fin pitch is 48 nm, at 28 nm ground rules the optimum fin pitch would be 60 nm or more (This actually coincides with what Intel used in their 22 nm node). As a consequence, the higher drive current per footprint that is advertised as one of the major benefits of FinFET diminishes if it is placed at older node unless the fins are made proportionally taller. Manufacturing complexity aside, FEOL capacitance grows in proportion, which defeats any advantage.

A natural extension of the above concept is to insert a reduced cost version of FDSOI at even more mature technology nodes. There are many products that do not benefit from the most advanced nodes because they are dominated by analog, passives, or need elements that are not available in leading edge technologies yet, such as embedded non-volatile memory (eNVM). With the coming wave of IoT applications that require such elements and typically need a small die size, there is growing interest in more mature technologies. Recent announcements of older nodes with process tweaked to offer an ultra-low-power (ULP) or ultra-low-leakage (ULL) technology is a testimony to the need for a better transistor architecture even at older nodes. FDSOI's main propositions, i.e., the record low local transistor mismatch, the ability to compensate for global variation with a body bias, and the ability to reduce threshold voltage, together allow record low operating voltage, rendering FDSOI a perfect device architecture to reduce active power. In the meantime, the ability to modulate the transistor $V_T$ enables a chip to deliver the target performance by lowering $V_T$ and then increase it to suppress leakage when the chip goes into standby.

In fact, several groups are actively pursuing implementations at larger dimensions. A low-cost implementation at 65 nm has been already demonstrated and is ready for foundry offering [78]. One can imagine a process shrink of this technology to 55 nm or 45/40 nm to further reduce the die cost. It is expected that these implementations open new possibilities in ultra-low voltage operation, which is essential for future internet-of-things (IoT) applications.

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**Conflict of interest** The authors declare that they have no conflict of interest.

## References

1 Semiconductor Industry Association Global Sales Report. http://www.semiconductors.org/industry_statistics/global_sales_report/
2 Moore G E. Cramming more components onto integrated circuits. Electronics, 1965, 38: 82–85
3 Auth C, Allen C, Blattner A, et al. A 22nm high performance and low-power CMOS technology featuring fully-depleted tri-gate transistors, self-aligned contacts and high density MIM capacitors. In: Proceedings of VLSI 2012 Symposium on Technology (VLSIT), Honolulu, 2012. 131–132
4 Dennard R H, Gaensslen F H, Rideout V L, et al. Design of ion-implanted MOSFET's with very small physical dimensions. IEEE J Solid-State Circuits, 1974, 9: 256–268
5 Wann H, Ko P K, Hu C. Gate-induced band-to-band tunneling leakage current in LDD MOSFETs. In: Technical Digest of International Electron Devices Meeting, San Francisco, 1992. 147–150
6 Bhavnagarwala A, Kosonocky S, Radens C, et al. Fluctuation limits & scaling opportunities for CMOS SRAM cells. In: Technical Digest of International Electron Devices Meeting, Washington DC, 2005. 659–662
7 Choi Y-K, Asano K, Lindert N, et al. Ultra-thin body SOI MOSFET for deep-sub-tenth micron era. IEEE Electron Dev Lett, 1999, 21: 254–255

8 Noel J-P, Thomas O, Jaud M-A, et al. UTB-FDSOI device architecture dedicated to low power design techniques. In: Proceedings of the European Solid-State Device Research Conference (ESSDERC), Sevilla, 2010. 210–213
9 Tsutsui G, Saitoh M, Hiramoto T. Experimental study on superior mobility in (110)-oriented UTB SOI pMOSFETs. IEEE Electron Dev Lett, 2005, 26: 836–838
10 Skotnicki T, Hutchby J A, King T-J, et al. The end of CMOS scaling: toward the introduction of new materials and structural changes to improve MOSFET performance. IEEE Circuits Dev Mag, 2006, 21: 16–26
11 Kilchytska V, Md Arshad M K, Makovejev S, et al. Ultra-thin body and thin-BOX SOI CMOS technology analog figures of merit. Solid-State Electron, 2012, 70: 50–58
12 Fenouillet-Beranger C, Denormel S, Icard B, et al. Fully-depleted SOI technology using high-K and single-metal gate for 32nm node LSTP applications featuring 0.179μm$^2$ 6T-SRAM bitcell. In: Technical Digest of International Electron Devices Meeting, Washington DC, 2007. 267–270
13 Skotnicki T. Competitive SOC with UTBB SOI. In: Proceedings of 2011 IEEE International SOI Conference (SOI), Tempe, 2011. 1–61
14 Liu Q, Yagashita A, Loubet N, et al. Ultra-thin-body and BOX (UTBB) fully depleted (FD) device integration for 22nm node and beyond. In: Proceedings of 2010 Symposium on VLSI Technology (VLSIT), Honolulu, 2010. 61–62
15 Grenouillet L, Vinet M, Gimbert J, et al. UTBB FDSOI transistors with dual STI and shrinked back gate architecture for a multi-$V_T$ strategy at 20nm node and below. In: Technical Digest of International Electron Devices Meeting, San Francisco, 2012. 64–67
16 Andrieu F, Weber O, Mazurier J, et al. Low leakage and low variability ultra-thin body and buried oxide (UT2B) SOI technology for 20nm low power CMOS and beyond. In: Proceedings of 2010 Symposium on VLSI Technology (VLSIT), Honolulu, 2010. 57–58
17 Numata T, Noguchi M, Oowaki Y, et al. Back gate engineering for suppression of threshold voltage fluctuation in fully-depleted SOI MOSFETs. In: Proceedings of 2000 IEEE International SOI Conference, Wakefield, 2000. 78–79
18 Sugii N, Tsuchiya R, Ishigaki T, et al. Comprehensive study on Vth variability in silicon on thin BOX (SOTB) CMOS with small random-dopant fluctuation: finding a way to further reduce variation. In: Proceedings of 2008 International Electron Devices Meeting, San Francisco, 2008. 1–4
19 Sugii N, Tsuchiya R, Ishigaki T, et al. Local $V_{th}$ variability and scalability in silicon-on-thin-BOX (SOTB) CMOS with small random-dopant fluctuation. IEEE Trans Electron Dev, 2010, 57: 835–845
20 Doris B, Ieong M, Zhu T, et al. Device design considerations for ultra-thin SOI MOSFETs. In: Technical Digest of International Electron Devices Meeting, Washington DC, 2003. 27.3.1–27.3.4
21 Schwarzenbach W, Cauchy X, Boedt F, et al. Excellent silicon thickness uniformity on ultra-thin SOI for controlling $V_T$ variation of FDSOI. In: Proceedings of IEEE International Conference on IC Design and Technology, Kao-hsiung, 2011. 1–3
22 Nayfeh H M, Singh D V, Hergenrother J M, et al. Effect of tensile uniaxial stress on the electron transport properties of deeply scaled FD-SOI n-Type MOSFETs. IEEE Electron Dev Lett, 2006, 27: 288–290
23 Barral V, Poiroux T, Andrieu F, et al. Strained FDSOI CMOS technology scalability down to 2.5nm film thickness and 18nm gate length with a TiN/$HfO_2$ gate stack. In: Technical Digest of International Electron Devices Meeting, Washington DC, 2007. 61–64
24 Uchida K, Watanabe H, Kinoshita A, et al. Experimental study on carrier transport mechanism in ultrathin-body SOI n- and p-MOSFETs with SOI thickness less than 5 nm. In: Technical Digest of International Electron Devices Meeting, San Francisco, 2002. 47–50
25 Faynot O, Andrieu F, Weber O, et al. Planar fully depleted SOI technology: a powerful architecture for the 20nm node and beyond. In: Technical Digest of International Electron Devices Meeting, San Francisco, 2010. 50–53
26 Fenouillet-Beranger C, Perreau P, Pham-Nguyen L, et al. Hybrid FDSOI/Bulk high-k/Metal gate platform for Low Power (LP) multimedia technology. In: Technical Digest of International Electron Devices Meeting, Baltimore, 2009. 1–4
27 Majumdar A, Wang X, Kumar A, et al. Gate length and performance scaling of undoped-body extremely thin SOI MOSFETs. IEEE Electron Dev Lett, 2009, 30: 413–415
28 Majumdar A, Ren Z, Koester S J, et al. Undoped-body extremely thin SOI MOSFETs with back gates. IEEE Trans Electron Dev, 2009, 56: 2270–2276
29 Cheng K, Khakifirooz A, Kulkarni P, et al. Fully depleted extremely thin SOI technology fabricated by a novel integration scheme featuring implant-free, zero-silicon-loss, and faceted raised source/drain. In: Proceedings of 2009 Symposium on VLSI Technology (VLSIT), Honolulu, 2009. 212–213
30 Khakifirooz A, Cheng K, Nagumo T, et al. Strain engineered extremely thin SOI (ETSOI) for high-performance CMOS. In: Proceedings of 2012 Symposium on VLSI Technology (VLSIT), Honolulu, 2012. 117–118
31 Cheng K, Khakifirooz A, Kulkarni P, et al. Extremely thin SOI (ETSOI) CMOS with record low variability for low power system-on-chip applications. In: Proceedings of 2009 IEEE International Electron Devices Meeting (IEDM), Baltimore, 2009. 49–52
32 Cheng K, Khakifirooz A, Loubet N, et al. High performance extremely thin SOI (ETSOI) hybrid CMOS with Si channel NFET and strained sige channel PFET. In: Technical Digest of International Electron Devices Meeting, San Francisco, 2012. 18.1.1–18.4
33 Khakifirooz A, Cheng K, Kulkarni P, et al. Challenges and opportunities of extremely thin SOI (ETSOI) CMOS technology for future low power and general purpose system-on-chip applications. In: Proceedings of International Symposium on VLSI Technology Systems and Applications (VLSI-TSA), Hsinchu, 2010. 110–111

34 Ponoth S, Vinet M, Grenouillet L, et al. Implant approaches and challenges for 20nm node and beyond ETSOI devices. In: Proceedings of 2011 IEEE International SOI Conference, Tempe, 2011. 1–2

35 Chau R, Kavalieros J, Doyle B, et al. A 50nm depleted-substrate CMOS Transistor (DST). In: Technical Digest of International Electron Devices Meeting, Washington DC, 2001. 29.1.1–29.1.4

36 Krivokapic Z, Maszara W, Arasnia F, et al. High performance 25nm FDSOI devices with extremely thin silicon channel. In: Proceedings of 2003 Symposium on VLSI Technology (VLSIT), Kyoto, 2003, 131–132

37 Chen H, Chang C, Huang C, et al. Novel 20nm hybrid SOI/bulk CMOS technology with 0.183μm$^2$ 6T-SRAM cell by immersion lithography. In: Proceedings of 2005 Symposium on VLSI Technology (VLSIT), Kyoto, 2005. 16–17

38 Fenouillet C, Perreau P, Denorme S, et al. Impact of a 10 nm ultrathin BOX (UTBOX) and ground plane on FDSOI devices for 32 nm node and below. In: Proceedings of the European Solid-State Device Research Conference (ESSDERC), Athens, 2009. 89–91

39 Fenouillet C, Thomas O, Perreau P, et al. Efficient multi-$V_T$ FDSOI technology with UTBOX for low power circuit design. In: Proceedings of 2010 Symposium on VLSI Technology (VLSIT), Honolulu, 2010. 65–66

40 Skotnicki T, Fenouillet-Beranger C, Gallon C, et al. Innovative materials, devices, and CMOS technologies for low-power mobile multimedia. IEEE Trans Electron Dev, 2008, 55: 96–130

41 Leobandung E, Barth E, Sherony M, et al. High performance 0.18 pm SOI CMOS technology. In: Technical Digest of International Electron Devices Meeting, Washington DC, 1999. 679–682

42 Puri R, Chuang C T. Hysteresis effect in pass-transistor based partially-depleted SOI CMOS circuits. In: Proceedings of 1998 IEEE International SOI Conference, Stuart, 1998. 103–104

43 Skotnicki T, Fenouillet-Beranger C, Gallon C, et al. Innovative materials, devices, and CMOS technologies for low-power mobile multimedia. IEEE Trans Electron Dev, 2008, 55: 96–130

44 Khakifirooz A, Antoniadis D A. MOSFET performance scaling—Part 1: historical trends. IEEE Trans Electron Dev, 2008, 55: 1391–1400

45 Pelgrom M. Matching properties of MOS transistors. IEEE J Solid-State Circuits, 1989, 24: 1433–1439

46 Cheng K, Khakifirooz A. FDSOI technology and its implications to analog and digital design. In: Jiang X C, ed. Digitally-Assisted Analog and Analog-Assisted Digital IC Design. Cambridge: Cambridge University Press, 2015. 86

47 Kuhn K J. Considerations for ultimate CMOS scaling. IEEE Trans Electron Dev, 2012, 59: 1813–1828

48 Yamamoto Y, Makiyama H, Shinohara H, et al. Ultralow-voltage operation of Silicon-on-Thin-BOX (SOTB) 2Mbit SRAM down to 0.37 V utilizing adaptive back bias. In: Proceedings of 2013 Symposium on VLSI Technology (VLSIT), Kyoto, 2013. T212–T213

49 Khakifirooz A, Cheng K, Jagannathan B, et al. Fully depleted extremely thin SOI for mainstream 20nm low-power technology and beyond. In: 2010 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC), San Francisco, 2010. 152–153

50 Ghani T, Armstrong M, Auth C, et al. A 90nm high volume manufacturing logic technology featuring novel 45nm gate length strained silicon CMOS transistors. In: Technical Digest of International Electron Devices Meeting, Washington DC, 2003. 11.6.1–11.6.3

51 Lee W-H, Waite A, Nii H, et al. High performance 32nm SOI CMOS with high-k/metal gate and 0.149μm$^2$ SRAM and ultra low-k back end with eleven levels of copper. In: Technical Digest of International Electron Devices Meeting, Washington DC, 2005. 56–59

52 Narasimha S, Chang P, Ortolland C, et al. 22nm high-performance SOI technology featuring dual-embedded stressors, epi-plate high-k deep-trench embedded DRAM and self-aligned via 15LM BEOL. In: Technical Digest of International Electron Devices Meeting, San Francisco, 2012. 3.3.1–3.3.4

53 Leobandung E, Nayakama H, Mocuta D, et al. High performance 65 nm SOI technology with dual stress line and low capacitance SRAM cell. In: 2005 Symposium on VLSI Technology, Digest of Technical Papers, Kyoto, 2005. 126–127

54 Ota K, Sugihara K, Sayama H, et al. Novel locally strained channel technique for high performance 55 nm CMOS. In: Proceedings of International Electron Devices Meeting, San Francisco, 2002, 27–30

55 Lim K-Y, Lee H, Ryu C, et al. Novel stress-memorization-technology (SMT) for high electron mobility enhancement of gate last high-k/metal gate devices. In: Proceedings of International Electron Devices Meeting, San Francisco, 2010. 10.1.1–10.1.4

56 Jan C-H, Bhattacharya U, Brain R, et al. A 22nm SoC platform technology featuring 3-D tri-gate and high-k/metal gate, optimized for ultra low power, high performance and high density SoC applications. In: Proceedings of International Electron Devices Meeting, San Francisco, 2012. 3.1.1–3.1.4

57 Natarajan S, Agostinelli M, Akbar S, et al. A 14nm logic technology featuring 2nd-generation FinFET, air-gapped interconnects, self-aligned double patterning and a 0.0588μm$^2$ SRAM cell size. In: Proceedings of International Electron Devices Meeting, San Francisco, 2014. 3.7.1–3.7.3

58 Jan C-H, Al-amoody F, Chang H-Y, et al. A 14 nm SoC platform technology featuring 2nd generation tri-gate transistors, 70 nm gate pitch, 52 nm metal pitch, and 0.0499 um$^2$ SRAM cells, optimized for low power, high performance and high density SoC products. In: Proceedings of 2015 Symposium on VLSI Technology, Kyoto, 2015. T12–T13

59 Liu Q, DeSalvo B, Morin P, et al. FDSOI CMOS devices featuring dual strained channel and thin BOX extendable to the 10nm node. In: Proceedings of International Electron Devices Meeting, San Francisco, 2014. 9.1.1—9.1.4

60 Kube M, Hori R, Minato O, et al. A threshold voltage controlling circuit for short channel MOS integrated circuits. In: Technical Digest of 1976 IEEE International Solid-State Circuits Conference, Philadelphia, 1976. 54–55

61 Thompson S, Young I, Greason J, et al. Dual threshold voltage and substrate bias: Keys to high performance, low power, 0.1 μm logic designs. In: 1997 Symposium on VLSI Technology, Digest of Technical Papers, Kyoto, 1997. 69–70

62 Nomura S, Tachibana F, Fujita T, et al. A 9.7mW AAC-decoding, 620mW H.264 720p 60fps decoding, 8-core media processor with embedded forward-body-biasing and power-gating circuit in 65nm CMOS technology. In: IEEE International Solid-State Circuits Conference, Digest of Technical Papers, San Francisco, 2008. 262–612

63 Sumita M, Sakiyama S, Kinoshita M, et al. Mixed body-bias technique with fixed $V_t$ and $I_{\rm ds}$ generation circuits. IEEE J Solid-State Circuits, 2005, 40: 60–66

64 Jacquet D, Hasbani F, Flatresse P, et al. A 3 GHz dual core processor ARM Cortex$^{TM}$-A9 in 28 nm UTBB FD-SOI CMOS with ultra-wide voltage range and energy efficiency optimization. IEEE J Solid-State Circuits, 2014, 49: 812–826

65 Wilson R, Beigne E, Flatresse P, et al. A 460MHz at 397mV, 2.6GHz at 1.3V, 32b VLIW DSP, Embedding FMAX Tracking. In: 2014 IEEE International Solid-State Circuits Conference, Digest of Technical Papers, San Francisco, 2014. 452–453

66 Ishibashi K, Sugii N, Usami K, et al. A perpetuum mobile 32bit CPU with 13.4pJ/cycle, 0.14μA sleep current using reverse body bias assisted 65nm SOTB CMOS technology. In: 2014 IEEE COOL Chips XVII, Yokohama, 2014. 1–3

67 Beigne E, Valentian A, Miro-Panades I, et al. A 460MHz at 397mV, 2.6GHz at 1.3V, 32 bits VLIW DSP embedding $F_{max}$ tracking. IEEE J Solid-State Circuits, 2015, 50: 125–136

68 Clerc S, Saligane M, Abouzeid F, et al. A 0.33V/−40°C process/temperature closed-loop compensation SoC embedding all-digital clock multiplier and DC-DC converter exploiting FDSOI 28nm back-gate biasing. In: Proceedings of 2015 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, 2015. 1–3

69 SFARDS. SFARDS new 28nm BTC & LTC dual-algorithm ASIC unveiled. http://www.sfards.com/detail?id=26

70 Bitcoin Wiki. ASIC. https://en.bitcoin.it/wiki/ASIC

71 Miyazaki M, Kao J, Chandrakasan A P. A 175mV multiply-accumulate unit using an adaptive supply voltage and body bias (ASB) architecture. In: 2002 IEEE International Solid-State Circuits Conference, Digest of Technical Papers, San Francisco, 2002

72 Keshavarizi A, Narendra S, Bloechel B, et al. Forward body bias for microprocessors in 130nm technology generation and beyond. IEEE J Solid-State Circuits, 2003, 38: 696–701

73 Soitec. Press release "Soitec and Shin-Etsu Handotai announce Smart Cut$^{\rm TM}$ licensing extension and expanded technology cooperation". 2012. http://www.soitec.com/en/news/press-releases/soitec-and-shin-etsu-handotai-announce-smart-cut-licensing-extension-and-expanded-technology-cooperation-1079/

74 Shin-Etsu Handotai Co., Ltd. Ultra Thin Body and Buried oxide substrate supply chain. FD-SOI Workshop, Kyoto, 2013. http://www.soiconsortium.org/fully-depleted-soi/presentations/june-2013/Nobuhiko%20Noto%20-%20UTBB-%20Wafer_SEH_June2013.pdf

75 Soitec. Press release "Soitec and SunEdison enter into patent license agreement". 2013. http://www.soitec.com/en-/news/press-releases/soitec-and-sunedison-enter-into-patent-license-agreement-1390/

76 Seo K-I, Haran B, Gupta D, et al. A 10nm platform technology for low power and high performance application featuring FINFET devices with multi workfunction gate stack on bulk and SOI. In: 2014 Symposium on VLSI Technology: Digest of Technical Papers, Honolulu, 2014. 1–2

77 Seo S-C, Edge L F, Kanakasabapathy S, et al. Full metal gate with borderless contact for 14 nm and beyond. In: Proceedings of 2011 Symposium on VLSI Technology (VLSIT), Honolulu, 2011. 36–37

78 Kamohara S, Sugii N, Yamamoto Y, et al. Ultralow-voltage design and technology of silicon-on-thin-buried-oxide (SOTB) CMOS for highly energy efficient electronics in IoT era. In: 2014 Symposium on VLSI Technology: Digest of Technical Papers, Honolulu, 2014. 1–2