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Single event upset induced by single event double transient and its well-structure dependency in 65-nm bulk CMOS technology

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Abstract Single event upset (SEU) is one of the most important origins of soft errors in aerospace applications. As technology scales down persistently, charge sharing is playing a more and more significant effect on SEU of flip-flop. Charge sharing can often bring about multi-node charge collection in storage nodes and non-storage nodes in a flip-flop. In this paper, multi-node charge collection in flip-flop data input and flip-flop clock signal is investigated by 3D TCAD mixed-mode simulations, and the simulate results indicate that single event double transient (SEDT) in flip-flop data input and flip-flop clock signal can also cause a SEU in flip-flop. This novel mechanism is called the SEDT-induced SEU, and it is also verified by heavy-ion experiment in 65 nm twin-well process. The simulation results also indicate that this mechanism is closely related with the well-structure, and the triple-well structure is more effective to increase the SEU threshold of this mechanism than twin-well structure.

Keywords single event upset (SEU), single event double transient (SEDT), SEDT-induced SEU, parasitic bipolar effect (PBE), charge sharing

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1 Introduction

Single event effects (SEE) are becoming a primary origin of soft errors in analog circuits, mixed-signal circuits, and integrated circuits (ICs) [1,2] especially in aerospace applications. Charge sharing is playing a more and more significant role in SEE with technology scaling down [3–7], for the multi-node charge collection [8] by charge sharing can often impact several devices in ICs and then reduce the gain of those hardening techniques.

In sequential logic, the threat of charge sharing is becoming more and more outstanding. As technology progresses, some redundancy designs become sensitive, the single event upset (SEU) mitigation of DICE flip-flop decreases greatly compared with D flip-flop [9]. The difference between D and DICE flip-flop error rates decreases to about 30%–50% in 40 nm technology [10].

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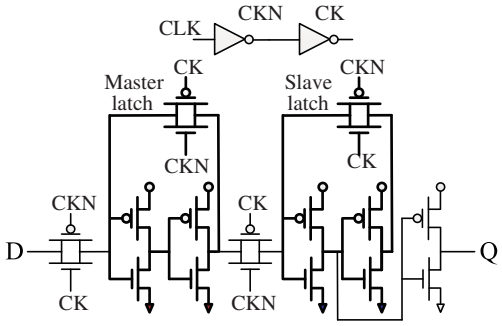

Figure 1 The circuit diagram of a master-slave D flip-flop (DFF) consisting of transmission gates and cross-coupled storage nodes.

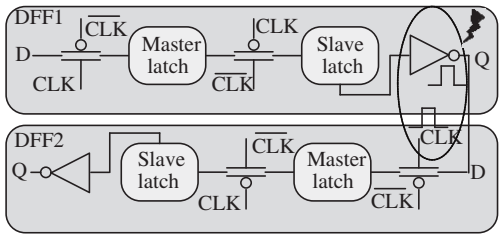

Figure 2 The sketch map for the generation of single event double transient (SEDT) in flip-flop data input and flip-flop clock signal.

As shown in Figure 1, a master-slave D flip-flop (DFF) consists of transmission gates and cross-coupled storage nodes. Except for direct upset at storage nodes (direct upset, for short) of this flip-flop, there are also indirect upset, that is, SEU can be caused by single event transient (SET) in non-storage nodes of a flip-flop [11–14]. The SET in transmission gate [11] and SET in clock signal [14] is also a possible cause of SEU. What is more, in nanometer technology, multi-node charge collection may occur in flip-flop data input circuit and clock signal of a flip-flop simultaneously, and then bring about two single event transients (SET) in flip-flop data input circuit and clock signal simultaneously. If these two SETs are large enough, the SET in flip-flop data input circuit may be latched by SET in flip-flop clock signal, and then an SEU occurs.

In this paper, SEU induced by multi-node charge collection in flip-flop data input circuit and flip-flop clock signal is simulated, and its well-structure dependency is investigated as well. The results indicate that the triple-well structure is beneficial for mitigating this upset mechanism.

2 SEDT-induced SEU mechanism

For the master-slave D flip-flop, when the master latch is in hold mode, the slave latch is in updating mode. While ion striking at the latch in hold mode with ion energy being large enough, direct upset will occur. Similarly, ion striking at other gates, for example, the latch in updating mode, may bring about indirect upset if a clock signal comes into being. In low-frequency applications, the SET in data input is hard to be captured by the clock signal. However, charge sharing [3,15] can lead to single event multiple transient (SEMT) [7,16] in nanometer CMOS technology. As shown in Figure 2, if a SET is generated in flip-flop data input nodes with a SET generated in the clock signal simultaneously, the SET in flip-flop data input may be latched into flip-flop by the SET in flip-flop clock signal. Because these two SETs are caused by one single events (SEs), it can be called as single event double transient (SEDT), and SEU induced by it can be called as SEDT-induced SEU.

3 Simulation setup

The simulated TCAD devices are calibrated to a commercial 65 nm bulk process. Its gate length is 60 nm, the widths of NMOS and PMOS are 300 nm and 450 nm respectively, and the well contact width is 160 nm. As shown in Figure 3, two PMOS transistors are built into TCAD devices, while others are configured with default SPICE models. One PMOS transistor is that in an inverter in data input of a DFF, while another is that in an inverter in clock circuit of this DFF. Then, 3D mixed-mode TCAD simulations were carried out.

As the same with our previous work [17,18], heavy ion strike is simulated with a Gaussian electron-hole pair column, and the included physical modes are the same with that in our previous work [4,18]. The

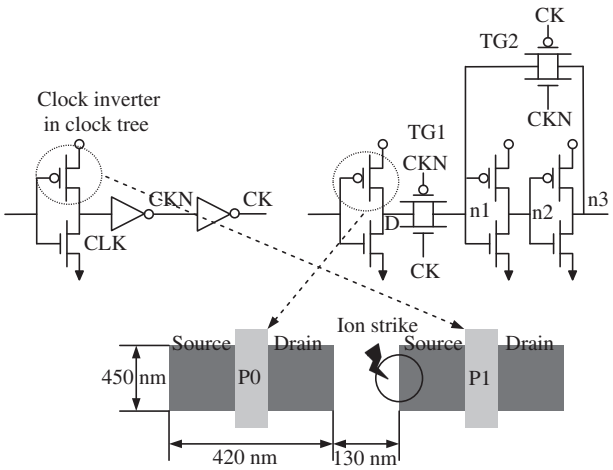

Figure 3 The TCAD simulation setup: a PMOS in clock inverter in clock circuit and a PMOS in data input of D flip-flop are built into TCAD devices, while others are configured with default SPICE models.

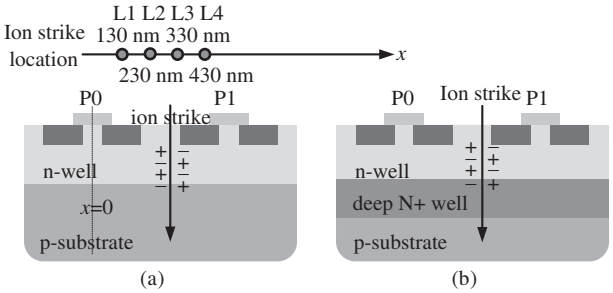

Figure 4 The side view of two PMOS transistors in TCAD. (a) Twin-well structure, (b) triple-well structure.

linear energy transfer (LET) value remains constant along the ion track. The length and character radius of the ion track is 5 μm and 50 nm respectively. As shown in Figure 4, the gate center of P0 is the origin (i.e. x=0), and four ion strike locations are selected, i.e. 'x=130, 230, 330 and 430 nm'. Besides, 'x=330 nm' is selected as the typical ion strike location, for it is almost the midpoint between drain centers of P0 and P1, and then charge sharing is easier to be observed. In this work, twin-well and triple-well structure are simulated, and the effect of N+ deep well on SEDT-induced SEU is studied with normal heavy-ion strike.

4 Simulation results and analysis

4.1 SEDT and SEDT-induced SEU

With ion striking at location L3 in twin-well structure (i.e. x=330 nm) with the LET of 16 MeV $\cdot$ cm$^2\cdot$ mg^{-1}, the single event double transients (SEDT) in D and CLK is shown in Figure 5. The SET in CLK can open the transmission gate TG1 momently, and then the node capacitor of n1 will neutralize the node capacitor of D, so that a downward glitch occurs at the SET in D. Certainly, only if the amplitude of SET in D is large enough, the node status of n1 and n2 can be upset.

However, not all SEDT in data input and clock circuit can cause an SEU in D flip-flop. As shown in Figure 6, with ion striking at location L3 with the LET of 15 MeV $\cdot$ cm^2 $\cdot$ mg^{-1}, there still exist SETs in D and CLK, though the SET in D has not been latched by the SET in CLK. In reality, with the LET decreasing, the SET amplitude in D is reduced, for the charge collection in D is reduced while the node capacitor of n1 is the same. When the amplitude of SET in D is smaller than a threshold, it cannot change the node status of n1 even if the transmission gate TG1 is opened momently.

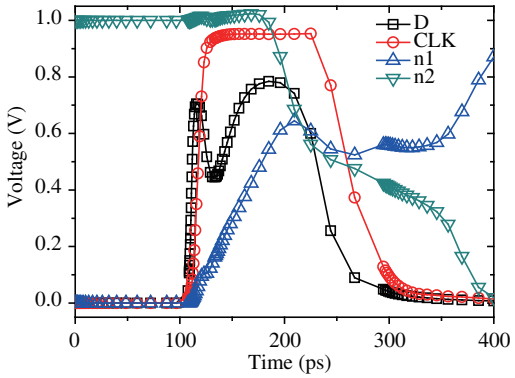

Figure 5 (Color online) Illustration of the SEDT in nodes D and CLK, and SEDT-induced SEU in twin-well DFF with ion strike at L3 with the LET of 16 MeV $\cdot$ cm^2 $\cdot$ mg^{-1}.

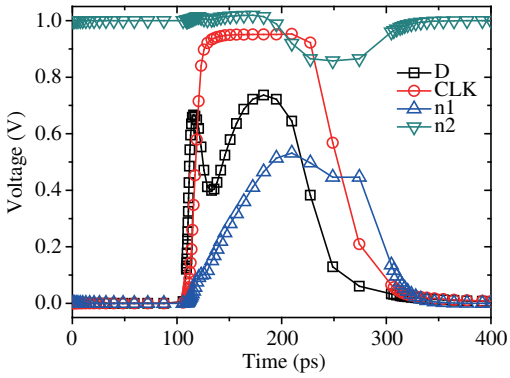

Figure 6 (Color online) Illustration of the SEDT in nodes D and CLK in twin-well DFF, with ion strike at L3 with the LET of 15 MeV $\cdot$ cm^2 $\cdot$ mg^{-1}.

Table 1 The SEDT-induced SEU threshold for D flip-flop in twin-well and triple-well process with ion strike location varies

The ion strike location	Upset threshold in twin-well structure (MeV $\cdot$ cm^2 $\cdot$ mg^{-1})	Upset threshold in triple-well structure (MeV $\cdot$ cm^2 $\cdot$ mg^{-1})
L1	18	70
L2	15	40
L3	16	28
L4	20	52

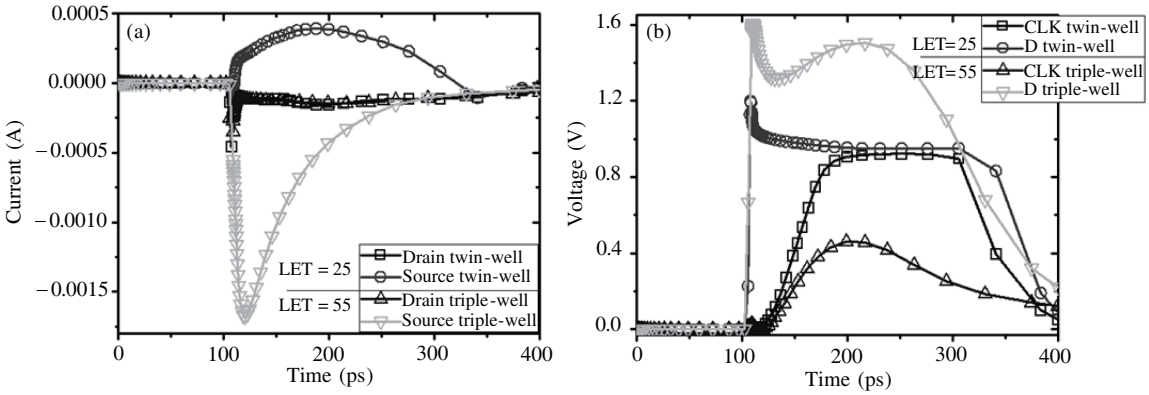

Figure 7 With ion striking at L1 with the LET of 25 and 55 MeV $\cdot$ cm^2 $\cdot$ mg^{-1} in twin-well and triple-well structure respectively. (a) The current transient in drain and source of P0, (b) the voltage transient in D and CLK.

4.2 The well-structure dependency of SEDT-induced SEU

As stated in the last section, SEDT-induced SEU can be observed if the ion LET is over the threshold. As shown in Table 1, as ion strike location changes, SEDT-induced SEU threshold for a flip-flop varies as well. When the ion strike location is between the drain center of P0 and P1, charge sharing between P0 and P1 is enhanced, and then the upset threshold is decreased, for example, ion strike location L2 and L3.

The SEU threshold variation with ion strike location is similar for triple-well process. Nevertheless, the SEU threshold increases greatly compared to that in twin-well process. As shown in Figure 7(a), in twin-well structure, the source current direction is opposite to the drain current direction, that is, the parasitic bipolar effect (PBE) exists. However, in triple-well structure, the source current direction is the same with the drain current direction, that is, no PBE occurs. PBE often has a significant effect on charge sharing, and it can enhance charge sharing in twin-well structure greatly. As shown in Figure 7(b),

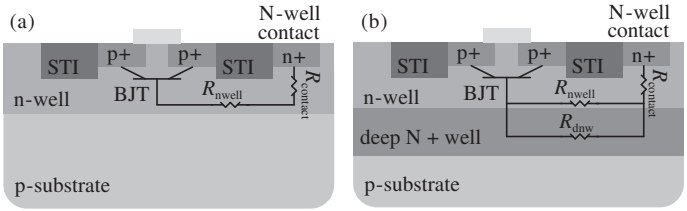

Figure 8 (a) The charge removal path in twin-well process consists of horizontal resistance ($R_{\rm nwell}$) and vertical resistance ($R_{\rm contact}$), (b) the charge removal path in triple-well process consists of horizontal resistance ($R_{\rm nwell}$ and $R_{\rm dnw}$) and vertical resistance ($R_{\rm contact}$).

Table 2 The SEDT-induced SEU threshold for D flip-flop in twin-well and triple-well process with ion strike location L3, while changing the well contact size

The width of well contact (nm)	Upset threshold in Twin-well process ($\rm MeV \cdot cm^2 \cdot mg^{-1}$)	Upset threshold in Triple-well process ($\rm MeV \cdot cm^2 \cdot mg^{-1}$)
100	14	27.9
160	16	28.0
220	19	28.1

in twin-well structure, with ion striking at L1 with LET of 25 $\rm MeV \cdot cm^2 \cdot mg^{-1}$, charge sharing between P0 and P1 is strong, and then the SET in D and CLK is large enough to cause an upset in DFF. However, in triple-well structure, the deep N+ well (DNW) layer [6, 19–21] can mitigate PBE effectively, so that charge sharing in n-well is mitigated greatly as well. As shown in Figure 7(b), for the same ion strike location, even the LET is 55 $\rm MeV \cdot cm^2 \cdot mg^{-1}$, the amplitude of the SET in CLK is not over 0.5 V, and then no SEU occurs.

As viewed from charge removal, PBE is dependent on how quickly the deposited charge by a single event (SE) can be removed from n-well. Slower charge removal will make more excess charge be left in n-well and then lead to a slower well potential recovery and enhanced PBE. As shown in Figure 8, there exists an additional horizontal charge removal path (i.e. Rdnw) in triple-well structure. Thus, the charge removal in triple-well structure is quicker than that in twin-well structure, and then the well potential recovery is more quickly in triple-well structure as well.

4.3 The effect of well contact size

As known to all, well contact size has a significant effect on the PBE in n-well generally by changing the well potential modulation [22–24]. Thus, the width of n-well contact is changed from 100 nm to 220 nm with the step of 60 nm, and its effect on SEDT-induced upset is simulated. The results are shown in Table 2.

With well contact size increasing, SEDT-induced SEU threshold increases either for twin-well process or for triple-well process. After the parasitic structure shown in Figure 8, $R_{\rm contact}$ decreases with well contact size increasing, thus the well potential modulation is enhanced, and then PBE is weakened. However, for triple-well process, the horizontal resistance $R_{\rm nwell}//R_{\rm dnw}$ is far less than $R_{\rm nwell}$ in twin-well, the effect of reducing $R_{\rm contact}$ is less, so that the increase is more apparent in twin-well process.

As a result, increasing well contact size can mitigate SEDT-induced SEU in twin-well DFF though it only has a slight effect on mitigating SEDT-induced SEU in triple-well DFF. However, we can also see that SEDT-induced SEU threshold in twin-well is still less than that in triple-well process even if the width of well contact is increased over 2 times (220 nm/100 nm). Hence, to mitigate SEDT-induced SEU, increasing well contact size in twin-well may be not as good as using triple-well structure. In reality, triple-well will increase the single event (SE) sensitivity of NMOS [18,19], but the selectively implanted Deep N+ well (SIDNW) structure [18] proposed by our group is a good improvement of triple-well structure for it will not increase the SE sensitivity of NMOS, and then NMOS is not simulated herein.

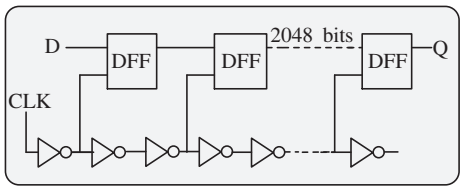

Figure 9 Schematic diagram of a master-slave DFF chain in the test chip.

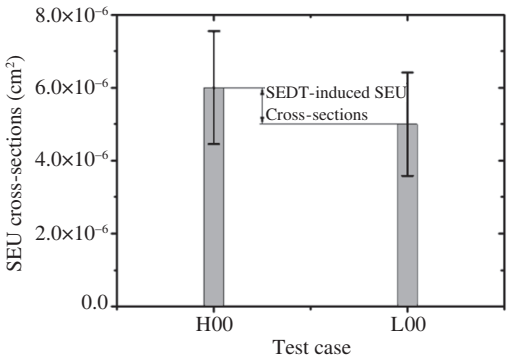

Figure 10 The experiment results from Kr ion (the LET is 29.5 MeV $\cdot$ cm^2 $\cdot$ mg^{-1}).

5 Partial experiment verification

5.1 Experiment setup

A test chip designed previously in twin-well process is used to verify the SEDT-induced SEU mechanism. In this chip, there exists a master-slave DFF chain shown in Figure 9, which consists of 2048 D-Flip-Flops (DFFs) and 4096 inverters acting as their clock tree. The DFFs in Figure 9 are all implemented with the circuit schematic shown in Figure 1. In the layout design, the inverters in clock tree are inserted into the DFF chain uniformly, that is, the repeatable basic module consists of an inverter, a DFF as well as an inverter, and the layout is composed of 2048 of this repeatable basic module. Thus, this DFF chain is used to verify the SEDT-induced SEU mechanism.

Heavy ion experiment was performed at Cyclotron in the China Institute of Modern Physics in Lanzhou, Kr ion is used, of which the LET is about 29.5 MeV $\cdot$ cm^2 $\cdot$ mg^{-1}. The chip works at room temperature with the supply voltage of 1.0 V, and the static test mode is employed. Only one data pattern is tested, i.e. all '0', that is to say, all DFFs are initialized with '0' before heavy ion radiation. In this static test mode, there are two possible configuration for 'CLK' signal in Figure 8, i.e. '0' and '1' (or 'Low' and 'High'), and the all '0' data pattern with 'CLK' biased to '0' and '1' is called 'L00' and 'H00' respectively. In summary, only two cases 'L00' and 'H00' are tested, and the total fluence is 1×10^7 ions $\cdot$ cm^{-2} for each case with the ion flux of 1×10^4 ions $\cdot$ cm^{-2} $\cdot$ s^{-1}.

5.2 Experiment principle

In 'L00' case, 'CLK' is biased to '0', then signal 'CK' in Figure 1 is '1', and then the master latch in any DFF is in updating mode while the slave latch in any DFF is in holding mode. At this circumstance, even if the input of the master latch and the clock inverter are struck by a heavy ion simultaneously, no SEDT-induced SEU occurs for the SET in clock inverter will change the state of the master latch into hold mode. However, in 'H00' case, 'CLK' is biased to '1', then all master latches are in holding mode while all slave latches are in updating mode. The simultaneous hit in the input of the master latch and the clock inverter will bring about SEDT-induced SEU, for the SET in clock inverter will change the stage of the master latch into updating mode. Because the test mode is static, the direct upset in 'L00' case and 'H00' case is the same in theory, other indirect upset mechanisms have no effect on total SEU, and then the difference of 'L00' and 'H00' cases is induced by SEDT-induced SEU mechanism.

5.3 Experiment results

The heavy-ion experiment results are shown in Figure 10. The SEU cross section is $6\times10^{-6}\pm1.55\times10^{-6}$ cm^2 in 'H00' case while it is $5\times10^{-6}\pm1.41\times10^{-6}$ cm^2 in 'L00' case, which agree well with the analysis in the context. Thus, no SEDT-induced SEU exists in 'L00' case, and the SEDT-induced

SEU cross section in 'H00' case is 1×10^{-6} cm^2 (6×10^{-6},-5×10^{-6}). The SEDT-induced SEU contributes 16.67% to the total SEU in 'H00' case. This is amazing, and then the SEDT-induced SEU is proved to exist in nanometer technology.

6 Conclusion

With technology scaling down to 65 nm bulk CMOS technology, SEDT-induced SEU is becoming a possible SEU mechanism for flip-flop, and it is closely related with the well structure. 3D TCAD simulation results indicate that the triple-well structure can promote the SEDT-induced SEU threshold greatly compared with twin-well structure. What is more, the well contact size has only a slight effect on SEDT-induced SEU, and increasing well contact size is not as good as using triple-well structure for a hardening design. The heavy-ion experiment has verified the SEDT-induced SEU mechanism in 65 nm bulk twin-well CMOS process, and the results indicate that this new upset mechanism should be taken into consideration in future hardening design in nanometer technology.

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Conflict of interest The authors declare that they have no conflict of interest.

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