

A 256×256 time-of-flight image sensor based on center-tap demodulation pixel structure

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Received July 21, 2015; accepted August 25, 2015; published online February 25, 2016

Abstract This paper proposes a 256×256 time-of-flight (TOF) image sensor based on the center-tap (CT) demodulation pixel structure. The image sensor can capture both the two-dimensional (2D) high speed image and the three-dimensional (3D) depth image. The CT pixel consists of two split pinned photodiode (PPD) regions and two pairs of transfer transistors. The transfer transistors adopt a non-uniform doped channel (NUDC) structure, which can increase the electron transfer speed along the transfer channel and eliminate the image lag for high speed imaging. The pixel size is $10 \mu\text{m} \times 10 \mu\text{m}$, and we design the implementation process of the pixel to increase the electron transfer speed. The sensor is fabricated in a $0.18 \mu\text{m}$ 1P5M CMOS image sensor process. Test results show that it can capture the 430-fps intensity image and the 90-fps depth image in two different imaging modes. The rectified non-linearity within the 1.0–7.5 m depth measurement range achieves less than 3 cm, and the measurement accuracy achieves 4.0 cm at 2.5 m, corresponding to the relative error of 1.6%.

Keywords CMOS image sensor, demodulation pixel, depth image, pinned photodiode, time-of-flight (TOF)

Citation Chen Z, Di S, Cao Z X, et al. A 256×256 time-of-flight image sensor based on center-tap demodulation pixel structure. *Sci China Inf Sci*, 2016, 59(4): 042409, doi: 10.1007/s11432-015-5453-0

1 Introduction

The vision chip is a smart vision sensor that integrates the image sensor and massively parallel processors on a single chip [1–3]. By mimicking the biological visual system, recent research on the vision chip focuses on complex vision tasks such as the object-of-interest detection [4] and the high speed object recognition [5]. However, compared with the binocular visual system of humans, state-of-the-art vision chips rely merely on the two-dimensional image sensor which ignores the depth information of the real world. Since the depth information plays an important role in complex vision tasks, the high speed image sensor with the depth imaging capability has great potential to increase the performance of the vision chip further in applications such as high speed object recognition, high speed robot vision, and human computer interaction.

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The time-of-light (TOF) image sensor based on the indirect-TOF (I-TOF) principle is one of the depth imaging methods [6,7]. It captures the depth image by demodulating the reflected signal and calculating the TOF time in a pixel-parallel way [8]. This method has such advantages as high speed, compact size, and low power consumption. Recently many prototype TOF image sensors based on this method have been reported [9–15]. An 80×60 TOF image sensor based on the lock-in pixel with extending transfer gates on top of the photodiode was presented [9]. The extending transfer gates are used to enhance the lateral electric field and increase the electron transfer speed. Based on the similar pixel structure, a QVGA resolution TOF image sensor with higher dynamic range [10] and a 198×108 TOF three-dimensional (3D) image sensor with the concentric-photogate pixel structure [11] were reported. However, the pixel with the extending transfer gate degrades the pixel sensitivity, so they are not suitable for the high speed imaging. Another TOF image sensor realizes a time-division multiplexing for color and depth imaging modes by using the unified pixel architecture [12], which shortens the electron transfer distance so that the electron transfer time is reduced. Based on the similar pixel architecture, a split and binning pixel structure was proposed to achieve a reconstruction between a 30-fps 1920×1080 color image sensor and an 11-fps 480×360 depth image sensor [13]. The issue of this architecture is the large driving load and the mismatch between different gates that may increase the measurement error. A 1.5 Mpixel RGBZ image sensor integrates 1920×720 color pixels and 480×360 depth measurement pixels [14]. It can achieve simultaneous color and depth imaging, but the frame rate is limited because it uses the serial readout method. The TOF depth-measurement sensor based on an improved pixel structure and a correspondingly novel TOF principle achieves less than 0.3 mm depth measurement accuracy [15]. However, the measurement range is limited to be within 32 mm.

This paper proposes a TOF image sensor based on a center-tap (CT) demodulation pixel structure. It can capture the two-dimensional (2D) high speed image and the I-TOF depth image separately in two operating modes: the 2D imaging mode and the 3D imaging mode. The CT pixel consists of two split pinned photodiode (PPD) regions, a CT floating diffusion (FD), two symmetric drain diffusions (DDs), two M_{TX} transistors, two M_{TXD} transistors and a M_{RST} transistor. The M_{TX} and M_{TXD} transistors adopt the non-uniform doped channel (NUDC) structure. It helps increase the electron transfer speed along the transfer channel and eliminate the image lag for high speed imaging. We fabricated a 256×256 TOF image sensor in a $0.18 \mu\text{m}$ 1P5M CMOS image sensor process. Test results show that the maximum frame rates in the 2D and 3D imaging modes achieve 430 fps and 90 fps, respectively. Measurement results demonstrate that the sensor achieves a reliable depth measurement range of 1.0–7.5 m. The rectified non-linearity is less than 3 cm, and the measurement accuracy achieves 4.0 cm at 2.5 m distance under the 20-ms integration time, corresponding to the 1.6% relative error.

2 Center-tap (CT) demodulation pixel structure

2.1 CT pixel structure

Figure 1(a) shows the schematic of the CT pixel. The pixel consists of two split PPD regions, a CT FD, two symmetric DDs, two M_{TX} transistors, two M_{TXD} transistors and a M_{RST} transistor. The PPD is split into two photosensitive regions so the lateral transfer distance from the PPDs to the FD is remarkably reduced. As a result, the electron transfer time is reduced. Compared with demodulation pixels with extending gates, the CT pixel achieves higher pixel sensitivity by avoiding the usage of the extending gates. In addition, the single-tap structure eliminates the mismatch existing in multi-tap pixel designs.

In an I-TOF depth sensing system, an infrared (IR) light source is driven by a continuous pulse modulated signal. The emitted IR signal irradiates the object and is reflected backwards to the sensor. The phase shift of the reflected signal is demodulated by the CT pixel. The M_{TX} and M_{TXD} transistors in the pixel are driven by a couple of sampling and resetting signals with opposite phase states. The frequency of the sampling signal is the same as that of the emitted IR signal. The M_{TX} and M_{TXD} transistors are switched on and off alternatively to fulfil the integration of the reflected signal at the FD and the resetting at the PPDs.

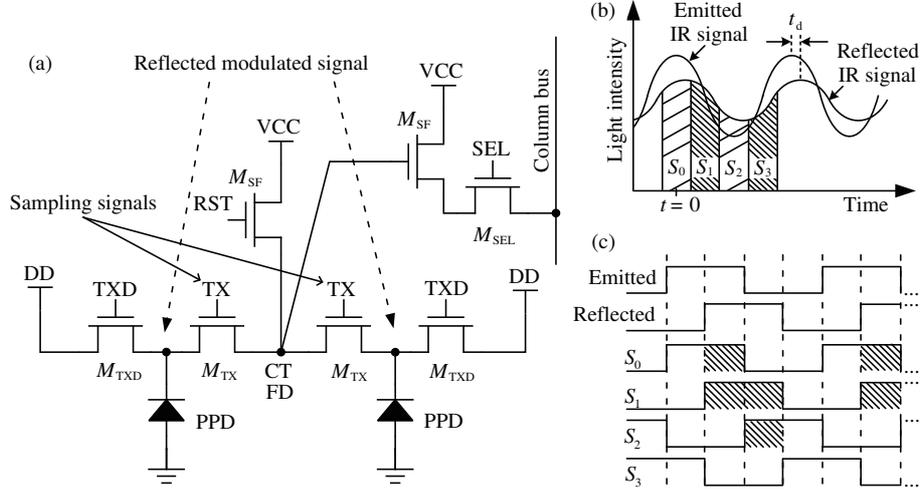


Figure 1 (a) Schematic of the CT pixel; (b) I-TOF sampling method; (c) timing diagram of the sampling signals.

In order to calculate the depth image, four images have to be captured by dedicated sampling signals with different phases. Figure 1(b) and (c) show the I-TOF sampling method and the sampling signal diagram, respectively. The phase shifts between the sampling signal and the emitted IR signal are set to be 0° , 90° , 180° , and 270° at four sampling points, respectively. For each pixel, the measured depth D can be calculated by

$$D = \frac{c}{4\pi f_m} \arctan\left(\frac{S_3 - S_1}{S_2 - S_0}\right), \quad (1)$$

where f_m is the modulation frequency, c is the propagation speed of the IR signal, and S_0 - S_3 represent the sampled IR signals at the FD in four sampling phases, respectively. Since the demodulated phase delay has an unambiguous range of 2π , the maximum measurement range D_R is limited by

$$D_R = \frac{c}{4\pi f_m} \cdot 2\pi = \frac{c}{2f_m}. \quad (2)$$

2.2 Pixel process design

2.2.1 NUDC structure

The proposed NUDC structure has been proved as an effective technique to eliminate the image lag in high speed image sensor design [16]. We designed the NUDC structures in the CT pixel, as shown in Figure 2(a). The NUDC structure forms gradient potential profile and enhances lateral electric field along the transfer channels of the M_{TX} and M_{TXD} transistors. Figure 2(b) shows the simulation result of the potential profile. When the M_{TX} and M_{TXD} transistors are switched from on-state into off-state, charges in the channels are driven into the FD and DDs rather than backwards into the PPDs. In this way, the electron transfer speed is increased, and the image lag caused by the backward charge into the PPDs can be eliminated. The NUDC structure is formed by the overlap of the $p+$ doped layers of the PPDs and the $p-$ doped layers of the M_{TX} and M_{TXD} channels, so it does not cost additional mask in the manufacturing process.

2.2.2 PPD process

Figure 3(a) shows the simulated doping concentration of the CT pixel structure. The doping concentration can be raised by increasing the injection dose and energy, and the doping concentration inside the PPDs has an effect on the electron transfer speed from the PPDs to the FD [17]. Figure 3(b) shows the simulated dependence of the electron transfer time on the injection dose and energy of the $n+$ layer in PPDs. If

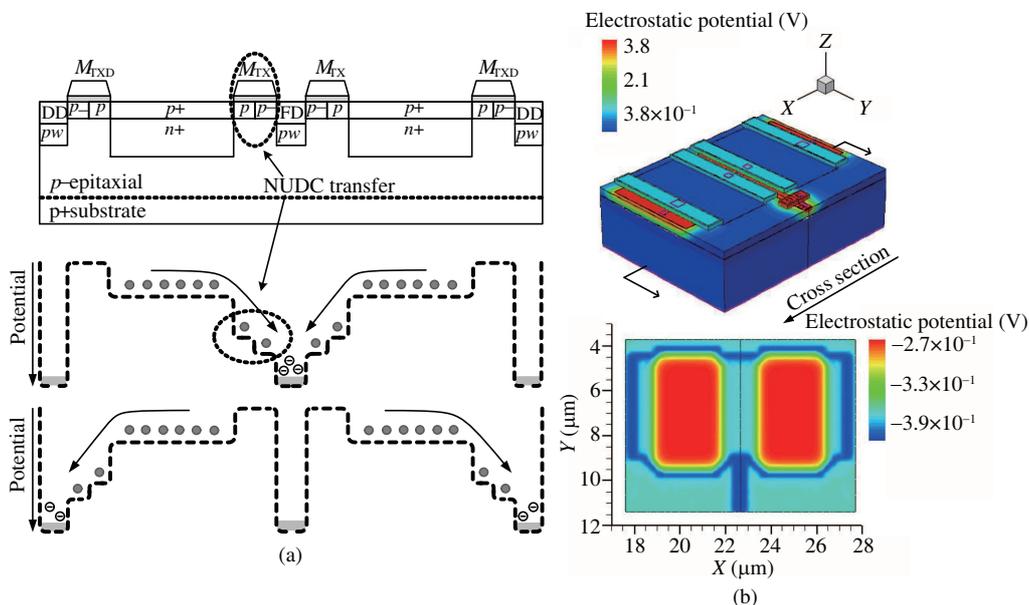


Figure 2 (a) Cross section and potential diagram of the CT demodulation pixel; (b) simulation of the gradient potential distribution formed by the NUDC structure.

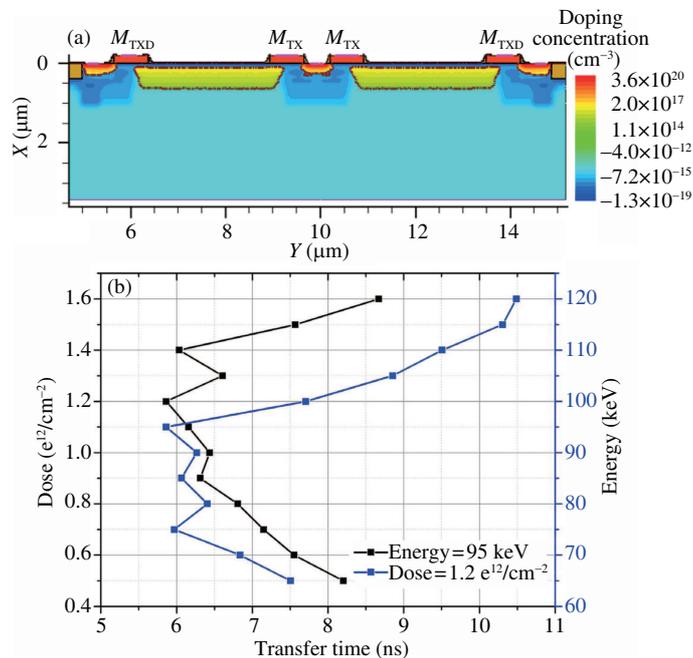


Figure 3 (a) Simulation result of the doping concentration in the CT pixel structure; (b) relationship between the electron transfer time and the injection dose and energy of the n^+ layer of the PPDs.

the doping concentration of the n^+ layer increases, the carrier mobility decreases so the diffusion velocity will decrease. On the other hand, if the doping concentration rises, the intensity of the vertical electric field inside the n^+ layer of the PPDs increases. The increased vertical electric field will increase the drift velocity of the electrons. Considering both of the effects, the electron transfer speed will first increase and then decrease as the doping concentration inside the n^+ layer of the PPDs increases. When the injection dose and energy are set $1.2 \text{ e}^{12}/\text{cm}^{-2}$ and 95 keV respectively, the electron transfer time reaches the minimum of 6 ns, which satisfies the I-TOF principle.

The split-PPD CT pixel structure reduces the transfer distance of the photo-generated electrons and

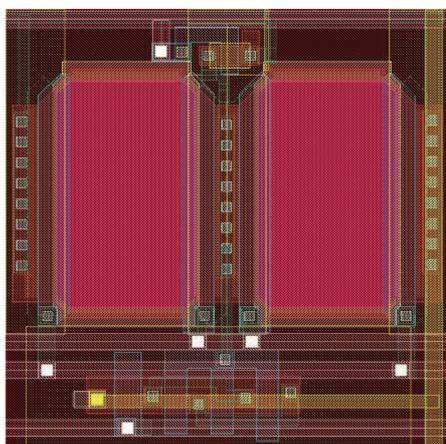


Figure 4 (Color online) Layout of the CT pixel.

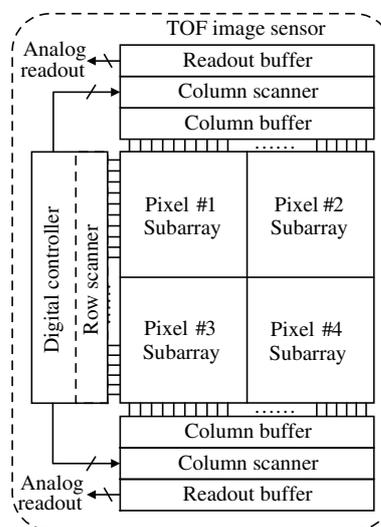


Figure 5 Architecture of the proposed TOF image sensor.

remains high pixel sensitivity at the same time. This pixel structure also eliminates the mismatch between different samplings. The NUDC structure adopted by the transfer transistors help increase the electron transfer speed along the transfer channel and reduce the image lag for high speed imaging. The adjusted doping dose and energy help increase the electron transfer speed further. By combining these techniques, the TOF image sensor achieves both the high speed imaging and the depth imaging.

2.2.3 CT pixel layout

Figure 4 shows the layout of the proposed CT pixel. The pixel size is $10\ \mu\text{m} \times 10\ \mu\text{m}$, and the fill factor of the pixel is 32%. Four types of pixels with different FD lengths of $4.5\ \mu\text{m}$, $3.5\ \mu\text{m}$, $2.5\ \mu\text{m}$ and $1.5\ \mu\text{m}$ are designed to evaluate the effect of the FD length on the depth measurement accuracy.

2.3 TOF image sensor architecture

We designed a 256×256 TOF image sensor based on the proposed CT pixel. Figure 5 shows the block diagram of the sensor architecture. The image sensor consists of a digital controller, four subarrays of pixels with different FD lengths, and the analog readout circuits arranged on both sides of the pixel array. The digital controller generates control signals for both of the imaging modes under an 80-MHz operating clock [18]. The clock frequency is set four times as high as the modulation frequency so that the sampling signals in four sampling phases can be easily generated. By reducing the clock frequency, the measurement range can be expanded. For example, when the clock frequency is reduced to 60 MHz, the modulation frequency becomes 15 MHz, and the measurement range turns out to be 10 m according to (2). The analog readout circuit is made up of column-parallel buffers, scanners and readout buffers. The raw data are read out in parallel through 16 readout paths for high speed imaging.

The timing diagrams of the 2D and 3D imaging modes are shown in Figure 6(a) and (b), respectively. In the 2D imaging mode, the rows of pixels are exposed in a rolling shutter manner. For each row of pixels, the control timing first implements the signal integration and then fulfils the correlated double sampling (CDS). First, the M_{RST} and M_{TXD} are switched on simultaneously to reset the FD and the PPDs. Then the exposure process begins, and it lasts until the row select signal $\phi_{\text{SEL}}[n]$ becomes high, which indicates that the readout procedure begins. The readout procedure consists of three steps. First, the FD is reset by switching on the M_{RST} , and the reset signal is read out. Secondly, the photoelectrons accumulated in the PPDs are transferred to the FD through the M_{TX} transistors. Finally the signal at the FD is read out to accomplish the external CDS. In the 3D imaging mode, the sensor also operates in the rolling shutter manner. During the exposure process, the M_{TX} and M_{TXD} transistors are switched on

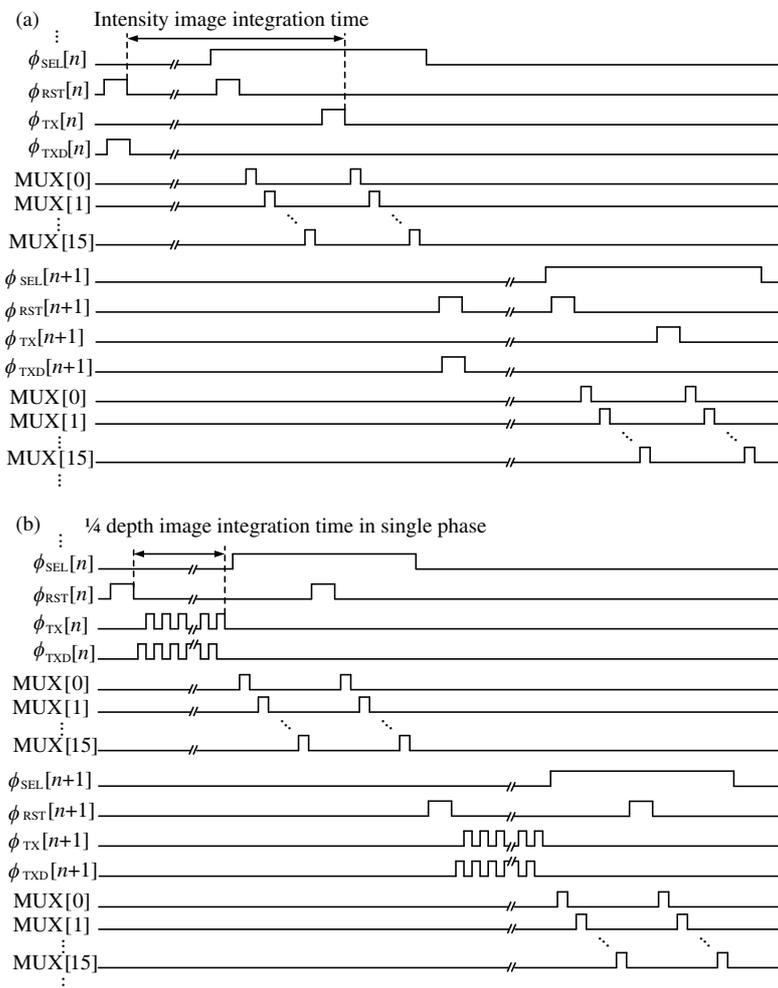


Figure 6 (a) Timing diagram of the integration and the CDS in the 2D imaging mode; (b) timing diagram of the integration and the pseudo-CDS in one of the four sampling phases in the 3D imaging mode.

and off alternatively to accomplish the signal integration at the FD. The exposure time can be adjusted by changing the switch-on-and-off times. When the exposure finishes, the integrated signal at the FD is read out first, and then the FD is reset and the reset signal is read out to fulfil the pseudo-CDS. After the pseudo-CDS finishes, we get the raw image data in one particular sampling phase. Raw image data in four sampling phases need to be collected completely until the depth image can be calculated by (1).

2.4 Experimental results

The TOF image sensor is fabricated in a 0.18 μm 1P5M CMOS image sensor process. Figure 7 shows the microphotograph of the sensor. Testing of the image sensor has been carried out in two separate cases: the high speed imaging and the depth imaging.

Figure 8 shows the photograph of the measurement setup for testing the fabricated image sensor. The measurement setup consists of the test board, the IR LED emitter, the lens and the camera obscura. The test board is equipped with the TOF image sensor under test, 16 parallel 14-bit ADCs, 8 parallel 28-bit LVDS transmitters and a FPGA. The FPGA has been used to collect data and implement the digital CDS and pseudo-CDS procedures. The IR LED source is driven by the 20-MHz continuous pulse modulated signal. The driving signal is synchronized with the 80-MHz clock of the on-chip controller.

The TOF image sensor has achieved a maximum frame rate of 430 fps in the 2D imaging mode, and the integration time is 250 μs . The frame rate is decided by the timing diagram of the rolling shutter exposure and can be configured by setting the parameters. When we set the time interval between

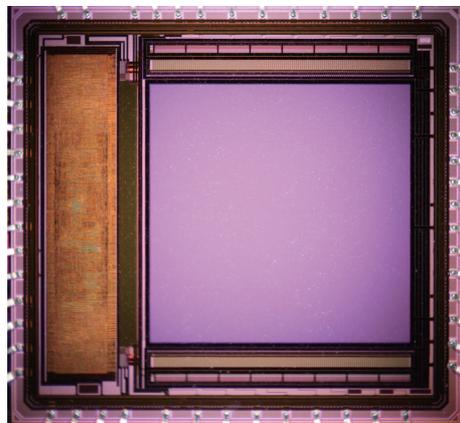


Figure 7 (Color online) Microphotograph of the TOF image sensor.

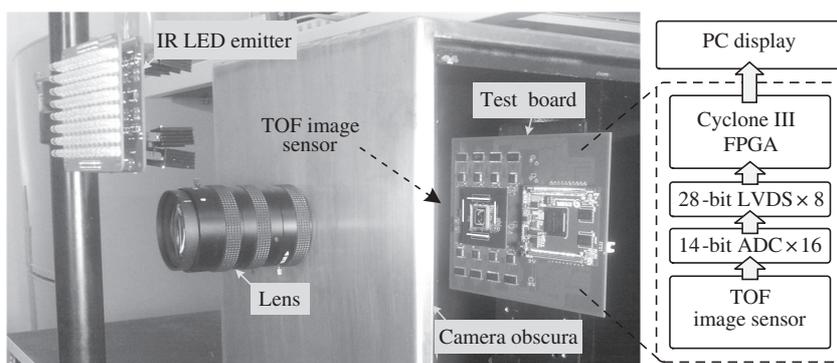


Figure 8 Measurement setup for testing the TOF image sensor.

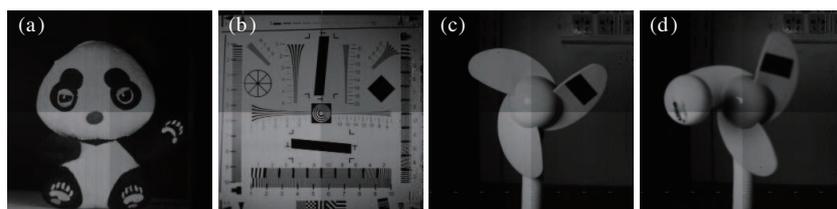


Figure 9 Captured images in the 2D and 3D imaging modes, including sample intensity images of (a) the panda doll, (b) the standard resolution chart, (c) the stationary fan, (d) the rotating fan with a falling table tennis ball.

different rows of pixels to be 714 clock cycles under the 80-MHz clock frequency, the frame rate reaches the maximum value of about 430 fps. The maximum frame rate is limited by the readout timing and can be increased further by improving the readout circuit design. Figure 9(a)–(d) shows the intensity images captured in the 2D imaging mode. It can be seen that four sub-images with different sizes of FD areas have different average intensities. The FD with smaller area has smaller parasitic capacitance and results in a higher conversion gain. As a result, under the same illumination condition, the sub-image captured by the small-FD pixels has a higher intensity. Figure 9(d) shows the captured image of a rotating fan with a falling table tennis ball under the maximum frame rate. It demonstrates the high speed imaging quality of the proposed TOF image sensor.

Figure 10(a) and (b) show the intensity and depth images captured under the same scene. The depth image is calculated according to (1) with four consecutive images captured in four sampling phases with the integration time of 10 ms, which corresponds to a frame rate of around 50 fps. However, since the integration time is configurable, it can be set as short as possible, and the maximum frame rate is only limited by the readout timing. In our design, the maximum speed for 3D imaging can reach up to 90 fps when we set the integration time as short as 100 μ s in the test with a mirror as the target. As

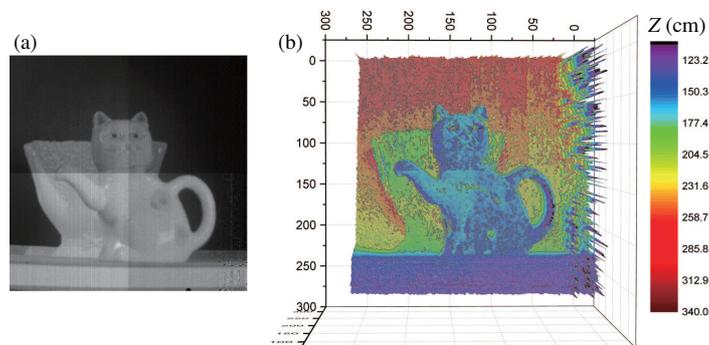


Figure 10 (a) Intensity image captured in the 2D imaging mode and (b) the corresponding depth image captured in the 3D imaging mode.

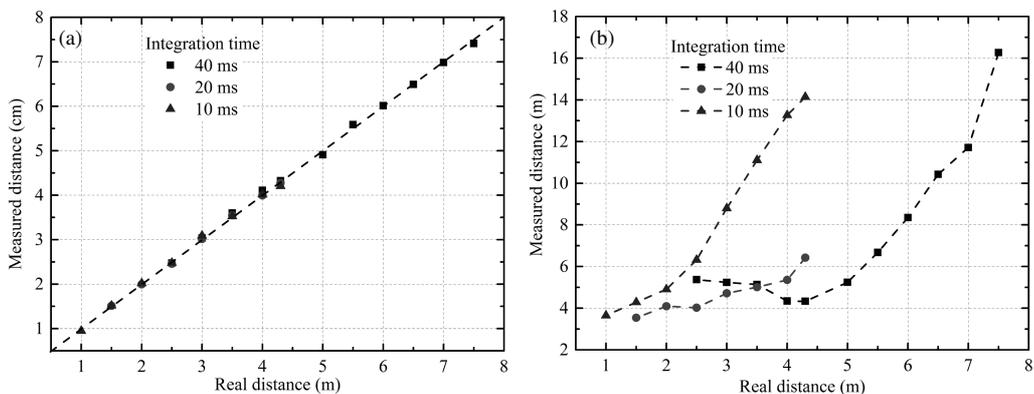


Figure 11 Depth measurement result: (a) the measured distance; (b) the depth measurement accuracy.

can be seen in Figure 10(b), the depth imaging qualities at the edges of the objects and in the dark areas at the background are relatively low. The reason is that the intensity of the reflected signals from these regions are very low. It is caused by the irregular specular reflection and the low reflectivity of the diffuse reflection [12]. It can also be observed that some erroneous depth measurement values exist on the right side of the captured image. In practice, we found that the volatile measurement results sometimes appear on the right side, and in other times appear on the left side, so we speculate that the erroneous values might be caused by the timing issues inside the measurement setup hardware.

In order to evaluate the depth measurement accuracy of the proposed TOF image sensor, we carried out the depth measurement with a piece of white paper. Figure 11(a) shows the depth measurement results with the integration time of 10 ms, 20 ms and 40 ms, respectively. In each case with specific integration time condition, we captured a subset of raw depth images under gradually increased target distances. Then we calculated the measured distance according to (1). Since there is constant delay between the emitted IR signal and the sampling signal inside the chip, the calculated result will be induced with an offset compared with the real distance. In order to eliminate the fixed system error caused by the measurement setup, we calibrate the calculated results by utilizing the estimated linear fitting formula based on the least squares method. The non-linearity of the calibrated measurement results within the measurement range of 1.0–7.5 m turns out to be less than 3 cm. Figure 11(b) shows the evaluated depth measurement accuracy of the depth imaging system. The accuracy is calculated by counting the pixel values in a 20×20 pixel subarray in 30 continuously captured depth images. According to the measurement setup, the depth measurement accuracy achieves 4.0 cm at 2.5 m under the 20-ms integration time, corresponding to the 1.6% relative error. The measurement accuracy is affected by both of the intensity of the reflected signal and the integration time, but the influence of the FD length on the accuracy has not been observed. Assuming that the integration time is constant, the intensity of the reflected signal decreases as the measurement distance increases. This makes the received signal to noise

Table 1 Chip characteristics and performance comparison with previous TOF image sensor designs

	This work	Range image sensor [9]	QVGA-Range image sensor [10]	2D/3D CMOS image sensor [12]
Process	0.18 μm 1P5M	0.18 μm 1P4M	0.18 μm 1P4M	0.11 μm 1P4M
Resolution	256 \times 256	80 \times 60	320 \times 240	712 \times 496
Pixel pitch	10 μm	10 μm	14 μm	6 μm for color, 12 μm for depth
Fill factor	32%	24%	48%	34.5%
Die size	4.4 mm \times 4.1 mm	N/A	5 mm \times 5 mm	6 mm \times 6 mm
Power dissipation	140 mA for 3.3 V, 30 mA for 1.8V	14 mW for 3.3 V, 4.4 mW for 1.8 V	73 mA for 3.3 V, 0.1 mA for 1.8 V	53 mW for color, 357 mW for depth
Emitter	850 nm LED	850 nm LED	850 nm LED	850 nm LED
Modulation freq.	20 MHz	20 MHz	16.67 MHz	10 MHz
Operating clock	80 MHz	N/A	N/A	N/A
Lens	f = 8 mm, F# = 1.6	f = 6 mm, F# = 1.4	f = 2.9 mm, F# = 1	f = 6.5 mm, F# = 2.2
Measurement range	1.0–7.5 m	0.2–6 m	0.8–7.5 m	1–3 m
Depth non-linearity	< 3 cm	< 2 cm	2.1 cm	< 2%
Depth accuracy	4.0 cm @ 2.5 m	< 4 cm best, 16 cm @ 6 m	2.6 cm best, 16 cm @ 7.5 m	10–43 mm
2D Integration time	250 μs –2.3 ms	N/A	1–18 ms	N/A
3D Integration time	10–40 ms ¹⁾	50–200 ms	4–72 ms	50 ms
2D max. frame rate	430 fps	N/A	280 fps	18 fps
3D max. frame rate	90 fps	20 fps	70 fps	6.4 fps

(SNR) ratio decrease, and causes the measurement accuracy to be decreased. The decreased received SNR can be compensated by increasing the radiant intensity of the IR emitter. However, the increased IR signal intensity may cause the pixel saturation when the object gets close to the sensor. Extending the integration time is another way to increase the intensity of the integrated received signal. However, the extended integration time increases the noise level at the same time. In addition, the frame rate of the depth imaging will decrease as a result.

Table 1 summarizes the chip characteristics and provides performance comparison with previous TOF image sensor designs. The prototype TOF image sensor outperforms its counterparts in high speed imaging, while it achieves the similar performance in depth imaging compared with other reported TOF image sensors.

3 Conclusion

A TOF image sensor based on the CT demodulation pixel structure has been proposed. The CT pixel structure has been designed to increase the electron transfer speed from the PPDs to the FD and DDs. This pixel structure achieves high pixel sensitivity and eliminates the mismatch between different sampling phases for the depth imaging. The NUDC structure has been designed in the CT pixel to increase the electron transfer speed along the transfer channel and eliminate the image lag for high speed imaging. The manufacturing process of the CT pixel has been designed to speed up the electron transfer further. The TOF image sensor is fabricated in a 0.18 μm 1P5M CMOS image sensor process. It achieves both the 430-fps 2D imaging and the 90-fps 3D imaging. The depth measurement accuracy achieves 4.0 cm at 2.5 m. Further research includes integrating the TOF image sensor with massively parallel processors and using the depth information to enhance the vision chip performance further in face of complex high speed vision tasks.

1) Values indicate the specific range used in the white-paper test and can be extended by configuration.

Acknowledgements This work was supported by National Natural Science Foundation of China (Grant Nos. 61234003, 61434004, 61504141) and Special Funds for Major State Basic Research of China (Grant No. 2011CB932902). The authors would like to thank Runjiang Dou for the setup of the imaging test platform.

Conflict of interest The authors declare that they have no conflict of interest.

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