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LSB page refresh based retention error recovery scheme for MLC NAND Flash

Haozhi MA[1*], Lifang LIU[1], Liyang PAN[1,2] & Jun XU[1,2]

[1] *Institute of Microelectronics, Tsinghua University, Beijing* 100084*, China;*
[2] *Tsinghua National Laboratory for Information Science and Technology, Beijing* 100084*, China*

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Abstract NAND Flash memories present inevitable decline in reliability due to scaling down and multi-level cell (MLC) technology. High retention error rate in highly program/erase (P/E) cycled blocks induces stronger ECC requirement in system, causing higher spare bits cost and hardware overhead. In this paper, a least significant bit (LSB) page refresh based retention recovery scheme is proposed to improve the retention reliability of highly scaled MLC NAND Flash. As in the scheme, LSB page refresh operation induces floating gate electron re-injection to compensate charge leakage during long retention time, and realizes retention error rate reduction. Experiment result on 2x-nm MLC NAND Flash exhibits more than 78% retention error rate reduction. Compared with reported retention error recovery scheme, the proposed scheme presents 2.5 times recovery efficiency promotion and 60% latency reduction.

Keywords NAND flash, reliability, retention, refresh, data error recovery

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1 Introduction

Due to significant improvements on data throughput, capacity and power consumption, NAND Flash memories have been the prevailing non-volatile storage solution and are widely used in consumer electronics productions. To satisfy the increasing demand for storage capacity, NAND Flash has scaled down to 16 nm technology node and multi-level cell (MLC) technology has also been adopted [1,2]. However, the highly scaled MLC NAND Flash memories suffer from serious degradation of reliability and endurance [3]. A 5x-nm single-level cell (SLC) NAND Flash cell can tolerate 10000 program erase (P/E) cycles, while a 2x-nm MLC cell can only endure 3000 P/E cycles [4]. As the geometric sizes of the floating gate are especially shrinked due to cells scaling down, electrons stored in floating gate tend to be remarkably decreased. In addition, MLC technology demands narrower threshold voltage distributions, so highly scaled NAND Flash memories present higher sensibility with floating gate charge leakage during data storage, and data error rate increases drastically with P/E cycles and retention time [5].

Error correction codes (ECC) such as Bose-Chaudhuri-Hocquenghem (BCH) and low-density parity check code (LDPC) [6,7] have been used to solve the reliability issues of highly scaled MLC NAND Flash

* Corresponding author (email: mhz10@mails.tsinghua.edu.cn)

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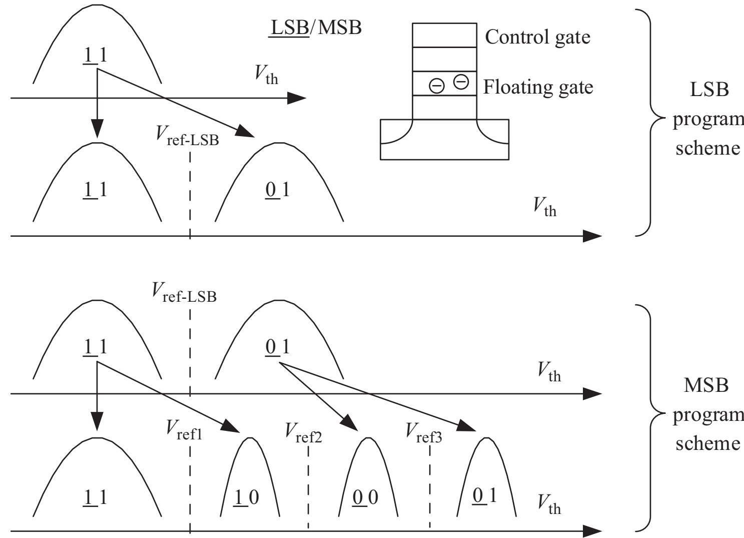


Figure 1 MLC NAND Flash cell V_{th} distributions.

memories. However, high retention error rate induces a trend of stronger ECC deployed in storage system, with higher hardware overhead and spare bits cost.

Currently, retention error recovery schemes are proposed to overcome the high retention error rate problem of MLC NAND flash memories [8–11]. In these schemes, floating gate electron leakage during retention can be compensated by electron re-injection. Electron re-injection is realized by either read disturbance (RD) [8–10] or word line program disturbance (WPD) [11]. WPD based scheme presents higher recovery efficiency than RD based scheme [11]. However, it still suffers from high operation cycles and long latency time.

In this paper, we proposed a least significant bit (LSB) page refresh based retention error recovery scheme to improve the retention reliability of highly scaled MLC NAND Flash. In the proposed scheme, electron compensation is realized by LSB page read and refresh. Experiments on 2x-nm MLC NAND Flash exhibit more than 78% retention error rate reduction and 40% error-correction capability relaxation. Compared with reported scheme, the proposed scheme presents 2.5 times recovery efficient promotion and 22% operation latency improvement. The improvement on retention reliability and recovery efficient implies 20% endurance extension.

The rest of the paper is organized as follows. Section 2 analyzes basic operations and reliabilities of MLC NAND Flash memories. Section 3 presents the proposed LSB page refresh based retention error recovery scheme. Section 4 presents the experiment results and discussion. And at last, Section 5 concludes this paper.

2 Reliability of MLC NAND Flash

2.1 MLC NAND Flash basic

NAND Flash cell features a transistor with a control gate (CG) and a floating gate (FG) as shown in the insert of Figure 1. Cell threshold voltage (V_{th}) can be quantized by controlling the amount of electrons in floating gate. In MLC NAND Flash, each cell stores 2-bit information by setting cell V_{th} into 4 non-overlapping voltage windows. As the conventional definition, one bit in a cell belongs to the least significant bit (LSB) page and the other bit belongs to the most significant bit (MSB) page [12].

Figure 1 illustrates cell voltage distributions during basic operations. After erase, all cells' V_{th} are set into the lowest status. As one MLC NAND flash cell stores two bits, cell program is achieved in two distinct rounds. In the first round, LSB is programmed by setting V_{th} into two windows, and then, in MSB program round, V_{th} is set into four windows decided by both LSB and MSB.

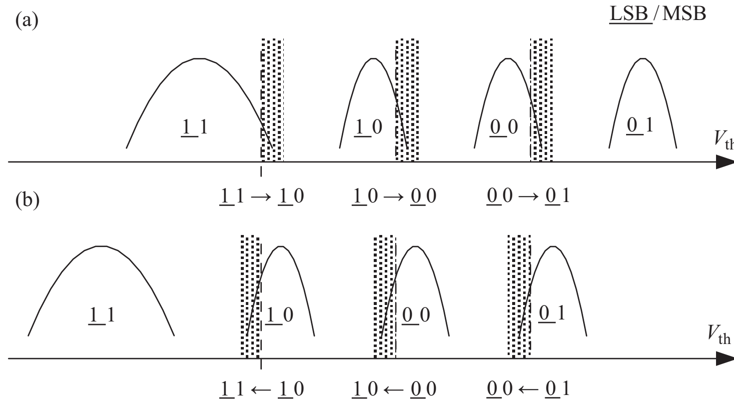


Figure 2 Cell V_{th} distributions of (a) over program error and (b) retention error.

2.2 Reliability of MLC NAND Flash

Data in NAND Flash are represented by cell $V_{\rm th}$ determined by the amount of floating gate electrons. Floating gate electron over-injection or leakage can induce data errors. Electron over-injection corresponds to error patterns indicating cell $V_{\rm th}$ increase such as 11→10, 10→00, or 00→01 and electron leakage corresponds to error pattern indicating cell $V_{\rm th}$ decrease such as 10→11, 00→10 and 01→00 (Figure 2). Program errors are mainly caused by floating gate electron over-injection and retention errors are mainly caused by floating gate electron leakage.

Program and retention error rate are characterized on 2x-nm 32 GB commercial MLC NAND Flash memories (Figures 3 and 4). The page size of the NAND Flash is 8832 bytes, and each block contains 128 pages. For the measurement, devices are stressed to 3000–6000 P/E cycles with pseudo random data. Program errors are measured immediately after block program completes and retention errors are examined by high temperature data-retention test (HTRD). According to the classic temperature activates Arrhenius law [1)], with activation energy of 1.1 eV for floating gate electrons detraining, the HTDR acceleration factor is 939 and annealing at 125°C for 9 hours 20 minutes is then equivalent to 1 year at 55°C according to JESD47G [13]. The bit error rate (BER) and pattern error rate are calculated by (1) and (2).

$$\text{Bit error rate (BER)} = \frac{\text{Number of error bits per block}}{\text{Total number of bits per block}}, \tag{1}$$

$$\text{Pattern error rate} = \frac{\text{Number of certain error pattern per block}}{\text{Total number of cells per block}}. \tag{2}$$

Figure 3 shows the correlations between program BER and P/E cycles. Program BER almost exponentially increases with P/E cycles, which can be explained by tunnel oxide defects accumulation during P/E cycles [14,15]. Similarly, retention BER also increases with P/E cycles. In addition, retention BER almost linearly increases with retention time as shown in Figure 4. The measured P/E cycles and retention time dependence of program BER and retention BER agree well with existing work [10,16,17].

According to Figures 3 and 4, program BER in 6000 P/E cycled blocks is about 3 orders higher than fresh blocks. Meanwhile, in 6000 P/E cycled blocks, 4-year retention BER is about 2 orders higher than program BER. That is, retention BER in blocks with 6000 P/E cycled and 4-year retention is about 5 orders higher than program BER in fresh blocks.

Since a storage system must guarantee the ability of keeping information reliably during long retention time, the high retention error rate results in much stronger ECC indispensable in system, with higher hardware overhead and spare bits cost. The high retention error rate represents one critical problem for highly scaled MLC NAND Flash.

1) Arrhenius equation (for reliability). http://www.jedec.org/standards-documents/dictionary/terms/arrhenius-equation-reliability.

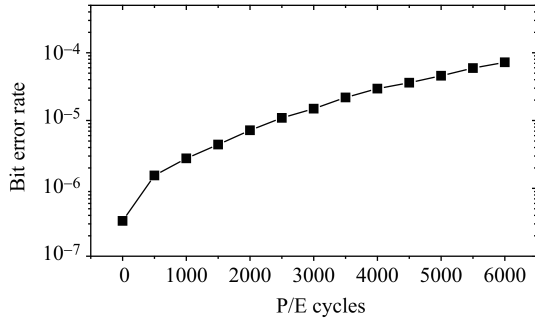


Figure 3 Program BER versus P/E cycles.

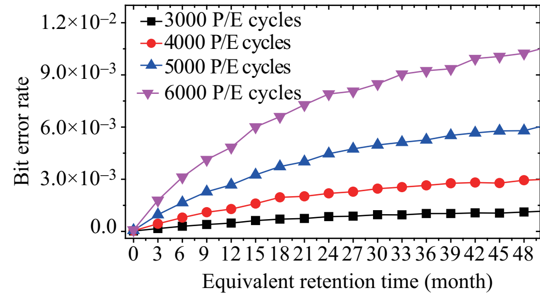


Figure 4 (Color online) Retention BER versus P/E cycles and retention time.

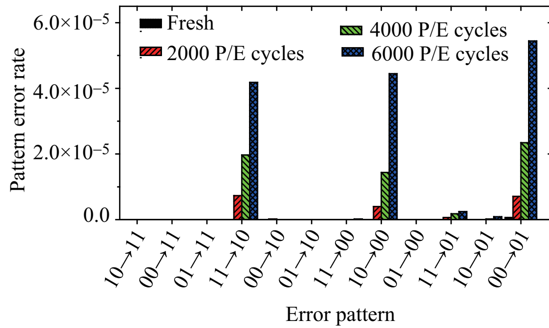


Figure 5 (Color online) Program error pattern distributions corresponding to P/E cycles.

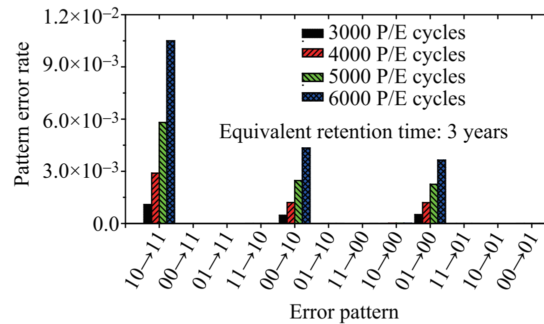


Figure 6 (Color online) One-year retention error pattern distributions versus P/E cycles.

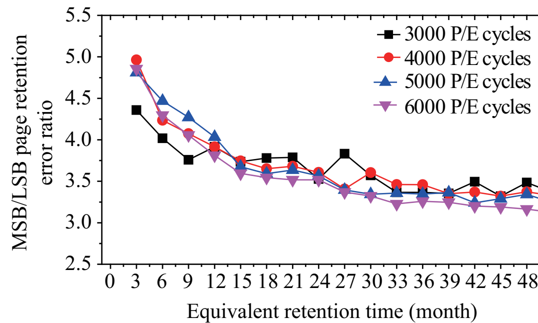
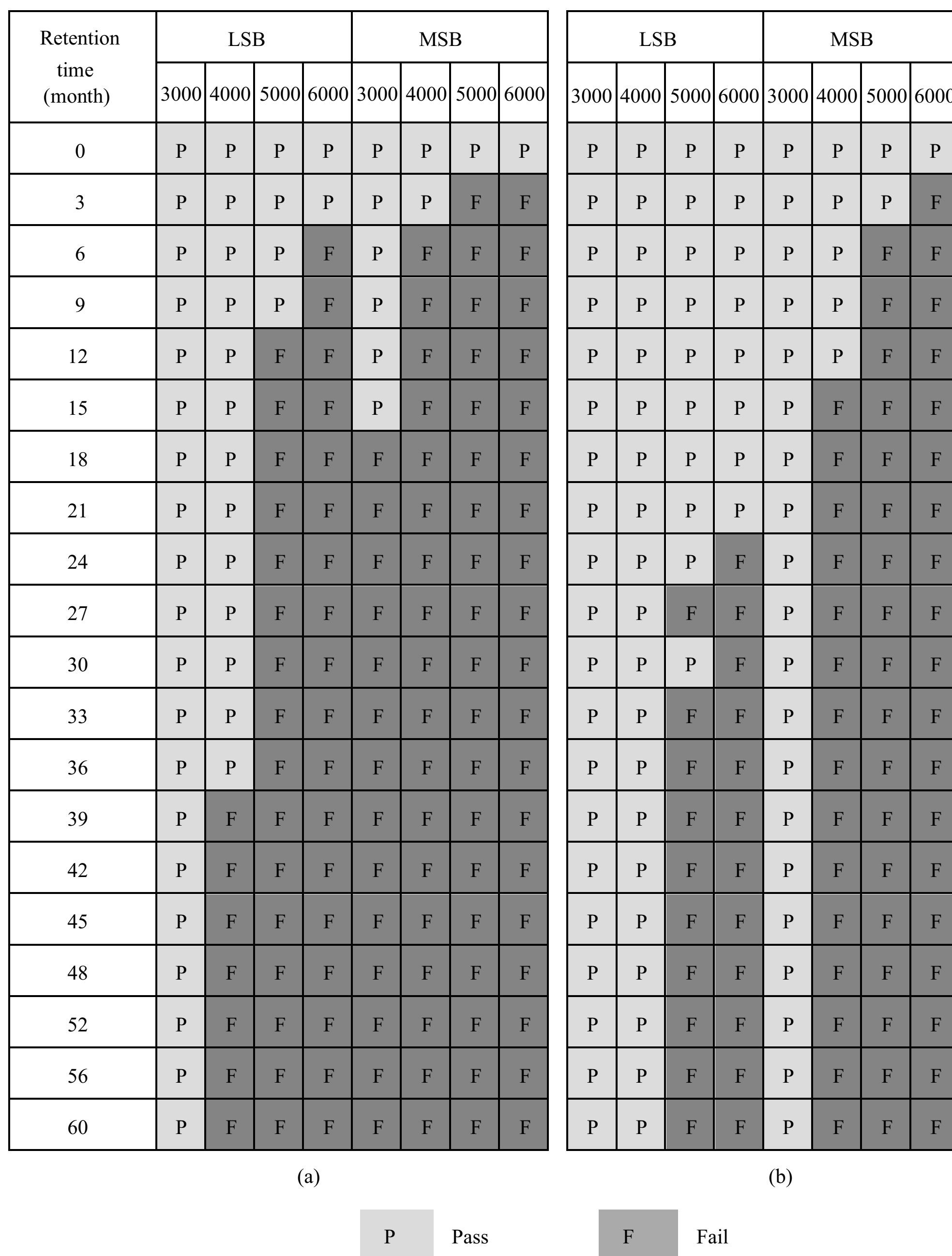


Figure 7 (Color online) MSB/LSB page retention error ratio corresponding to P/E cycles and equivalent retention time.

In the experiment, program and retention error pattern distributions are also measured as shown in Figures 5 and 6. The dominant program error patterns are 11→10, 10→00 and 00→01, while the dominant retention error patterns are 10→11, 00→10 and 01→00. The opposite distribution can be explained as follows: program errors are mainly caused by floating gate electron over-injection due to program disturbances [18], cell-to-cell interference [19], and incremental step pulse programming (ISPP) failing [20], while retention errors are mainly caused by floating gate electron leakage due to de-trapping [21] and trap assisted tunneling (TAT) [22].

According to LSB and MSB mapping scheme as shown in Figure 1, in the above dominant error patterns, only 10→00 and 00→10 correspond to LSB errors while 11→10, 00→01 and 10→11, 01→00 correspond to MSB errors. So MSB pages present higher program and retention BER than LSB pages in MLC NAND flash memories.

Figure 7 measures retention BER ratios between MSB and LSB pages in the same block. MSB pages retention BER is about 3 to 5 times higher than LSB pages. The asymmetric retention BER causes ECC



Retention time (month)	(a) LSB				(a) MSB				(b) LSB				(b) MSB			
	3000	4000	5000	6000	3000	4000	5000	6000	3000	4000	5000	6000	3000	4000	5000	6000
0	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P
3	P	P	P	P	P	P	F	F	P	P	P	P	P	P	P	F
6	P	P	P	F	P	F	F	F	P	P	P	P	P	P	F	F
9	P	P	P	F	P	F	F	F	P	P	P	P	P	P	F	F
12	P	P	F	F	P	F	F	F	P	P	P	P	P	P	F	F
15	P	P	F	F	P	F	F	F	P	P	P	P	P	F	F	F
18	P	P	F	F	F	F	F	F	P	P	P	P	P	F	F	F
21	P	P	F	F	F	F	F	F	P	P	P	P	P	F	F	F
24	P	P	F	F	F	F	F	F	P	P	P	F	P	F	F	F
27	P	P	F	F	F	F	F	F	P	P	F	F	P	F	F	F
30	P	P	F	F	F	F	F	F	P	P	P	F	P	F	F	F
33	P	P	F	F	F	F	F	F	P	P	F	F	P	F	F	F
36	P	P	F	F	F	F	F	F	P	P	F	F	P	F	F	F
39	P	F	F	F	F	F	F	F	P	P	F	F	P	F	F	F
42	P	F	F	F	F	F	F	F	P	P	F	F	P	F	F	F
45	P	F	F	F	F	F	F	F	P	P	F	F	P	F	F	F
48	P	F	F	F	F	F	F	F	P	P	F	F	P	F	F	F
52	P	F	F	F	F	F	F	F	P	P	F	F	P	F	F	F
56	P	F	F	F	F	F	F	F	P	P	F	F	P	F	F	F
60	P	F	F	F	F	F	F	F	P	P	F	F	P	F	F	F

Figure 8 LSB/MSB ECC results with (a) 24-bit and (b) 40-bit BCH code.

performance differences between MSB and LSB pages even in the same block.

Figure 8 shows BCH ECC results in LSB and MSB pages. The error-correction capacity of BCH code is set to conventional 24-bit and 40-bit. Each BCH frame has 1084 bytes and each NAND Flash page contains 8 frames. BCH code decoding will succeed only if frame error bit number is not higher than code error-correction capability. ECC pass/fail is decided by whether BCH decoding succeeds or not in 1024 frames.

The reliable retention time can be defined as the last data-retention time before the first ECC failure [9]. As shown in Figure 8, LSB pages exhibits much longer reliable retention time than MSB pages. For blocks after 4000 P/E cycled, the reliable retention time of LSB pages is 36 months with 24-bit BCH ECC and more than 60 months with 40-bit BCH ECC, while data in MSB pages can only survive for 15 and 12 months with the same BCH ECC.

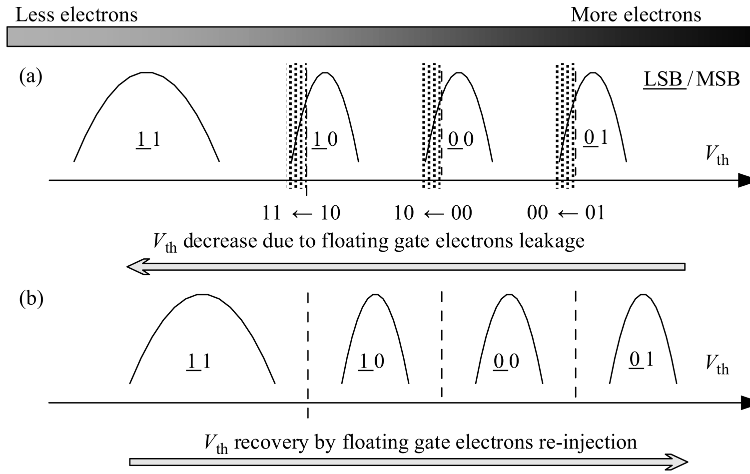


Figure 9 $V_{\rm th}$ distribution after (a) retention and (b) retention error recovery.

3 Proposed retention error recovery scheme

3.1 Retention error recovery basic

Retention errors are mainly caused by floating gate electron leakage during retention. Electrons trapped in floating gate have a small probability to dissipate. During long retention time, the slight leakage of floating gate electrons accumulates a significantly cell $V_{\rm th}$ drop, and induces serious retention errors. Retention errors can be recovered by electron re-injection and compensating floating gate electron loss during retention as shown in Figure 9.

3.2 Proposed retention error recovery scheme

During data storage, retention errors increase with retention time. When error bit numbers exceed the error-correction capability of ECC module, ECC decoding will fail. During data read, when ECC decoding failure is detected, the proposed LSB page refresh based retention error recovery scheme is triggered. Since retention BER in MSB pages is much higher than in LSB pages, ECC decoding failure is always detected in MSB pages before LSB pages.

As in the proposed scheme, ECC decoding is implemented on all LSB pages in the block to be recovered first, and then the corrected data are rewritten back to corresponding LSB pages respectively. The process can be defined as LSB page refresh.

During LSB page refresh, array voltage schemes are shown in Figure 10(a). Cells with LSB data '1' are biased in program inhabit status as shown in Figure 10(b), while cells with LSB data '0' are biased in program status as shown in Figure 10(c). The high voltage between control gate (CG) and channel induces floating gate electron re-injection and compensates floating gate electron loss during retention time, resulting in retention error recovery.

Cells with LSB data '0' are in 00 or 01 status, and have higher $V_{\rm th}$ than $V_{\text{ref-LSB}}$ as shown in Figure 1. According to the incremental step pulse programming algorithm (ISPP) [23], program voltage schemes stop after the first verification operation, and avoid excessive elections re-injection during a single refresh operation.

LSB page refresh can repeat multiple cycles so as to re-inject enough electrons to compensate floating gate electron leakage during retention. Data retention errors are gradually recovered as the increasing of the applied LSB page refresh operation cycles. After every several cycles of LSB page refresh operation are applied, ECC should be performed again to the data with reduced retention errors. If ECC succeeds, data are correctly recovered, otherwise, LSB page refresh operation will continue. The strategy will be stopped when the cycles of LSB page refresh operation reach the per-setting limits, and then the data should be labeled as failed.

Figure 10 (a) Array bias condition in LSB refresh; (b) bias condition in cells with LSB data ‘1’; (c) bias conditions in cells with LSB data ‘0’.

Figure 11 Array and cell bias conditions in (a) RD and (b) WPD scheme.

Read disturbance (RD) and word line program disturbance (WPD) based retention error recovery scheme has also been reported [8–11].

In RD based scheme [8–10], all LSB and MSB pages are read out sequentially and all cells are biased in read status as shown in Figure 11(a). The voltage between CG and channel induces read disturbance (RD) and achieves extra floating gate electron re-injection. As the voltage is typically less than 4 V in RD scheme, the floating gate electron re-injection is inefficient, and to achieve effective retention error recovery, a large number of read operation cycles are indispensable.

In WPD based scheme [11], all ‘1’ data are written to LSB pages in the block to be recovered and cells are biased in program inhabit status as shown in Figure 11(b). The voltage between CG and channel induces word line program disturbance (WPD) and achieves extra floating gate electron re-injection. During WPD write operation, array voltage schemes can induce markedly electron re-injection in 11 status due to high voltage between control gate and channel as shown in Figure 11(b), and 10→11 errors can be effectively recovered. However, as to 00→10 errors, high floating gate electron density in 00 and 01 state cells causes low electron re-injection efficiency.

The proposed LSB page refresh based retention error recovery scheme presents higher recovery voltage in 00 and 01 state cells as shown in Figure 10(c), and presents higher recovery efficiency which results in less operation cycles and latency demands.

4 Results and discussion

The proposed LSB page refresh based retention error recovery schemes is applied on 2x-nm MLC NAND Flash memory chip. For comparison, RD and WPD based schemes are also applied. As in the experiment, the data BER are measured after every 10 operation cycles applied. Figure 12 compares the normalized retention BER reduction with RD, WPD and the proposed schemes. For 3000 to 6000 P/E cycled blocks after 3-year retention, the proposed scheme achieves 78%, 81%, 83% and 84% retention BER reduction with 70, 90, 100 and 120 refresh operation cycles.

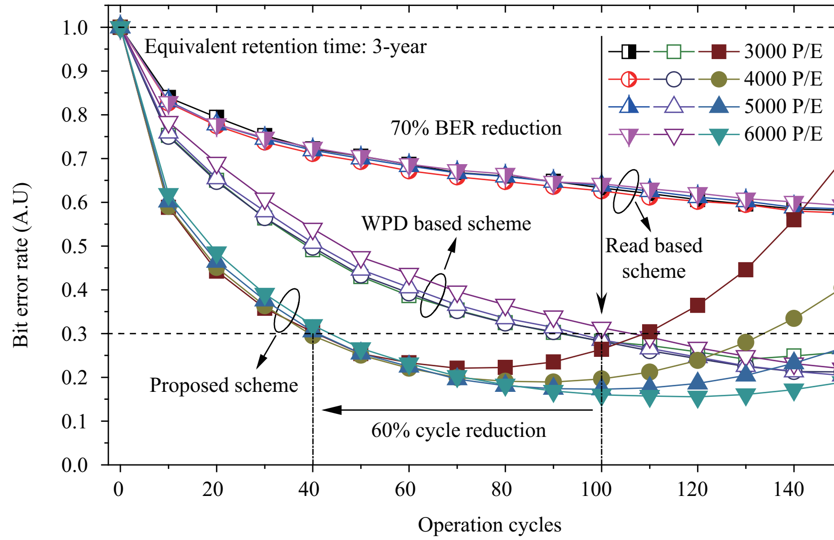


Figure 12 (Color online) Array and cell bias conditions in (a) RD and (b) WPD scheme.

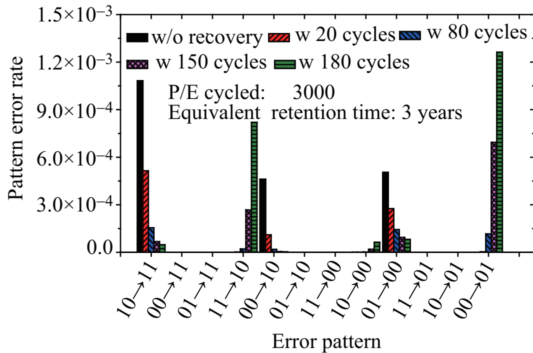


Figure 13 (Color online) Error pattern distributions versus operation cycles.

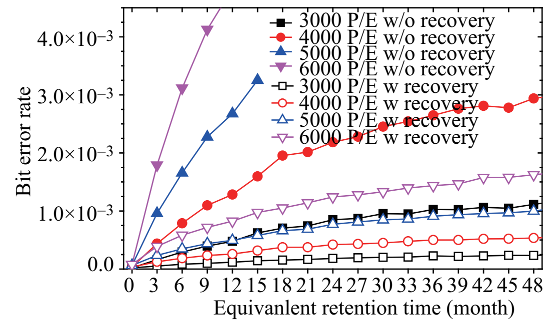


Figure 14 (Color online) Retention BER reduction with optimal LSB page refresh cycles.

Both WPD based and the proposed scheme present higher retention error recovery efficiency than RD based scheme. However, the proposed LSB page refresh based scheme achieves 70% retention BER reduction with 40 operation cycles, while WPD based scheme demands 100 operation cycles, indicating 2.5 times recovery efficient promotion and 60% latency reduction. In addition, it should be noted that excess LSB page refresh cycles will cause BER increase.

Figure 13 exhibits error pattern distribution variations with LSB page refresh cycles. Before retention error recovery, the predominant error patterns are 10→11, 00→10 and 01→00 and corresponding pattern error rates are 1.08×10^{-3}, 4.62×10^{-4} and 5.04×10^{-4}, respectively. After 20 LSB page refresh cycles, the corresponding pattern error rates decrease by 52.5%, 76.1% and 45.3% due to floating gate electron compensation. As the number of LSB page refresh cycles increases, 10→11, 00→10 and 01→00 errors present a continued momentum of reduction. However, program error patterns such as 11→10, 10→00 and 00→01 begin to increase. After 180 LSB page refresh cycles, nearly all 10→11, 00→10 and 01→00 errors have been recovered, however, 11→10 and 00→01 pattern errors increase from nearly 0 up to 8.2×10^{-4} and 1.26×10^{-3}. Retention error recovery and program error generation can be explained by floating gate electron injection during LSB page refresh, and program error generation will ultimately result in total BER increases as discussed in Figure 12. So the applied cycles of LSB refresh should be optimized to achieve the best tradeoff between retention error recovery and program error generation, and realize maximum retention BER reduction.

During experiment, block retention BER is measured after every 10 LSB page refresh cycles applied. The lowest BER achieved by the proposed scheme is shown in Figure 14, and the corresponding optimal

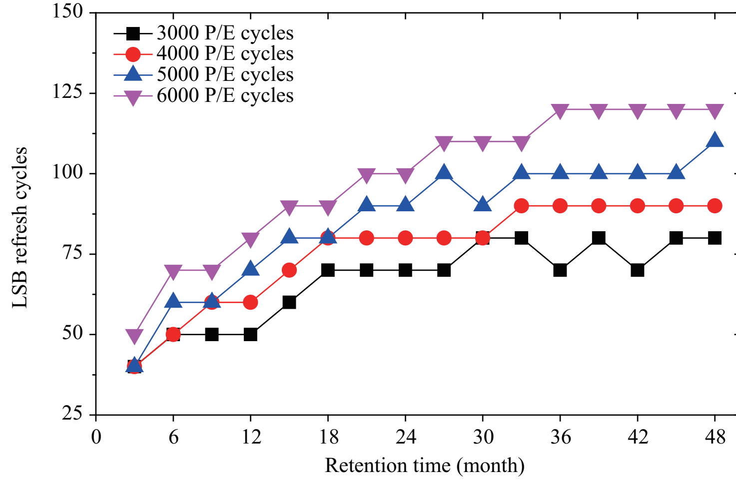


Figure 15 (Color online) Optimal LSB page refresh cycles versus P/E cycles and retention time.

Retention time (month)	w/o recovery				WPD scheme				This work			
	3000	4000	5000	6000	3000	4000	5000	6000	3000	4000	5000	6000
0	P	P	P	P	P	P	P	P	P	P	P	P
3	P	P	F	F	P	P	P	F	P	P	P	F
6	P	F	F	F	P	P	F	F	P	P	F	F
9	P	F	F	F	P	F	F	F	P	P	F	F
12	P	F	F	F	P	F	F	F	P	P	F	F
15	P	F	F	F	P	F	F	F	P	F	F	F
18	F	F	F	F	P	F	F	F	P	F	F	F
21	F	F	F	F	P	F	F	F	P	F	F	F
24	F	F	F	F	P	F	F	F	P	F	F	F
27	F	F	F	F	P	F	F	F	P	F	F	F
30	F	F	F	F	P	F	F	F	P	F	F	F
33	F	F	F	F	P	F	F	F	P	F	F	F
36	F	F	F	F	P	F	F	F	P	F	F	F
39	F	F	F	F	F	F	F	F	P	F	F	F
42	F	F	F	F	F	F	F	F	P	F	F	F
45	F	F	F	F	F	F	F	F	P	F	F	F
48	F	F	F	F	F	F	F	F	P	F	F	F
52	F	F	F	F	F	F	F	F	P	F	F	F
56	F	F	F	F	F	F	F	F	P	F	F	F
60	F	F	F	F	F	F	F	F	P	F	F	F

(a)

Retention time (month)	w/o recovery				WPD scheme				This work			
	3000	4000	5000	6000	3000	4000	5000	6000	3000	4000	5000	6000
0	P	P	P	P	P	P	P	P	P	P	P	P
3	P	P	P	F	P	P	P	P	P	P	P	P
6	P	P	F	F	P	P	P	F	P	P	P	F
9	P	P	F	F	P	P	F	F	P	P	P	F
12	P	P	F	F	P	P	F	F	P	P	F	F
15	P	F	F	F	P	F	F	F	P	P	F	F
18	P	F	F	F	P	F	F	F	P	P	F	F
21	P	F	F	F	P	F	F	F	P	P	F	F
24	P	F	F	F	P	F	F	F	P	P	F	F
27	P	F	F	F	P	F	F	F	P	F	F	F
30	P	F	F	F	P	F	F	F	P	F	F	F
33	P	F	F	F	P	F	F	F	P	F	F	F
36	P	F	F	F	P	F	F	F	P	F	F	F
39	P	F	F	F	P	F	F	F	P	F	F	F
42	P	F	F	F	P	F	F	F	P	F	F	F
45	P	F	F	F	P	F	F	F	P	F	F	F
48	P	F	F	F	P	F	F	F	P	F	F	F
52	P	F	F	F	P	F	F	F	P	F	F	F
56	P	F	F	F	P	F	F	F	P	F	F	F
60	P	F	F	F	P	F	F	F	P	F	F	F

(b)

P Pass F Fail

Figure 16 ECC results with (a) 24-bit and (b) 40-bit BCH code.

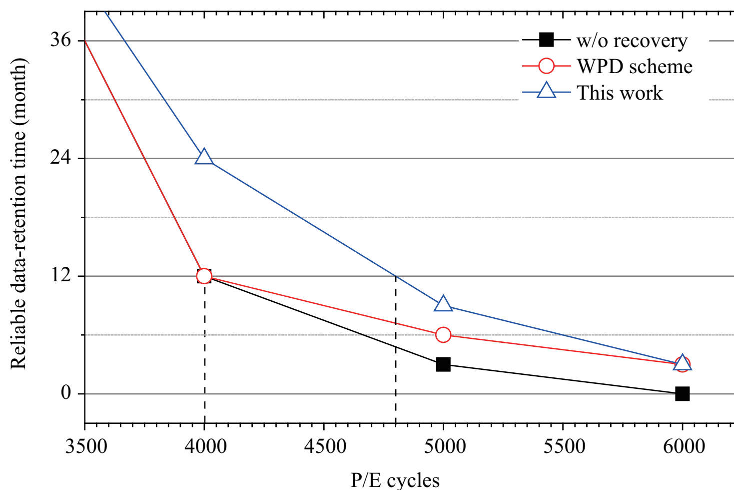


Figure 17 (Color online) Reliable retention time with 40-bit BCH code.

operation cycles are shown in Figure 15.

The experiment result exhibits a significant reduction in retention BER. With the proposed scheme, blocks with 5000 P/E cycles present lower retention BER than 3000 P/E cycled blocks without recovery scheme, indicating 67% device lifetime extension.

As floating gate electron leakage is more serious in blocks experienced high P/E cycles and long retention time, the optimal cycles increase with P/E cycles and retention time as shown in Figure 15. Besides, the slight fluctuation of optimal cycles may be caused by the erratic tunneling due to random thermal noise (RTN) [24].

Figure 16 exhibits the BCH ECC results with and without retention error recovery. The error-correction capacity of BCH code is set to conventional 24-bit and 40-bit. To limit the system latency time, recovery schemes are limited to 20 operation cycles.

From the viewpoint of reliable data-retention time, 24-bit BCH with the proposed LSB page refresh scheme exhibits the same retention reliability with 40-bit BCH without retention error recovery. The retention reliability improvement by the proposed scheme results in 40% ECC error-correction capability relaxation, indicating lower hardware overhead and spare bits cost.

Figure 17 compares the reliable retention time with 40-bit BCH ECC. For conventionally required data retention time of 1 year, compared with WPD based scheme and without recovery, the proposed scheme extends the P/E cycle time from 4000 to 4800, achieving 20% device endurance extension.

5 Conclusion

In this paper, an LSB page refresh based retention error recovery scheme is proposed to improve the retention reliability issue of highly scaled MLC NAND Flash. The proposed scheme realizes retention error rate reduction by compensating floating gate electron leakage during data retention and floating gate electron compensating is realized by LSB page refresh. The proposed scheme is applied on 2x-nm MLC NAND Flash. For 3000 to 6000 P/E cycled blocks after 3-year retention, the proposed scheme achieves 78%, 81%, 83% and 84% retention BER reduction. Compared with reported RD and WPD based scheme, the proposed scheme presents 2.5 times recovery efficient promotion and 60% operation latency reduction. From the viewpoint of reliable data-retention time, the improvement on retention reliability and recovery efficiency implies 20% device endurance extension or 40% ECC error-correction capability relaxation.

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Conflict of interest The authors declare that they have no conflict of interest.

References

1 Choi S, Kim D, Choi S, et al. 19.2 A 93.4 mm^2 64 GB MLC NAND-flash memory with 16 nm CMOS technology. In: IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC). San Francisco: IEEE, 2014. 328–329
2 Helm M, Park J K, Ghalam A, et al. 19.1 A 128 Gb MLC NAND-flash device using 16 nm planar cell. In: IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC). San Francisco: IEEE, 2014. 326–327
3 Koh Y. NAND flash scaling beyond 20 nm. In: IEEE International Memory Workshop, IMW'09. Monterey: IEEE, 2009. 1–3
4 Yoon J H, Tressler G A. Advanced flash technology status, scaling trends & implications to enterprise SSD technology enablement. In: Flash Memory Summit, Santa Clara, 2012
5 Kang D, Lee K, Seo S, et al. Generation dependence of retention characteristics in extremely scaled NAND flash memory. IEEE Electron Device Lett, 2013, 34: 1139–1141
6 Ho K C, Fang P C, Li H P, et al. A 45 nm 6b/cell charge-trapping flash memory using LDPC-based ECC and drift-immune soft-sensing engine. In: IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC). San Francisco: IEEE, 2013. 222–223
7 Dong G, Xie N, Zhang T. Enabling NAND Flash memory use soft-decision error correction codes at minimal read latency overhead. IEEE Trans Circuits Syst I Regular Papers, 2013, 60: 2412–2421
8 Tanakamaru S, Yanagihara Y, Takeuchi K. Over-10x-Extended-Lifetime 76%-Reduced-Error Solid-State Drives (SSDs) with Error-Prediction LDPC Architecture and Error-Recovery Scheme (Invited Talk). Technical Report Ieice Icd, 2012, 112: 23–28
9 Tanakamaru S, Yanagihara Y, Takeuchi K. Error-prediction LDPC and error-recovery schemes for highly reliable solid-state crives (SSDs). IEEE J Solid-State Circ, 2013, 48: 2920–2933
10 Tanakamaru S, Doi M, Takeuchi K. Error-prediction analyses in 1X, 2X and 3X nm NAND flash memories for system-level reliability improvement of solid-state drives (SSDs). In: IEEE International Reliability Physics Symposium (IRPS). Anaheim: IEEE, 2013. 3B.3.1–3B.3.6
11 Ma H, Zou H, Pan L, et al. MLC nand flash retention error recovery scheme through word line program disturbance. In: International Symposium on Next-Generation Electronics (ISNE). Kwei-Shan: IEEE, 2014. 1–2
12 Micheloni R, Marelli A, Commodaro S. NAND overview: from memory to systems. In: Micheloni R, Crippa L, Marelli A, eds. Inside NAND Flash Memories. New York: Spinger, 2010. 19–53
13 JEDEC Solid State Technology Association. Stress-test-driven qualification of integrated circuits. JESD47G. http://www.jedec.org/. 2010
14 Olivo P, Ricco B, Sangiorgi E. High-field-induced voltage-dependent oxide charge. Appl Phys Lett, 1986, 48: 1135–1137
15 Cappelletti P, Bez R, Cantarelli D, et al. Failure mechanisms of flash cell in program/erase cycling. In: International Electron Devices Meeting IEDM'94 Technical Digest. San Francisco: IEEE, 1994. 291–294
16 Cai Y, Haratsch E F, Mutlu O, et al. Error patterns in MLC NAND flash memory: measurement, characterization, and analysis. In: Design, Automation and Test in Europe Conference and Exhibition (DATE). Dresden: IEEE, 2012. 521–526
17 Dong G, Pan Y, Xie N, et al. Estimating information-theoretical nand flash memory storage capacity and its implication to memory system design space exploration. IEEE Trans Very Large Scale Integration Syst, 2012, 20: 1705–1714
18 Satoh S, Hagiwara H, Tanzawa T, et al. A novel isolation-scaling technology for NAND EEPROMs with the minimized program disturbance. In: International Electron Devices Meeting IEDM'97 Technical Digest. Washington: IEEE, 1997. 291–294
19 Lee D, Hur H, Choi D. Effects of floating-gate interference on NAND flash memory cell operation. IEEE Electron Device Lett, 2002, 23: 264–266
20 Monzio Compagnoni C, Spinelli A S, Gusmeroli R, et al. Ultimate accuracy for the nand flash program algorithm due to the electron injection statistics. IEEE Trans Electron Devices, 2008, 55: 2695–2702
21 Lee J D, Choi J H, Park D, et al. Data retention characteristics of sub-100 nm NAND flash memory cells. IEEE Electron Device Lett, 2004, 24: 748–750
22 Papadas C, Pananakakis G, Ghibaudo G, et al. Modeling of the intrinsic retention characteristics of FLOTOX EEPROM cells under elevated temperature conditions. IEEE Trans Electron Devices, 1995, 42: 678–682
23 Choi Y J, Suh K D, Koh Y N, et al. A high speed programming scheme for multi-level NAND flash memory. In: IEEE Symposium on VLSI Circuits Digest of Technical Papers, Honolulu, 1996. 170–171
24 Miki H, Osabe T, Tega N, et al. Quantitative analysis of random telegraph signals as fluctuations of threshold voltages in scaled flash memory cells. In: Proceedings of 45th Annual IEEE International Reliability Physics Symposium. Phoenix: IEEE, 2007. 29–35