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Ultralow-power high-speed flip-flop based on multimode FinFETs

Kai LIAO[1], Xiaoxin CUI[1]*, Nan LIAO[1], Tian WANG[1], Dunshan YU[1] & Xiaole CUI[2]*

[1]*Institute of Microelectronics, Peking University, Beijing* 100871*, China;*
[2]*Key Laboratory of Integrated Microsystems, Shenzhen Graduate School, Peking University, Shenzhen* 518055*, China*

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Abstract In this paper, we first reconstruct a novel planar static contention-free single-phase-clocked flip-flop (S^2CFF) based on high-performance fin-type field-effect transistors (FinFETs) to achieve high speed and ultralow power consumption. Benefiting from better control of the conductive channel, the shorted-gate (SG-mode) FinFET flip-flop obtains a persistent reduction of 56.7% in average power consumption as well as a considerable improvement in timing performance at a typical 10% data switching activity, while the low-power (LP-mode) FinFET flip-flop promotes the power reduction to 61.8% without appreciable degradation in speed. However, through further analysis of the simulation results, we have revealed an unnecessary energy loss caused by the redundant leaps of internal nodes at the static input '0', which has a noticeable negative impact on total power consumption at low data switching activity. In order to overcome this defect, a conditional precharge technique is introduced to control the charging path, and we demonstrate that the independent-gate (IG-mode) FinFET is the best option for the added control transistor. The verification results indicate that our optimization reduces the power consumption by more than 50% at low data switching activity with an acceptable area and setup time penalty compared with that of LP-mode FinFET flip-flop.

Keywords multimode FinFET, flip-flop, ultralow-power, high-speed, high-performance

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1 Introduction

Flip-flops are considered one of the most essential memory types in the vast majority of digital integrated circuits (ICs), and thus, it is extensively utilized in very large scale integration (VLSI). Under the current circumstances, especially where high-density pipeline technology is frequently used, large numbers of flip-flops have become indispensable components [1,2]. Previous researches have found that the timing performance (including set-up time, hold time, and clock-to-output delay) of flip-flops has a direct effect on the clock frequency of digital circuit systems, and these irreplaceable flip-flops also generally consume 30%–50% of the power dissipation of the entire chip [3, 4]. Thus, high-performance flip-flops with the

* Corresponding author (email: cuixx@pku.edu.cn, cuixl@pkusz.edu.cn)

advantages of fast speed and ultralow power consumption have been a popular research topic, and numerous different types of flip-flops have been invented and investigated over the past decades [5–9]. Recently, a static contention-free single-phase-clocked (SPC) flip-flop (S^2CFF) with low-power consumption has been presented in [10] by Kim et al., which to our knowledge is one of the best edge-trigged flip-flops implemented by traditional planar MOSFET technology in the literature.

It is well known that the total power dissipation can be divided into three major parts: dynamic power dissipation, static power dissipation, and short-circuit power dissipation. However, with the technology scaling down, leakage power consumption has become an increasingly important part of the total power consumption. Since the states of flip-flops only switch at the rising edges of the clock signal and remain the same at other times in the clock period, this inherent trend could be an unpleasant restriction for advanced flip-flops to further reduce the power consumption. To solve this problem, several novel multigate devices aiming at implementing ultralow leakage current have been proposed, such as ultrathin body devices [11], fully depleted silicon on insulator (FDSOI) [12], and fin-type field-effect transistors (FinFETs) [13]. So far, FinFET seems to be the most promising option because of its superior electrical properties and timing performance, and commercial chips based on FinFETs have already been released by Intel, TSMC, and other global foundries.

In this article, we chose the original S^2CFF based on planar MOSFET as our research object and reconstructed it with FinFETs to achieve high speed and ultralow power consumption. At the same time, we discovered an intrinsic defect (unnecessary energy loss) of S^2CFF by analyzing the simulation results and proposed an improvement approach by utilizing the excellent design flexibility of multimode FinFET. The verification results show that the multimode FinFET flip-flop offers a good solution for the discovered defect, and the additional penalty on timing performance is acceptable.

2 FinFET devices

With the scaling down of transistor conductive channels, short-channel effects (SCEs) become intolerable, and many multigate devices have been proposed to overcome SCEs. Due to its relatively simple manufacturing process and good compatibility with bulk CMOS, FinFET is considered to be the most feasible new multigate device. Through the stronger control of the conductive channel by the double gate (front gate and back gate), the FinFET device has the advantages of higher on-state current, lower off-state current, and faster switching speed [14, 15].

Furthermore, according to whether the front gate and back gate are tied together or not, FinFET circuits can be divided into three different operating modes, namely, shorted-gate (SG-mode), low-power (LP-mode), and independent-gate (IG-mode) [16]. Different circuit operating modes have different characteristics, which increases the design flexibility. For example, the SG-mode FinFET has high on-state current and fast switching speed to achieve high performance, while the LP-mode FinFET has low off-state current to reduce the leakage power dissipation. Figure 1(a) and (b) illustrate the three-dimensional diagram and cross-sectional top view of a FinFET transistor, and Figure 1(c) shows the electrical model schematic of the three operating modes of N-FinFETs and P-FinFETs, respectively.

In our study, the simulations are based on the predictive technology model (PTM) for 32-nm FinFETs [17]. PTM is a theoretical mode that ignores the actual process parameters. It covers sufficient physical effects, and excellent scalability of PTM across process and design conditions has been shown in the published results. Considering there is no FinFET Spice model officially offered by foundries, PTM was selected for our study without loss of generality. The primary parameters of the devices are listed in Table 1, which are typical for manufactured 32-nm FinFETs. The parameter $L_{\rm gate}$ denotes the length of the gate, while $H_{\rm fin}$ and $W_{\rm fin}$ denote the height and width of the silicon fin, respectively. For a common SG-mode FinFET, the equivalent gate width $W_{\rm gate}$ can be calculated by

$$W_{\rm gate} = 2 \times H_{\rm fin} + W_{\rm fin}. \tag{1}$$

Note that, $W_{\rm fin}$ is usually much smaller than $H_{\rm fin}$, and for LP- and IG-mode FinFETs, $W_{\rm fin}$ is eliminated because the top silicon of the gate is polished to separate the double gates. In addition, the thickness of

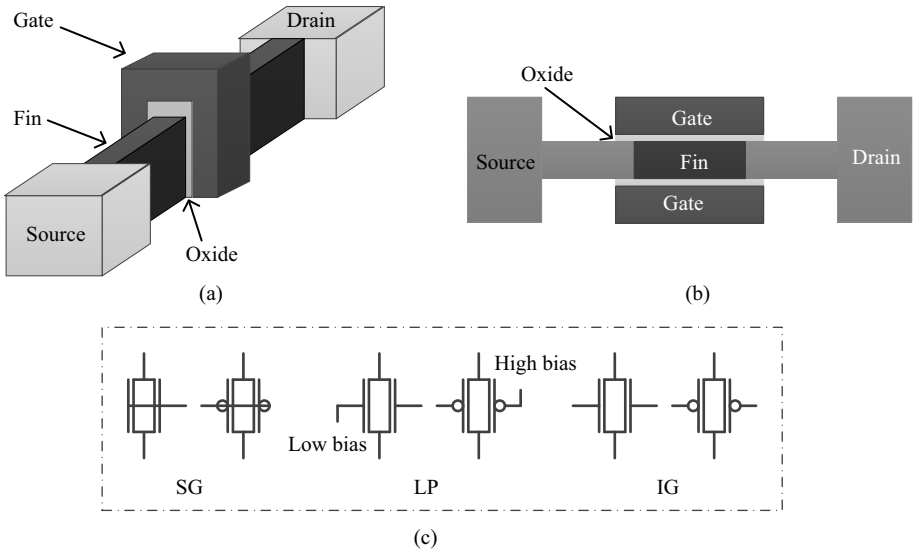

Figure 1 FinFET model and schematic. (a) Three-dimensional structure, (b) cross sectional top view, and (c) electrical model schematic.

Table 1 Primary parameters in PTM

Device	Primary parameters				
N-type FinFET	$L_{\rm gate} = 32$ nm	$H_{\rm fin} = 40$ nm	$W_{\rm fin} = 8.6$ nm	$T_{ox} = 1.4$ nm	$V_{DD} = 1$ V
P-type FinFET	$L_{\rm gate} = 32$ nm	$H_{\rm fin} = 40$ nm	$W_{\rm fin} = 8.6$ nm	$T_{ox} = 1.4$ nm	$V_{DD} = 1$ V

the silicon dioxide layer (T_{ox}) is fixed to 1.4 nm and the normal operating voltage (V_{DD}) of the devices is set to be 1 V.

Simulations that compare the different modes of FinFET operations are implemented. Figure 2(a) shows the transfer characteristic curve of the three operating modes 32-nm N-FinFET based on PTM (the equivalent gate width is 80 nm). The supply voltage is 1.0 V, and the reverse bias voltage of the LP-mode N-FinFET is set to be -0.2 V (1.2 V for the LP-mode P-FinFET). The results indicate that the leakage current of the LP-mode N-FinFET is almost 20 times lower than that of the SG-mode N-FinFET at the cost of halving the on-state current. The LP-mode P-FinFET can also be verified to have the similar properties. Therefore, we can use an LP-mode FinFET to substitute for an SG-mode FinFET in a noncritical path to reduce the power dissipation without degrading the timing performance.

The determination of the reverse bias voltage is based on the fact that the coupling of the back gate to front gate is observed only in the weak inversion region of operation. In the region of strong inversion, the presence of inversion charge in the channel shields the FinFET gates from each other and no coupling is observed. A generalized model for the relationship between the threshold voltage ($V_{\rm th}$) at the front gate (gf) of a FinFET and the voltage applied to its back gate (gb) is derived as follows [18]:

$$V_{\rm thgf} \approx \begin{cases} V^0_{\rm thgf} - \delta \cdot (V_{\rm gbs} - V_{\rm thgb}), & \text{if } V_{\rm gbs} < V_{\rm thgb}, \\ V^0_{\rm thgf}, & \text{other situations}, \end{cases} \tag{2}$$

where $V_{\rm gbs}$ denotes the voltage at the source terminal of the FinFET, δ is a positive value determined by the ratio of gate and body capacitances, $V_{\rm thgf}$ and $V_{\rm thgb}$ are the threshold voltage of the front gate and back gate respectively, and $V^0_{\rm thgf}$ is the minimum observed $V_{\rm thgf}$. The above equation is given for an N-type FinFET, but may also be used for a P-type FinFET with the usual changes in sign. According to the basic transistor properties, the threshold voltage increase will result in an exponential decrease of leakage power dissipation. However, on the other hand, it will also make the propagation delay ($t_{\rm pd}$) grow gradually as approximately given by [19]

$$t_{\rm pd} = \frac{\rm k \cdot C_L \cdot V_{DD}}{(V_{DD} - V_{\rm th})^{\alpha}}, \tag{3}$$

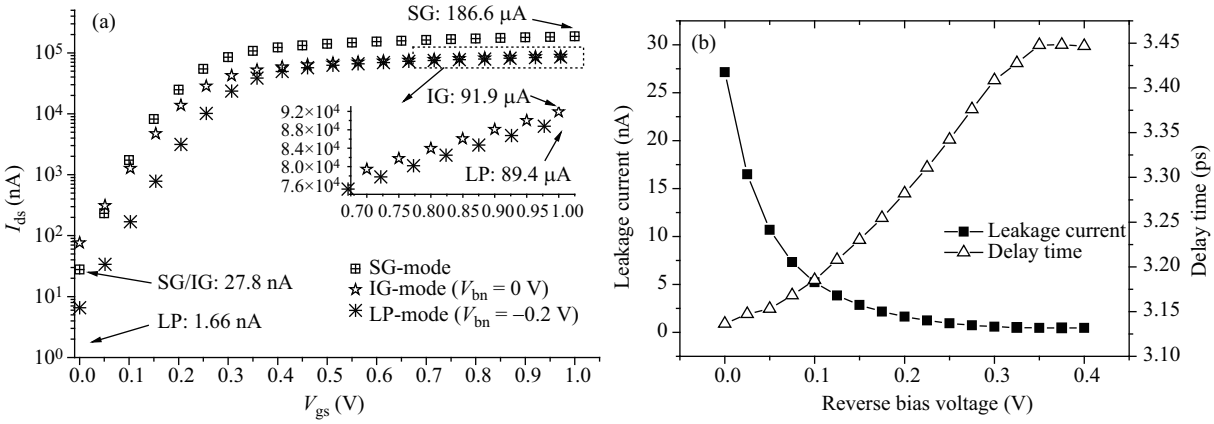

Figure 2 Simulation results. (a) Transfer characteristic curve of the 32-nm N-FinFET based on PTM and (b) the delay and leakage variation of an LP-mode FinFET inverter.

where α is typically 1.3 and k is a constant. Therefore, it is necessary to find an appropriate reverse bias to balance the leakage and delay. An LP-mode FinFET inverter whose pull-up and pull-down path were both driven by a back gate bias of equal strength was simulated, as shown in Figure 2(b). Note that, since the carrier mobility of the N-FinFET is twice as high as that of the P-FinFET, the pull-up path consists of a pair of parallel P-FinFETs to equilibrate the transmission characteristic curve of the inverter. Simulation results show that increasing the reverse bias will lead to an exponential decline of leakage current, while the delay grows near-linearly. It can be seen that the leakage curve displays an initial sharp decrease, but flattens out when the reverse bias exceeds 0.2 V. Further increasing the reverse-bias can only lead to delay overheads without much corresponding saving in leakage. Hence, 0.2 V would be the most suitable value for the reverse bias, which would be set as the reverse bias voltage (-0.2 V for N-FinFET and 1.2 V for P-FinFET) in our simulations.

3 Circuit description

As mentioned previously, the SG-mode FinFET has better electrical properties than a planar MOSFET and it is also the simplest and most common operating mode in FinFET circuits. Therefore, we first reconstruct the original S^{2}CFF based on SG-mode FinFETs. Figure 3 shows the circuit diagram of S^{2}CFF based on SG-mode FinFETs and the input/output signals and key nodes are marked with black boldface letters. In this version, the underlying planar MOSFETs in S^{2}CFF circuit are directly substituted by SG-mode FinFETs to improve the timing performance and reduce the power consumption. Based on the operating principle of S^{2}CFF, node Y will be precharged to a high level at the low level of the clock signal. Because node X is the inverted signal of the input signal D, node Y will be re-evaluated at the rising edge of the clock signal. As a result, node Qb can obtain the correct logical value through transistors M13, M14, and M15 controlled by signals Y and Xb. Finally, the last inverter, consisting of transistors M23 and M24, generates the output signal Q and ensures sufficient driving capability. Other transistors (such as M8, M9, M10, M18, and M19, etc.) employ the feedback technology to stabilize the voltage level of the corresponding nodes and enhance the robustness of the entire circuit. Moreover, according to the depiction in Kim's paper [10], S^{2}CFF also has the advantage of a fully static and contention-free operating mode, and readers may find more details in the original paper. Obviously, due to the intrinsic superior electrical properties of the SG-mode FinFET, the substitution will maintain the inherent features of S^{2}CFF and the expected design goal can also be achieved without any doubt.

Furthermore, considering that the forced stack transistor is an effective method to reduce the leakage current [20,21]. According to [22], for forced-stack N-FinFETs, assuming $I_{\mathrm{off},M\mathrm{up}}$ is the off-state current of the up N-FinFET, and $I_{\mathrm{off},M\mathrm{down}}$ is that for the down N-FinFET, the leakage current in the stack can

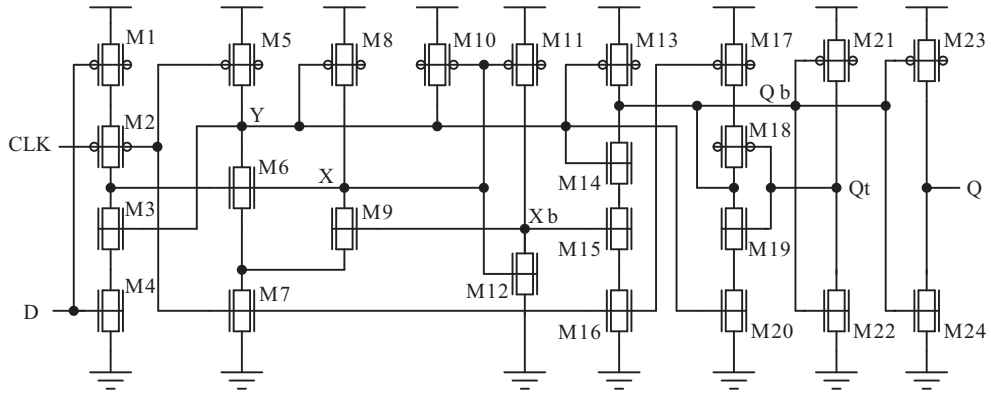

Figure 3 Circuit diagram of the S^{2}CFF based on SG-mode FinFETs.

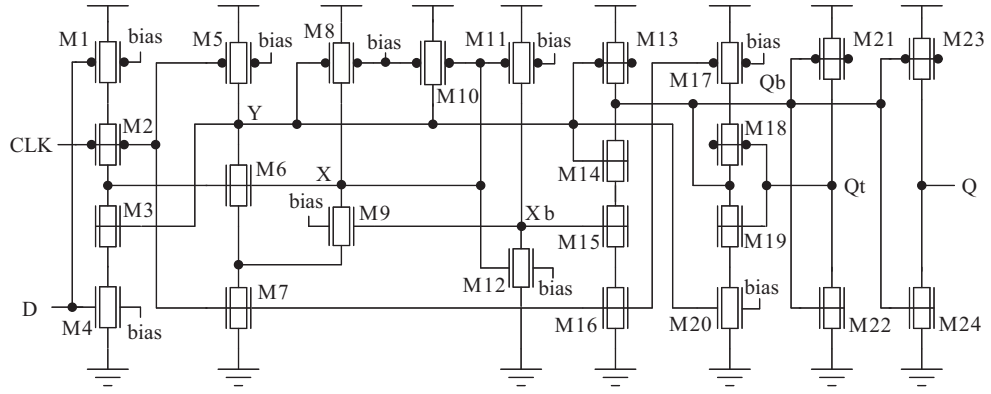

Figure 4 Circuit diagram of the S^{2}CFF based on LP-mode FinFETs.

be expressed as

$$I_{\text{stack}} = I_{\text{off},M\text{up}}^{\alpha} \cdot I_{\text{off},M\text{up}}^{1-\alpha} \cdot 10^{\alpha k}, \tag{4}$$

where α and k are technology-dependent parameters and α is certainly much lower than 1. Since $\alpha \ll 1$, as a result, the leakage current of forced-stack N-FinFETs is dominated by the off-state current of the stacked transistor near the ground. Similarly, for P-FinFETs, the stacked transistor near the power supply is decisive. Based on the above principle, the corresponding transistors of the flip-flop in Figure 3 (not in critical paths) are quite suitable for LP-mode FinFETs. Note that the transistors in critical paths maintain SG-mode FinFETs to provide sufficient on-state current for charging and discharging processes. Thus, this substitution can tremendously reduce the leakage power dissipation without too much degradation of timing performance. As for the area penalty caused by the usage of LP-mode FinFETs, it mainly comes from the extra requirement of the fin pitch to accommodate for separate contacts of the front and back gates [23]. However, as declared in [23], the circuits with mixed SG- and LP-mode FinFETs exhibit an almost equally good layout density compared with the pure SG-mode FinFET circuits. Thus, in our work, we assume that the area penalty of the proposed S^{2}CFF based on LP-mode FinFETs in Figure 4 is acceptable. Another consideration is that we have to design extra circuitry to deal with the bias voltage. However, this problem can be solved in a systematic view [24], and the additional resource consumption is acceptable compared with the scale of the entire system. Figure 4 presents the circuit diagram of the S^{2}CFF based on LP-mode FinFETs, and the gates connecting the bias voltage (for LP-mode FinFETs) are clearly marked with the word 'bias'.

4 Simulation results and analysis

To verify the improvement of SG-mode and LP-mode FinFET flip-flops relative to the planar MOSFET flip-flop, detailed simulations were conducted, followed by thorough analysis. In our work, all simulations

Table 2 Measured timing parameters of three types of flip-flops

Circuit type	Setup time (ps)		Hold time (ps)		Clock to Q delay (ps)	
	Rise	Fall	Rise	Fall	Rise	Fall
Planar MOSFET	2.44	31.14	1.57	−30.10	15.60	26.23
SG-mode FinFET	8.14	12.84	−4.42	−11.80	6.51	7.59
LP-mode FinFET	10.68	12.62	−7.33	−11.56	6.40	6.84

Table 3 Measured detailed power consumption of static inputs of three types of flip-flops

Circuit type	Node Y (μW)		Other nodes (μW)		Total power (μW)	
	Static '0'	Static '1'	Static '0'	Static '1'	Static '0'	Static '1'
Planar MOSFET	2.391	0.647	0.996	1.157	3.387	1.806
SG-mode FinFET	1.483	0.111	0.279	0.451	1.762	0.561
LP-mode FinFET	1.106	0.110	0.210	0.363	1.316	0.472

are based on the HSPICE tool, and the on-state currents of the corresponding (in the same location of both circuits) SG-mode FinFET and planar MOSFET (N-type and P-type, respectively) were set to be identical by adjusting the gate's width-to-length ratio to ensure a valid comparison. In the meantime, to increase the reliability of the simulation results, the sizes of all transistors were optimized aiming for the best power-delay-product (PDP). The initialized input signals are transmitted by buffers before they are sent to the flip-flops in order to simulate the real situation, and the output load capacitance is equivalent to the input capacitance of four standard inverters.

The measured average power consumption of the three types of S^2CFF circuits against different data switching activities is presented in Figure 5. As mentioned before, the LP-mode FinFET flip-flop dissipates the least power within the entire range of data switching activity, while the SG-mode FinFET flip-flop falls between the other two flip-flops. For a 10% data switching activity ratio (also the typical value in general digital systems), the reductions of SG-mode FinFET and LP-mode FinFET flip-flops compared with the planar MOSFET flip-flop are 56.7% and 61.8%, respectively. At the same time, Table 2 lists some measured important timing parameters for these three flip-flops. From Table 2, we can see that the SG-mode FinFET and LP-mode FinFET flip-flops also exhibit considerable improvement in circuit speed at the worst cases relative to the planar MOSFET flip-flop.

However, through in-depth study on the operating process of the original S^2CFF, we find that it suffers a serious drawback which sharply weakens its low-power advantage in the domain of low data switching activity. Note that node Y will be charged at the precharge stage (clock signal is at low voltage) and then will be discharged if the input signal D is '0' at the evaluation stage (clock signal is in high voltage). From another perspective, node Y keeps being unnecessarily charged and discharged in every clock period when the input D maintains a static low voltage (i.e. 0% activity ratio). These redundant leaps lead to superfluous energy loss, which can be seen clearly in Figure 5. On the contrary, the circuit remains in a low-power state when the static input D is '1' since node Y will not be discharged.

Table 3 lists the detailed simulation results of the flip-flops in the condition of static input '1' and '0'. The data in Table 3 reveal that node Y consumes extremely larger power consumption at static input '0', but slightly smaller power consumption at static input '1' than other nodes regardless of the underlying transistor type. As a consequence, static input '0' has an unacceptable total power consumption (especially for the LP-mode FinFET flip-flop) compared with static input '1'. We note that the total power consumption at static input '0' is even comparable with that of 20% data switching activity ratio. Thus, based on the above analysis, the original S^2CFF ought to be optimized to overcome this drawback.

5 Optimization

In this part, the LP-mode FinFET flip-flop in Figure 4 was optimized to eliminate the extra energy loss caused by redundant leaps. The reason we chose the LP-mode FinFET flip-flop is that it has the

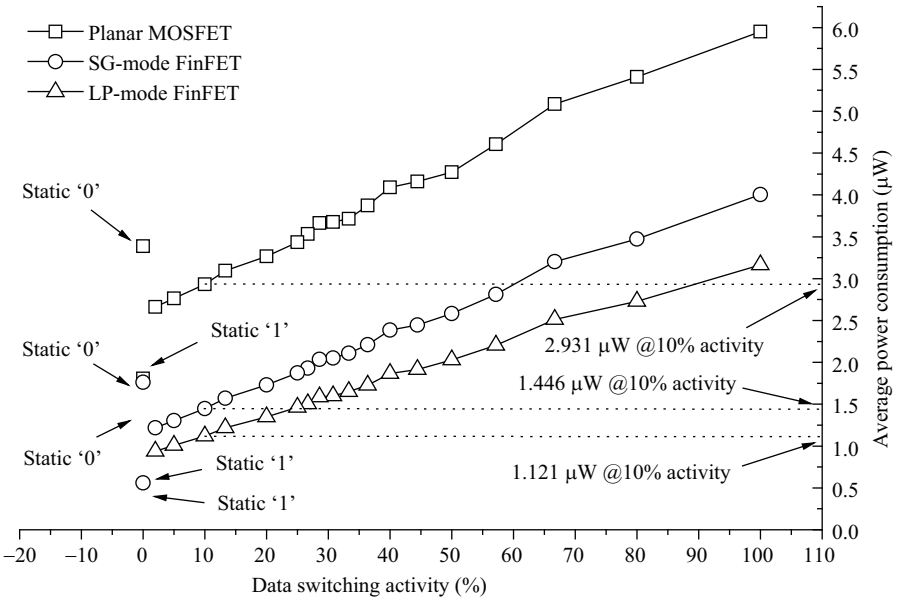

Figure 5 Measured average power consumption against different data switching activity of three types of flip-flops.

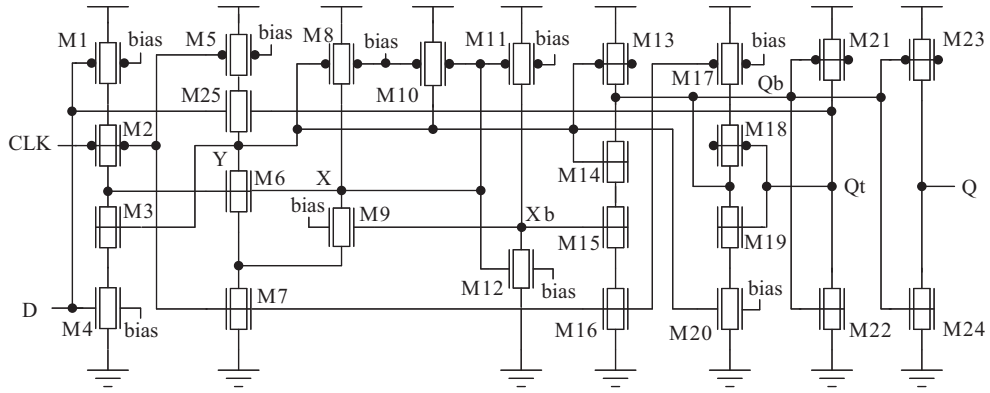

Figure 6 Circuit diagram of the optimized S^{2}CFF based on multimode FinFETs.

best simulation performance among the above three types of flip-flops, which makes the optimization more convincible. On the other hand, we want to make full use of the design flexibility of all operating modes of FinFETs to obtain the best result, including timing performance, power dissipation, and area consumption.

As mentioned before, in Figure 4 it is unnecessary for node Y to be repetitively charged through transistor M5 when the clock signal CLK is at low voltage (i.e., the precharge stage) and the input signal D remains at static '0'. However, considering the stability of other internal nodes in the circuit, there is one exception that if node Qb equals '0' (i.e., the input signal D is '1' in the previous clock period before jumping to static '0'), node Y needs to be charged to high voltage to enable transistor M20 to prevent node Qb from floating; otherwise, the state of the flip-flop may incorrectly reverse.

To settle the problem jointly, two parallel N-FinFETs enabled by the input signal D and internal node Qt (the inverted signal of Qb) respectively should be employed between transistor M5 and node Y to control the charging path. Note that the IG-mode FinFET should be quite suitable in this case since only one transistor is required to achieve the above function. Figure 6 shows the circuit diagram of the optimized S^{2}CFF based on multimode FinFETs, and the transistor M25 implemented by an IG-mode FinFET is highlighted by black bold line.

Although an N-type transistor has threshold loss in the transmission of high voltage as shown in the previous research, the P-FinFET M10 controlled by node X makes up this shortcoming when D is '1'

Table 4 Comparison of measured detailed power consumption of static inputs

Circuit type	Node Y (μW)		Other nodes (μW)		Total power (μW)	
	Static '0'	Static '1'	Static '0'	Static '1'	Static '0'	Static '1'
LP-mode FinFET	1.106	0.110	0.210	0.363	1.316	0.472
Optimized multimode FinFET	0.051	0.110	0.140	0.363	0.191	0.472

Table 5 Comparison of measured timing parameters

Circuit type	Setup time (ps)		Hold time (ps)		Clock to Q delay (ps)	
	Rise	Fall	Rise	Fall	Rise	Fall
LP-mode FinFET	10.68	12.62	−7.33	−11.56	6.40	6.84
Optimized multimode FinFET	37.55	12.72	−34.52	−11.66	6.31	6.82

(i.e., node X is at low voltage) in the precharge stage. Thus, due to the self-coupling, node Y can eventually be charged to supply voltage completely by given some additional time. Obviously, the other LP-mode FinFETs remain the same, and the size of the transistors in critical paths should be fine-tuned to maintain the best PDP for fair comparison.

6 Verification

Simulations under the same configuration have been implemented to verify the optimization, and the comparative simulation results are presented in Tables 4 and 5 respectively. We chose the LP-mode FinFET flip-flop as the reference, and from Table 4, we can clearly see that the optimized multimode FinFET flip-flop not only extremely reduces the power consumption of node Y by a factor of more than twenty at static input '0', but also has no effect on total power consumption at static input '1'. This inspiring result directly comes from the removal of the redundant leaps of precharging node Y by the control of transistor M25. In addition, the employment of IG-mode FinFET also saves the total number of transistors. An interesting phenomenon is that since the leakage current of the N-type transistor is usually smaller than that of the P-type transistor and the added transistor M25 will not influence the normal operating process at static input '1' (merely equals a connected switch), the power consumption of the optimized multimode FinFET flip-flop at static input '0' is nearly half of that at static input '1'. As for the other nodes of the optimized flip-flop, it is obvious that transistors M3, M14, and M20 will not be repetitively turned on because node Y remains at low voltage at static input '0', which definitely cuts down the leakage power dissipation of the pull-down paths containing these transistors. Thus, the measured power consumption of other nodes also significantly drops by about one-third.

Considering the timing performance, the setup time and hold time at the falling edge of input signal D are essentially unchanged. The only penalty of the optimized multimode FinFET flip-flop is that the setup time at the rising edge of input signal D increases by about three times compared with that of the LP-mode FinFET flip-flop. The reason for this degradation lies in that transistor M25 is controlled by the input signal D, and only if D jumps to high voltage will it be enabled to start charging node Y. Limited by this causality, the circuit takes more time to become prepared before switching to the evaluation stage. However, on the other hand, the hold time improves significantly in the worst case due to the same reason and offsets the above shortage in a certain degree. As for the clock-to-output delay, it also remains the same on account of the same evaluating structure. Hence, from an overall perspective, the timing performance of the optimized multimode flip-flop is acceptable.

Figure 7 shows the comparison of measured average power consumption between the LP-mode FinFET flip-flop and the optimized multimode FinFET flip-flop over the entire range of data switching activity. As is mentioned previously, the optimized flip-flop tremendously reduces the power consumption of node Y at static input '0', which results in a corresponding drop of more than 50% in total average power consumption at the low data activity ratio (specifically from 0% to 20%). With the ratio increasing to a high value, the improvement declines somewhat in magnitude since the input data switches faster and the ratio of static input '0' becomes smaller. Although the optimized multimode FinFET flip-flop

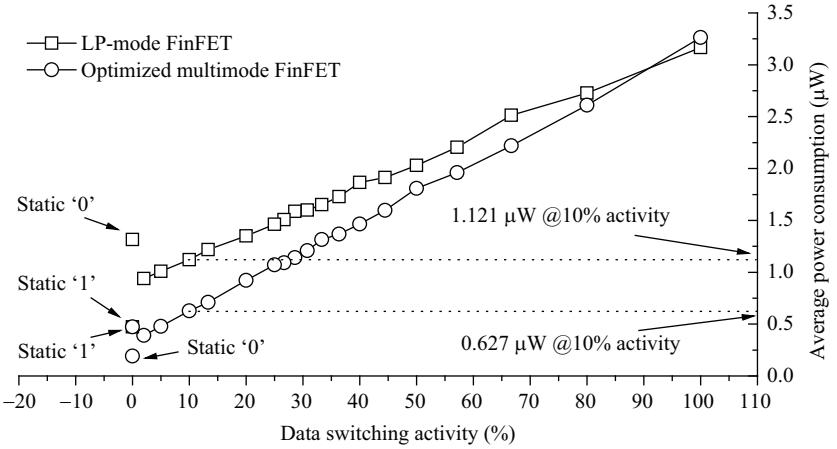

Figure 7 Comparison of average power consumption between the LP-mode FinFET flip-flop and optimized multimode FinFET flip-flop.

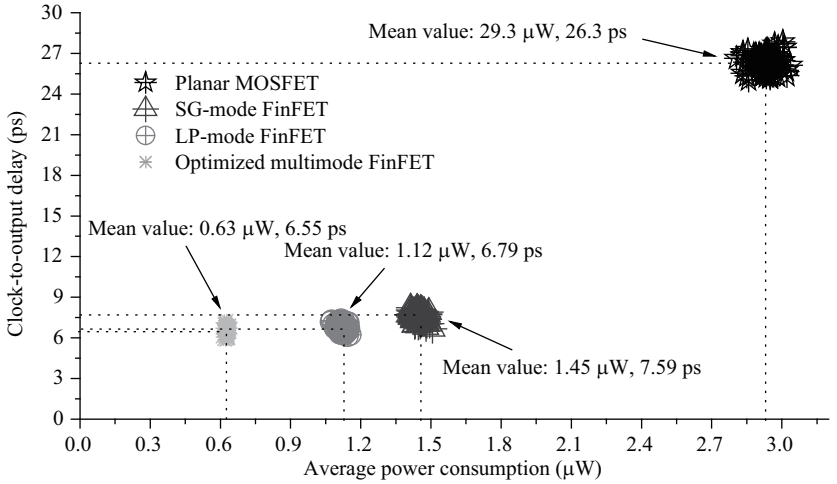

Figure 8 Monte Carlo simulation results at the typical 10% data switching activity.

has a slightly larger average power consumption at 100% data switching activity compared with that of the LP-mode FinFET flip-flop due to the short-circuit current which lasts a relatively longer time in transition processes, it is well-known that the normal data switching activity ratio of flip-flops in digital IC systems is approximately 5%–15%. Therefore, in normal cases, the optimized multimode FinFET flip-flop is definitely suitable for ultralow-power high-speed applications.

Figure 8 shows the Monte Carlo simulations based on the variation in transistor sizes. In order to study more realistic situations, the variation is modelled by a normal distribution with a standard deviation equal to 5% of the transistor width. All of the above four flip-flops are set to operate at typical 10% data switching activity and 100 simulation sweeps are conducted. The average power consumption and the clock-to-output (CtoQ) delay of the four flip-flops are measured and displayed in Figure 8 as x-coordinate and y-coordinate respectively. Therefore, the closer the point is to the lower left part of the plot, the better the performance of this design. From the simulation results, the mean value of the measured average power consumption and CtoQ delay are consistent with the aforementioned analysis, and the advantage of the optimized multimode FinFET flop-flop is obvious compared with the other three flip-flops. In addition, the simulation points of the optimized multimode FinFET flip-flop exhibit a more concentrated distribution than the other flip-flops, which results in less sensitivity to process variation and environment changes.

7 Conclusion

In this study, a novel flip-flop called the static contention-free single-phase-clocked flip-flop (S^2CFF) has been reconstructed by SG-mode FinFETs and LP-mode FinFETs, which achieve corresponding reductions of 56.7% and 61.8%, respectively, in measured average power consumption at the typical 10% data switching activity, as well as significant improvement in timing performance. In addition, to eliminate the extra energy loss introduced by the redundant leaps of node Y at static input '0', further optimization based on the IG-mode FinFET was implemented, and the simulation results show that the power consumption drops more than 50% on average at the low data switching activity ratio without obvious speed degradation.

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Conflict of interest The authors declare that they have no conflict of interest.

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