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Single event upset rate modeling for ultra-deep submicron complementary metal-oxide-semiconductor devices

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Abstract Based on the integral method of single event upset (SEU) rate and an improved charge collection model for ultra-deep submicron complementary metal-oxide-semiconductor (CMOS) devices, three methods of SEU rate calculation are verified and compared. The results show that the integral method and the figure of merit (FOM) methods are basically consistent at the ultra-deep submicron level. By proving the validity of the carrier collection model considering charge sharing, the applicability of two FOM methods is verified, and the trends of single-bit and multiple-bit upset rates for ultra-deep submicron CMOS are analyzed.

Keywords ultra-deep submicron, complementary metal-oxide-semiconductor devices, single event, upset rates, charge sharing

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1 Introduction

With the rapid development of aerospace and nuclear technology, the single event effects of advanced semiconductor devices in space and nuclear radiation environment have resulted in increased attention. Studies show that single event upset (SEU) becomes more serious for complementary metal-oxide-semiconductor (CMOS) devices with the technology node scaling in the radiation environment of high-energy particles (such as heavy ions, protons and neutrons) [1–3], which causes the random variation of the logic state or stored data, and even the permanent failure of the devices. Therefore, the research on SEU rates for ultra-deep submicron CMOS devices will provide a theoretical basis of radiation hardening for advanced devices, and will predict SEU rates for devices on-orbit.

The integral method [4] and figure of merit (FOM) [5] are commonly used in predicting SEU rates. In the integral method, the induced particle differential energy spectrum multiplied by SEU cross-section is integrated within the particle spectrum. The FOM method is a direct calculation of parts of devices parameters combined within the radiation environment [6]. The integral method has the advantage

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of being an intuitional and distinct physical concept, although its calculation is complicated. The FOM method is suitable for predicting SEU rates of large-scale devices that have not been verified for ultra-deep submicron devices. Simultaneously, with the decrease in device size and distance between the devices, some new effects will arise, such as the charge sharing effect [7], the bipolar amplification effect [8], and the decrease of critical charge in sensitive regions [9], which increase the probability of multiple-bit upset [10]. Therefore, it is necessary to establish a new model and verify the applicability of FOM methods for ultra-deep submicron technology.

First, the charge sharing effect is introduced and a charge collection model is improved for ultra-deep submicron technology. Second, on the basis of the integral method and the FOM method, a verification scheme of upset rates for ultra-deep submicron technology is proposed. Using the integral method as a standard, the validity of the charge collection model based on the charge sharing and the applicability of the two FOM methods for the ultra-deep submicron devices are verified. Finally, the trends of single-bit and multiple-bit upset rates for ultra-deep submicron technology are analyzed.

2 The charge collecting model based on the charge sharing for ultra-deep submicron technology

SEU usually occurs in large-scale storage arrays, such as SRAM and DRAM. When a charged particle hits a semiconductor material, the energy will be lost, so that electric charges will be generated in the particle's path. If a node of an electric circuit selects enough charges, it will upset. If an incident particle causes several storage units' upset, we call that multiple-bit upset (MBU).

In the past, the calculation of MBU rates was based on the situation where a particle's path passes through several sensitive units at once. This situation involves particle deposit energy in different units, so that MBU might be induced. However, other situations of carriers transport among different units are not included, so they could not be used to evaluate the MBU rate of ultra-deep submicron devices correctly. In ultra-deep submicron devices, sensitive nodes are closer to each other, and charge collection is no longer limited to a single transistor. An incident particle will induce charge collection in several devices. The increase of MBU in SRAM is mainly caused by the charge sharing effect, and diffusion is the principal mechanism of charge sharing.

The charge sharing effect is a type of radiation effect where the generated charges are collected by some sensitive nodes at the same time that an energetic particle strikes the device [7]. In a radiation environment, when the angle between the direction of incident particles and the normal vector of device surface is small, some of the electron-hole pairs generated in the device will be collected by adjacent regions through diffusion and the bipolar effect. In this work, adopting NMOSs at 130 nm technology node, a model is established where charge sharing is led by diffusion mechanism.

The traditional calculation of the SEU cross-section is based on the rectangular parallelepiped (RPP) model [11–13]. However, in this model, the concept of single sensitive volume could not accurately explain some new effects at the ultra-deep submicron scale, such as the charge sharing effect. In the concept of multi-volume that has emerged recently [14–17], the sensitive region that collects charges is a series of RPP geometric areas, which is conducive to modeling on multiple devices, and calculating the amount of collection charge at the same time. Therefore, the concept of multi-volume is introduced in the RPP model at the ultra-deep submicron scale. The charges induced by incident particle will be regarded as a series of punctated charges, whose position is expressed by its distance to the drain (as shown in Figure 1). Simultaneously, the concept of charge collection efficiency $\eta(\mathrm{r}_i)$ [18] is introduced in the model, which is determined by two exponential functions. It can be expressed as

$$\eta(r_i) = \exp\left(-\frac{r_i^{\mathrm{lat}}}{r_{\mathrm{lat}}}\right) \cdot \exp\left(-\frac{r_i^{\mathrm{depth}}}{r_{\mathrm{depth}}}\right), \tag{1}$$

where r_{lat} and r_{depth} are the horizontal and vertical diffusion coefficients, respectively, with charge-sharing effect. r_i^{lat} and r_i^{depth} are the horizontal and vertical distances of punctate charge to the drain, respectively.

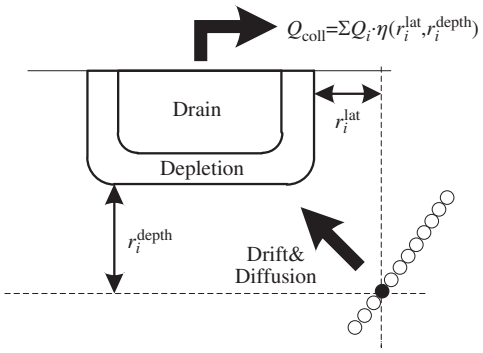

Figure 1 Punctate charge path and charge collection mechanism.

Due to the smaller size of devices at the ultra-deep submicron scale, the effective collection depth [19] should be taken into consideration, which means the charges generated deeper than the effective collection depth will not be taken into account. Studies show [7] that for 130 nm technology node, the effective collection depth of NMOS is about 0.9 μm, while that of PMOS is about 1.2 μm. The total amount of charge collection within the effective collection depth is

$$Q_{\text{coll}} = \sum Q_i \cdot \eta(r_i), \tag{2}$$

where $\eta(r_i)$ is the collection efficiency of punctate charges Q_i. Q_i depends on the linear energy transfer (LET) or energy of incident particles. Generally, LET = 96.608 MeV·cm^2/mg is equivalent to 1 pC/μm, which means Q_i= (LET/96.608) pC/μm. Therefore, the incident particles with different LET values striking into SRAM can be simulated by computer, based on the random sampling method. Since the drain area of off-state MOS is the sensitive area of charge collection, the amount of charge collection is calculated by using (1) and (2) based on the size of MOS sensitive area. The number of upsets can be determined by comparing the amount of charge collection with the critical charge, and the upset cross-section can be obtained by the number of upsets divided by total number of incident particles.

SRAM is composed of many equal units in total, with each unit having the same constructure, and the arrangement is symmetrical, hence the fundamental storage unit can be modeled by sensitive drain zone. The size of this zone can be measured by the surface area and the depth, which represents the depletion region. Every sensitive zone of a fundamental storage unit can also be characterized by sensitive volume. Every sensitive volume has a RPP structure, which means every storage unit has two RPP structures with the ability of charge collection. The device model of our research is shown in Figure 2. Figure 2(a) represents a particle striking a storage unit vertically, with the carriers being collected by two sensitive volumes through several transport mechanisms. Figure 2(b) represents the topology structure of multiple storage units in SRAM, and can reflect the concept of multiple sensitive volume and the carriers' transport mechanism. In Figure 2(b), black and white blocks represent the sensitive volumes of PMOS and NMOS, respectively.

3 Calculation method of SEU rate and verification scheme at the ultra-deep submicron scale

3.1 Calculation method of SEU rate at the ultra-deep submicron scale

The integral method [4,11] is generally used for calculating the rate of single event upset for devices. In recent years, FOM [5] has emerged as a simpler method. In the FOM method, a single parameter is used to characterize the single-particle sensitivity of the device, and to estimate the SEU rate on geosynchronous orbit. Its general expression is

$$R = C \times \text{FOM}, \tag{3}$$

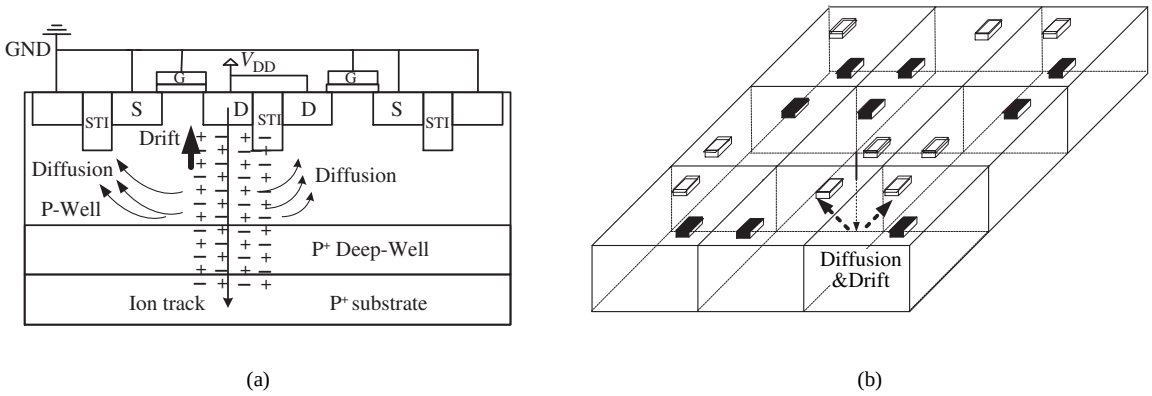

Figure 2 Adjacent NMOS charge sharing and collection model. (a) Cross-sectional view; (b) lateral view.

where R is SEU rate for the device, and C is the coefficient of SEU rates on-orbit, which has the same dimension with R (upset/(day·bit)). C is associated with the track, shielding, ion species (protons or heavy ions) and the type of device (hardened and unhardened). FOM is a dimensionless parameter, that characterizes the SEE sensitivity of the devices. The FOM expressions can be obtained either through the cross-sectional data (FOM_C) or through the device parameters (FOM_P).

In FOM_C, FOM can be calculated from the experimental data. For heavy ions and protons, FOM expressions are [20]

$$\mathrm{FOM} = \frac{\sigma_{\mathrm{HL}}}{L_{0.25}^2}\left(\frac{(\mathrm{MeV}\cdot\mathrm{cm}^2/\mathrm{mg})^2}{\mathrm{cm}^2}\right), \tag{4}$$

and

$$\mathrm{FOM} = 4.5\times10^4\times\sigma_{\mathrm{PL}}\left(\mathrm{cm}^2\right), \tag{5}$$

respectively, where σ_{HL} and σ_{PL} are the saturated cross-section of SEU induced by heavy ions and by protons, respectively. $L_{0.25}$ is the LET value corresponding to 25% of saturated cross-section.

Due to this, C in FOM_P and C in FOM_C have the same significance but are different in order of magnitude; C in FOM_P is represented by C', and FOM is obtained by the physical parameters of devices in FOM_P. If the sensitive area is assumed to be a RPP, whose surface dimensions are a, b, and depth is c, the FOM expression is

$$\mathrm{FOM} = \frac{a\times b\times c^2}{Q_c^2}\left(\frac{\mathrm{fC}^2}{\mu\mathrm{m}^4}\right), \tag{6}$$

where critical charge Q_c is defined as the minimum amount of charge induced SEU in a storage unit, and whose first-order approximation is expressed as

$$Q_c = C_N V_{\mathrm{DD}}, \tag{7}$$

where C_N is the equivalent capacitance of the node struck, and V_{DD} is the operating voltage.

When the experimental data is inadequate or unavailable and the device model data is available, Eqs. (6) and (7) can be used to estimate the SEU rate, which can assess the effects of devices variation on SEU rates rapidly. The FOM method is commonly used in the upset calculation at a large scale, which remains to be verified at the ultra-deep submicron scale.

3.2 Verification scheme of SEU rate at the ultra-deep submicron scale

In order to verify the validity of the improved model and the applicability of two FOM methods, the calculation of SEU rate based on the integration and two FOM methods are programmed, respectively. The flow charts of the programs are shown in Figure 3.

The form of Weibull function used to fit the data of SEU cross-section in the programs is

$$y = A\left\{1-\exp\left(-(k(x-x_c))^d\right)\right\}, \tag{8}$$

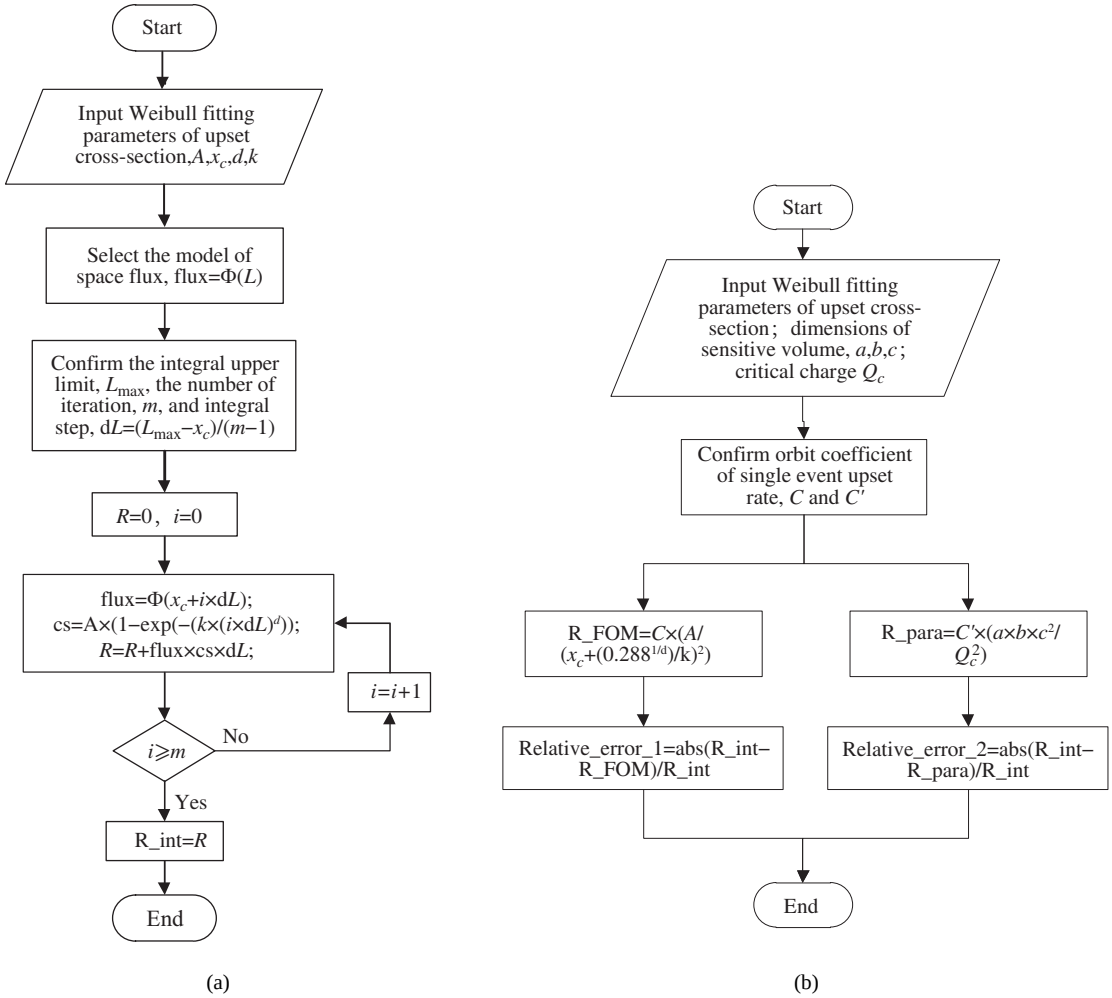

Figure 3 The flow charts of the programs of SEU rate calculation. (a) Arithmetic based on the integration; (b) arithmetic based on FOM.

where y is the cross-section of SEU $\sigma(L)$, A is the saturated cross-section $\sigma_{\rm sat}$, x_c is the threshold of LET, k and d are the size factor and the shape factor of the Weibull distribution, respectively.

The CMOS bulk silicon technology is used in SRAM model for 130 nm technology node without any radiation-hardened technology. The sensitive volume is 0.2 μm × 0.3 μm × 0.4 μm, and the critical charge is 2.5 fC in a 130 nm device model. Due to the lack of specific parameters for the 90 nm technology node, we use the experimental data in [21]. The sensitive volume is 0.15 μm × 0.25 μm × 0.25 μm, and the critical charge is 1.7 fC.

In the integral method, the Adams's "10% worst-case" model of galactic cosmic rays is used, whose expression of the LET spectrum is [22]

$$\Phi = 5.8 \times 10^2 L^{-3}, \tag{9}$$

where Φ is the differential flux of particles, and the unit is /((cm^2/day)·(MeV·cm^2/mg)). L is LET value of particles, and the unit is MeV·cm^2/mg. As in [6], the coefficients of SEU rates C and C' are 500 upsets/(day·bit) and 5×10^{-4}upsets/(day·bit), respectively, in FOM methods. The particles are assumed to have normal incidence, and the range of LET is 1–60 MeV·cm^2/mg.

Based on the above data, the amount of charge collection is calculation and compared to the critical charge, which can be determined whether upset or not. The cross-section can then be calculated based on the calculation scheme above, and SEU rate is calculated and compared.

Table 1 Cross-sectional data of the heavy ion induced SEU in 130 nm and 90 nm SRAM

LET	1.5	3.4	6.8	8.0	11.5	16.6	23.4	26.5	37.6	53.1	57.9
CS (130 nm)	1.20	3.72	19.4	30.1	51.4	74.7	103	110	138	174	160
LET	3.5	4.7	6.2	8.6	11.9	14.5	19.7	28.2	34.3	–	–
CS (90 nm)	2.43	3.99	5.26	8.05	11.4	14.0	17.5	22.2	24.3	–	–

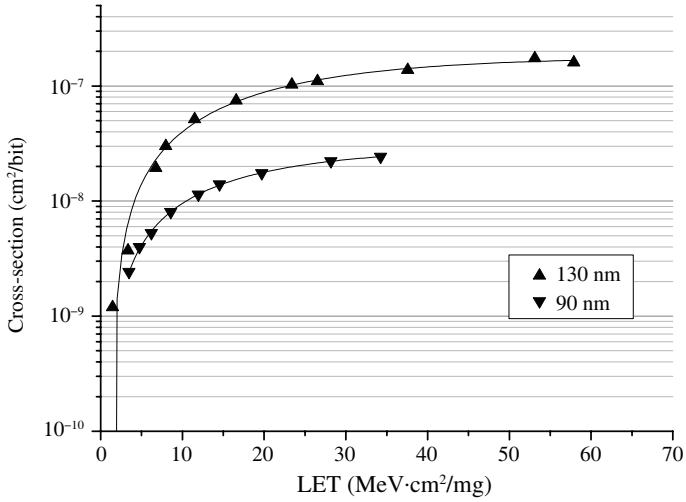

Figure 4 Cross-sections of SEU at 130 nm and 90 nm.

Table 2 The SEU rates of the devices of two different technology nodes

	R_int	R_FOM	relative_error_1	R_para	relative_error_2
130 nm	7.2291×10^{-7}	7.5470×10^{-7}	0.0440	7.6800×10^{-7}	0.0624
90 nm	2.5169×10^{-7}	2.3775×10^{-7}	0.0554	4.0549×10^{-7}	0.6111

4 Results and analysis of SEU rate calculation for ultra-deep submicron CMOS devices

4.1 Results of SEU rate calculation at 130 nm and 90 nm technology nodes

Based on the model and parameters above, the cross-section of SEU induced by heavy ions for 130 nm SRAM is obtained. Due to the lack of specific parameters for the 90 nm technology node, we use the experimental data in [21], as shown in Table 1. The LET is the effective LET value, i.e., L_{eff}, and the unit is MeV·cm^2/mg; CS is the equivalent cross-section, and the unit is 10^{-9}cm^2/bit. The two sets of data are fitted by Weibull function, respectively, as shown in Figure 4.

When the data of upset cross-section is obtained, the integral method of SEU rate calculation is still able to predict the SEU rate for ultra-deep submicron devices as a universal method [23]. Based on the parameters above, the SEU rates can be calculated by the integral method and the two FOM methods, respectively. Taking the integral method of SEU rate as a reference, the relative deviations of the two FOM methods can be calculated, as shown in Table 2, where R_int is the result of the integral method, R_FOM is the result of the FOM method based on cross-sectional data, R_para is the results of the FOM method based on the device parameters, the unit of SEU rates is upsets/(day·bit), relative_error_1 is the deviation of R_FOM with respect to R_int, and relative_error_2 is the deviation of R_para with respect to R_int (these also hold for Table 5 below).

The data in Table 2 are obtained from a single storage unit, and show that the SEU rate reduces slightly with a reduction in feature size, related to the change of device parameters. First, the feature size will affect the charge collection efficiency. With the reduction in feature size, the channel length and depletion region depth will reduce correspondingly. Since the effective charge collection length is

Table 3 The change of sensitive volume and critical charge with the decrease of feature size

Feature size (nm)	Critical charge (fC)	Sensitive volume (μm^3)
250	8	$0.5 \times 0.7 \times 1$
180	5	$0.35 \times 0.5 \times 0.7$
130	2.5	$0.2 \times 0.3 \times 0.4$
90	1.7	$0.15 \times 0.25 \times 0.25$

proportional to the depletion region depth, it follows:

$$L_c = \left(1 + \frac{\mu_{\rm n}}{\mu_p}\right) X_d / \cos\theta, \tag{10}$$

where μ_n is the electronic mobility, μ_p is the hole mobility, θ is the angle of incidence, L_c is the effective charge collection length, hence, charge collection efficiency Q_s will reduce correspondingly.

Second, the decrease of feature size will also reduce the critical charge. The critical charge Q_c can be determined by junction capacitance and surface area S of the space charge region:

$$Q_c = \left[2\varepsilon_s\varepsilon_0 q \left(\frac{N_D N_A}{N_D + N_A}\right)\left(\frac{K_B T}{q}\ln\frac{N_D N_A}{n_i^2} + V_R\right)\right]^{1/2} S, \tag{11}$$

where ε_0 is the vacuum permittivity, ε_s is the relative dielectric constant of semiconductor material, q is the electron charge, N_A is the acceptor impurity concentration, N_D is the donor impurity concentration, V_R is the reversed bias, n_i is the intrinsic carrier concentration, K_B is the Boltzmann constant, and T is temperature. It can be seen that Q_c is mainly decided by drain bias, function capacitance of reverse-biased pn junction, gate capacitance and parasitic capacitance, etc. Using first-order approximation, Q_c can be expressed as (7), the decrease of feature size will cause the reduce of equivalent capacitance C_N and operating voltage $V_{\rm DD}$, so the critical charge Q_c will also reduce.

For a single CMOS SRAM unit, based on the soft error rate model proposed by Hazucha and Svensson [24]:

$$\mathrm{SER} \propto A \times \exp\left(-\frac{Q_c}{Q_s}\right), \tag{12}$$

where A is the surface area of the sensitive volume, and the SEU rate relates to the ratio of $-Q_c/Q_s$ and the sensitive volume. When the ratio is significant, it leads to a change of SER; however, if Q_c is close to Q_s, the SEU rate almost lies on the sensitive volume.

Sensitive volume relates to the parameters from device structure and technique, such as junction depth, doping concentration and substrate characteristics. Our research adopts the RPP model, in which a sensitive volume is supposed to be a rectangular parallelepiped, the surface area of this volume is $a \times b$, and the depth is c, as described in (6). Through this model, the sensitive volume and critical charge changes caused by the decrease of feature size can be obtained, as shown in Table 3. It can be seen that with the decrease of feature size, the size of sensitive volume will reduce.

Based on the discussion above, for single storage unit, a decrease of feature size will lead to a reduction in the SEU rate. For a chip, although the SEU rate of a single storage unit decreases, the growth rate of the integration level is more significant, so the SEU rate of the chip increases.

4.2 Results of multiple-bit upset for 130 nm devices

Simultaneously, the cross-section of multiple-bit upset induced by charge sharing at 130 nm technology node is calculated and compared with the data of single-bit upset, as shown in Table 4.

Based on the integral method and the FOM_C method, the rates of single-bit upset and multiple-bit upset are calculated at the 130 nm technology node, respectively, accompanied by the model of space radiation environment flux. The relative deviations are also calculated, as shown in Table 5. Figure 5 shows the trends of upset rates of two methods as the number of upset bits increases.

Table 4 The cross-sectional data of SEU and MBU for 130 nm SRAM

LET (MeV·cm^2/mg)	Cross-section (cm^2/bit)				
	SBU	2-bit	3-bit	4-bit	MBU
1.5	1.20×10^{-9}	–	–	–	–
3.4	2.50×10^{-9}	3.72×10^{-10}	1.12×10^{-10}	–	4.84×10^{-10}
6.8	1.30×10^{-8}	1.94×10^{-9}	5.82×10^{-10}	1.45×10^{-10}	2.67×10^{-9}
8.0	2.02×10^{-8}	3.01×10^{-9}	9.03×10^{-10}	2.26×10^{-10}	4.14×10^{-9}
11.5	3.44×10^{-8}	5.14×10^{-9}	1.54×10^{-9}	3.85×10^{-10}	7.07×10^{-9}
16.6	5.00×10^{-8}	7.47×10^{-9}	2.24×10^{-9}	5.60×10^{-10}	1.03×10^{-8}
23.4	6.90×10^{-8}	1.03×10^{-8}	3.09×10^{-9}	7.72×10^{-10}	1.42×10^{-8}
26.5	7.37×10^{-8}	1.10×10^{-8}	3.30×10^{-9}	8.25×10^{-10}	1.51×10^{-8}
37.6	9.25×10^{-8}	1.38×10^{-8}	4.14×10^{-9}	1.04×10^{-9}	1.90×10^{-8}
53.1	1.17×10^{-7}	1.74×10^{-8}	5.22×10^{-9}	1.31×10^{-9}	2.39×10^{-8}
57.9	1.07×10^{-7}	1.60×10^{-8}	4.80×10^{-9}	1.20×10^{-9}	2.20×10^{-8}

Table 5 Rates of SEU and MBU for 130 nm SRAM

	SEU	SBU	MBU	2-bit	3-bit	4-bit
R_int	7.2291×10^{-7}	4.8050×10^{-7}	7.0239×10^{-8}	5.1361×10^{-8}	1.5424×10^{-8}	3.1957×10^{-9}
R_FOM	7.5470×10^{-7}	5.0347×10^{-7}	1.0609×10^{-7}	7.6685×10^{-8}	2.2997×10^{-8}	5.7247×10^{-9}
relative_error_1	0.0440	0.0478	0.5105	0.4931	0.4910	0.7914

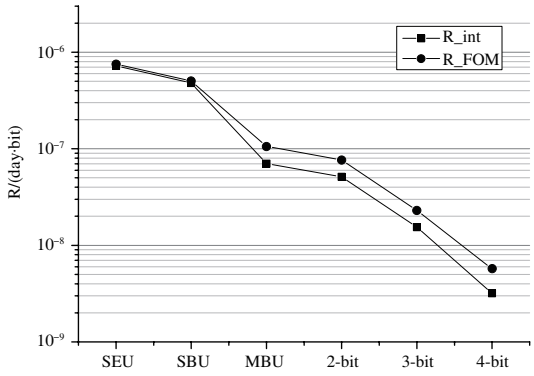

Figure 5 Trends of SEU and MBU rates at 130 nm technology node.

4.3 Discussion about the single event upset at ultra-deep submicron

4.3.1 *Discussion about the charge-sharing model based on diffusion*

The cross-sectional data in Table 1 demonstrates the same trend with the results in [21,25,26], and their absolute error is less than an order of magnitude. The fitted data in Figure 4 show that the cross-section at 130 nm is greater than the cross-section at 90 nm at the same LET, which also has the same trend in [21,25,26]. Therefore, to some extent the validity of the improved model is verified at the ultra-deep submicron scale.

One feature of this model is the consideration of multiple-bit upset induced by charge sharing. As analyzed above, the main mechanism of multiple-bit upset in an ultra-deep submicron device is not particle path cross-through for several sensitive nodes simultaneously, but is the charge sharing among adjacent devices.

If the incident positions are diverse, multiple-bit upset caused by charge sharing is not the same either. When the incident point is on the sensitive volume, the main mechanisms of charge sharing are diffusion and drift assisted by funnel. When the incident point is between sensitive volumes, the mechanism is diffusion only. Based on available research, when a particle strikes between sensitive volumes, bits of

multiple-bit upset are much more than directly striking on sensitive volume. If the strike is on the sensitive volume, the diffusion charges will reduce, and many more charges will be collected by funnel-assisted drift, so only the two nearest nodes will upset. If the strike happens near the sensitive node, the transverse diffusion will cause more multiple-bit upsets, such as 3-bit upset or 4-bit upset. Figure 5 is the simulation result of upset rate, and models the situation of where strikes occur among sensitive nodes, so there is some certainty there will be 3-bit or 4-bit upset.

After a particle strikes into a device, there are some charge transport and sharing processes: (1) Due to the bias voltage on drain, electrons and holes generated by strike will drift under an electric field. (2) Due to the concentration gradient, electrons and holes will diffuse. On the one hand, diffused charge will be collected by drain and other adjacent nodes, and cause a charge sharing effect. On the other hand, diffused charge will disturb the well potential: for NMOS, most electrons and holes are collected by drain and well respectively, and a small part of holes diffused will lead to a little rise of p-well potential; for PMOS, a large number of holes and electrons are collected by drain and n-well, respectively. As n-well has a high voltage, the diffusion of electrons will induce a loss of n-well potential. (3) The disturbance of well potential will lead to the parasitic transistor being open, will increase the collected charge of the struck device, at the same time, it will prompt the lateral parasitic transistor being open between adjacent devices, resulting in a bipolar amplification effect. Normally, the charges generated from this effect cannot be shared, as it can only increase the charge collect for struck devices.

In the analysis above, the main reason for charge sharing is the diffusion between substrate and well. For advanced technology, the distance between devices is becoming increasingly short, so charges will diffuse from struck node to other nodes, and the quantity of diffused charge becomes very significant. Hence, compared to large-scale devices, our model deduces a higher multiple-bit upset rate.

While there are still some errors between the calculation results and the results of simulation or experiment, these could be explained by the following reasons. First, the actual shape of the sensitive volume is very complicated, and related to the specific technology process. Although the RPP model is improved, it is still a simplified model and cannot completely replace the actual device. Second, the main mechanisms of charge sharing in NMOS and PMOS are diffusion and bipolar amplification effect, respectively. Our model is based on NMOS, which leads inevitably to some deviations from the calculated cross-section.

4.3.2 *Comparative analysis of two FOM methods and the integral method*

In Table 2, the results of two FOM methods and the integral method are basically the same for the SEU rate at ultra-deep submicron scale. The total SEU rate of FOM_C method and that of integral method are almost identical, the relative deviation between them being less than 5%. Although the total SEU rate of the FOM_P method has larger deviation with respect to that of integral method, both have the same trend, and their absolute deviation is less than an order of magnitude. In Table 5, the rate of multiple-bit upset of the FOM_C method is slightly larger than that of integral method at the 130 nm technology node. While the relative deviation is about 50%, their trends are almost the same, and absolute deviation between them is less than an order of magnitude. All this indicates the applicability of two FOM methods at ultra-deep submicron scale, which can assess the sensitivity of a CMOS device to a single particle.

One reason for the result of the FOM method being larger than that of the integral method is the sensitive volume; the critical charge in FOM_P are the classic values at different technology nodes, but not the actual value of the specific device. Another reason is the sensitive volume of NMOS is slightly larger than that of PMOS for SRAM. Our model is based on the NMOS, which leads inevitably to a larger result.

4.3.3 *Analysis of the rate of multiple-bit upset at the ultra-deep submicron scale*

In Table 4, the cross-section of single-bit upset is the major part of total cross-section at the 130 nm technology node. In multiple-bit upset, 2-bit upset is the major part and the cross-sections of multiple-bit

upset decrease rapidly with an increase in upset bits. Table 5 and Figure 5 show the same trend of the SEU rate with the distribution in [16]. In single-bit upset, the rate of single-bit upset is the major part of total upset rate. In multiple-bit upset, the MBU rate decreases rapidly with an increase in the number of upset bits, which leads to a decrease in the total upset rate. The conclusions above can be explained by the efficiency of charge collection of (1). When one ion strikes into a device, the sensitive nodes closer to the path of charges collect more charges and the further sensitive nodes collect fewer charges, which leads to a smaller probability that some adjacent nodes collect enough charges to upset at the same time. The more bits upset at the same time, the more energy they need. When the energy of particles is not too high, the probability of multiple-bit upset is small, and the rate of single-bit upset is the major part.

In Table 5, the rate of multiple-bit upset is 9.72% of the total upset rate. As the feature size of devices continues to be reduced, the probability of multiple-bit upset is getting increasingly greater, which cannot be simply ignored. This is mainly caused by the following reasons. First, as feature sizes decrease, the size of sensitive volume is also decreasing, which leads to a decrease in the critical charge. Therefore, it will cause more sensitive nodes upset when the collect charge is more than the critical charge. Second, with an increase in degree of integration, the distance between the devices decreases gradually and the efficiency of charge collection increases, which leads to more multiple-bit upset. Finally, some new effects emerge as feature size decreases, such as the bipolar amplification effect, which will result in an increase in charge collected by adjacent devices, and in the percentage of multiple-bit upset.

5 Discussion and conclusion

The improved model based on the collecting efficiency of charge diffusion has some validity at the ultra-deep submicron scale. It is suitable for the calculation of SEU cross-section of CMOS, as well as the SEU rate with the integral method.

Two FOM methods that calculate the SEU rates are both suitable for ultra-deep submicron technology. The FOM method based on cross-sectional data needs neither the parameters of device structure, nor a large number of experimental data. It is necessary to obtain the saturated cross-section and upset threshold to predict the SEU rates for the devices on-orbit. This method is simple, practical, and its accuracy is no less than for the universal integral method. The FOM method based on the device parameters is suitable for the prediction of SEU rates by using the characteristics of the device itself directly, but needs to obtain the accurate values of device sensitive volume, which increases the difficulty of application and limits the scope of this method. However, it is still an effective way of making a rough prediction of SEU rates for the devices on-orbit.

In multiple-bit upset, 2-bit is the main part at the ultra-deep submicron scale. The rate of multiple-bit upset decreases rapidly as the number of upset bits increases. Although single-bit upset is the main part of total upset, the percentage of MBU rates is about 10% at the 130 nm technology node. Therefore, for the smaller sizes of device, the MBU should not be ignored.

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