SCIENCE CHINA
Information Sciences

• REVIEW •

January 2016, Vol. 59 012101:1–012101:8
doi: 10.1007/s11432-015-5431-6

An introduction to CPU and DSP design in China

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Received June 26, 2015; accepted August 10, 2015; published online October 29, 2015

Abstract In recent years, China has witnessed considerable achievements in the production of domestically-designed CPUs and DSPs. Owing to fifteen years of hard work that began in 2001, significant progress has been made in Chinese domestic CPUs and DSPs, primarily represented by Loongson and ShenWei processors. Furthermore parts of the CPU design techniques are comparable to the world's most advanced designs. A special issue published in *Scientia Sinica Informationis* in April 2015, is dedicated to exhibiting the technical advancements in Chinese domestically-designed CPUs and DSPs. The content in this issue describes the design and optimization of high performance processors and the key technologies in processor development; these include high-performance micro-architecture design, many-core and multi-core design, radiation hardening design, high-performance physical design, complex chip verification, and binary translation technology. We hope that the articles we collected will promote understanding of CPU/DSP progress in China. Moreover, we believe that the future of Chinese domestic CPU/DSP processors is quite promising.

Keywords Chinese domestic CPUs and DSPs, Loongson CPU, ShenWei CPU, YHFT DSP, BWDSP

Citation Hu W W, Zhang Y F, Fu J. An introduction to CPU and DSP design in China. Sci China Inf Sci, 2016, 59(1): 012101, doi: 10.1007/s11432-015-5431-6

1 Introduction

Integrated circuits play a crucial role in the information industry. Microprocessors, including CPUs and DSPs, are the core components of integrated circuits, and the progress of the domestic processor industry is an important criterion for evaluating a nation's strength and innovation capability in science and technology.

The development of Chinese domestic CPUs and DSPs began with the 10th Five-Year Plan (2001–2005); these development efforts were mainly supported by National High Technology Research and Development Program (863 Program) of China. After five years of effort, several domestically-designed CPUs and DSPs were developed successfully. The resulting CPUs included the Loongson (also called Godson) processors [1] developed by the Institute of Computing Technology, CAS, the ShenWei processors [2] developed by the National High Performance IC (Shanghai) Design Center, and the YHFT processors [3] designed by National University of Defense Technology.

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During the 11th Five-Year Plan (2006–2010), the Chinese government initiated the HGJ (core electronic devices, high-end generic chips and basic software) project, a major national science and technology effort that focused on core electronic devices, high-end general-purpose chips, and basic software products. The project's purpose was to further optimize the performance of the aforementioned CPUs and DSPs, and to promote their transformation into marketable products. As a result, multi-core CPUs and DSPs were designed and subsequently introduced into the market. During this period, CPU companies such as Loongson Technology Corporation Limited were founded.

During the 12th Five-Year Plan (2011–2015), the HGJ project aimed to promote the application of Chinese domestic CPUs and DSPs. A preliminary eco-system of domestic hardware and software was organized, which is widely utilized in several fields including industrial control, e-government, and weapons systems. For example, in April 2015, it was reported that radiation hardened Loongson CPUs were used in the new-generation BeiDou manmade satellite.

Recently, China has faced increasing challenges in network security and information security. Without the self-reliant design and fabrication of processors, the national security of China would be diminished. In the future, the Chinese government will further increase its investment in the development and deployment of domestic CPUs. Currently, Chinese domestic CPUs and DSPs show a promising momentum of development. We expect that by the end of 2020, Chinese domestic CPUs and DSPs will be able to completely fulfill the requirements of most security-critical fields in China, including (but not limited to) national defense, e-government, energy, communication, transportation, and financial affairs.

Owing to the rapid development of domestic CPUs and DSPs, *Scientia Sinica Informationis* (in Chinese) produced a special issue to describe the current progress of CPU and DSP design in China [4–13]. This special issue details the cutting-edge research and development of Chinese domestic CPUs and DSPs, including high-performance micro-architecture design, multi-core and many-core design, radiation hardening design, high-performance physical design, complex chip verification, and binary translation technology. Although these designs may still lag behind the most advanced designs by Intel and IBM, parts of Chinese CPU design techniques are comparable to the world's most advanced designs.

The special issue includes nine papers related to CPUs/DSPs. These nine papers fall into two categories. The first category involves the design and optimization of high performance processor products, including the Loongson CPU, ShenWei CPU, YHFT DSP, and BWDSP. The second category highlights some key technologies in processor development, such as binary translation, verification technology, and clock mesh technology in physical design.

It should be emphasized that all work introduced in this special issue is based on domestically designed CPU and DSP cores. Introduction of domestically designed SoCs based on licensed CPU or DSP cores is not included in the issue's content. More than one billion domestically designed SoC chips (primarily based on ARM CPU cores) are sold every year.

2 Design and optimization of high performance processors

The following six papers introduce the designs of the Loongson CPU, Loongson anti-radiation CPU, ShenWei multi-core CPU, ShenWei many-core CPU, YHFT DSP, and BWDSP100.

2.1 Design of Loongson GS464E processor architecture

The paper titled "Design of Loongson GS464E processor architecture" presents the Loongson GS464E CPU core which is the latest processor microarchitecture introduced by Loongson Technology.

In the past few years, all Loongson high performance processors [14–16] were built with the four-issue, 64-bit Loongson GS464 CPU core that originated from the design of Loongson 2F processors [17]. However, performance issues with the Loongson GS464 CPU core were gradually exposed with the wide use of Loongson processors. To improve the performance of Loongson processors, researchers and engineers at Loongson Technology have been dedicated to the development of the Loongson GS464E CPU core since 2012. Compared with the previous GS464 micro architecture, GS464E uses larger queues to improve

Table 1 Key parameters of GS464E CPU core

	SandyBridge	Bulldozer	GS464E
Reorder Buffer	168	128	128
Integer register file	160	96	128
FP register file	144	160 shared by 2 cores	128
L1 Inst. Cache	32 kB, 8-way (per core)	64 kB, 2-way (shared by 2 cores)	64 kB, 4-way (per core)
L1 Data Cache	32 kB, 8-way (per core)	16 kB, 4-way (per core)	64 kB, 4-way (per core)
L2 Cache	256 kB 8-way (per core)	2 MB 16-way (shared by 2 cores)	256 kB 16-way (per core)

pipeline efficiency, more memory access units, larger caches and TLBs to improve the memory subsystem performance, and a more complex branch prediction algorithm to improve branch prediction accuracy. In addition, the micro architecture was fine tuned with benchmarks at the RTL level to reduce pipeline stalls, and dozens of optimizations were made at the RTL level.

Two important features stand out from the various characteristics of the Loongson GS464E micro architecture. First, the performance of single thread programs is significantly improved. According to the performance evaluation results at the RTL simulation level, the GS464E greatly improves the branch predication performance (with the microbench benchmark), memory subsystem performance (with memcpy system call and Stream benchmarks), and pipeline efficiency (with dhrystone and coremark benchmarks) compared with its predecessor, the GS464. Second, an enhanced instruction set architecture called LoongISA is implemented on the GS464E. LoongISA extends MIPS64 with virtualization and features that accelerate the binary translation from X86 and ARM binary codes to LoongISA binary code.

Table 1 shows the key parameters of the GS464E CPU core. As a comparison, parameters for Intel SandyBridge and AMD Bulldozer are also listed. As the data shown in the table, after 2010, the micro architecture of GS464E has been comparable to CPUs by AMD and Intel.

Based on the Loongson GS464E architecture, the 4-core Loongson 3A1500/3A2000 processor (3A1500 is for embedded application, 3A2000 is for PCs and servers) was designed and fabricated based on a low power 40 nm CMOS technology. The Loongson 3A1500/3A2000 processor, which runs at speeds of 800 MHz–1 GHz, was fabricated and packaged when the special issue was published. According to performance test results provided by Loongson Technology, the SPEC CPU2006 ratio is approximately 7 per GHz using GCC as the compiler. Thus, it provides a three-fold performance improvement compared to its predecessor, the Loongson 3A1000. Its SPEC CPU2006 ratio per GHz is close to that of AMD's latest CPU [6].

2.2 Loongson X-CPU radiation hardening by design

The paper titled "Loongson X-CPU radiation hardening by design" introduces the design of a radiation hardened processor for space applications.

Radiation hardening can be achieved by adjusting the manufacturing process; however, this approach is prohibitively expensive. Radiation hardening by design (RHBD) [18,19] is the most widely used radiation hardening method that does not require adjustments to the manufacturing process. The authors discuss the RDHB method from multiple aspects, including circular-shape gate layout, guard-ring protect, time and space triple modular redundancy, dual interlocked storage cells, and error detection and correction coding, and apply all of them to the anti-radiation design of Loongson X-CPU.

The Loongson X-CPU is a highly integrated, high-performance SoC based on the dual-issue, 32-bit Loongson GS232 CPU core. It was fabricated with 180 nm CMOS technology. The chip operates at 100 MHz and contains a CPU core with separate instruction and data caches, an SDRAM/SRAM controller, a PCI controller, an SPI controller, an interrupt controller, two UARTs, an I2C and WDT interfaces. The chip was tested up to a total dose of 300 krad (Si), and it yielded an SEU error rate

better than 1.90362×10^{-5}/device/day. The results demonstrate that the chip can adapt to complex space environments and meet the demands of complicated applications.

On March 30, 2015, China launched a new-generation manmade satellite into space for its BeiDou global navigation and positioning network. In this satellite, Loongson X-CPUs are used to perform tasks such as controlling, communication and data processing.

2.3 ShenWei-1600: a high-performance multi-core microprocessor

The paper titled "ShenWei-1600: A high-performance multi-core microprocessor" presents the ShenWei-1600, the first domestically designed sixteen-core general-purpose microprocessor.

The ShenWei-1600 processor [2] was developed on a self-defined 64-bit RISC instruction set architecture. To improve the performance, multi-level parallelism is utilized, including data level, instruction level and thread level parallelism. In addition, a multi-hierarchy memory system was designed to accelerate memory access speed. The low-power design is employed in multiple levels, including the structure level, micro structure level, and circuit level. Thus, the ShenWei-1600 is characterized by its high-performance and low-power consumption.

The ShwnWei-1600 was fabricated using 65 nm CMOS technology. At 1.1 GHz, the peak performance was 140.8 GFLOPS, and the power consumption was less than 50 W. More than 8,700 ShenWei-1600 processors were used to build the Sunway BlueLight MPP which is one of the top 20 fastest supercomputers in the world.

2.4 A homegrown many-core processor architecture for high-performance computing

The paper titled "A homegrown many-core processor architecture for high-performance computing" introduces the architecture of a world-leading TFLOPS many-core processor for high performance computing.

Many-core processors [20–22] are widely used in high-performance computing. With the support of the national 863 program and national HGJ project, research and development in many-core processors have progressed significantly in China. This paper introduces a heterogeneous many-core architecture which consists of management processing elements (MPE), computing processing elements clusters (CPE cluster), memory controllers (MC) and system interfaces (SI). A group consists of an MPE, a CPE cluster with 64 CPEs, and an MC.

The key feature of the processor is the deep fusion of heterogeneous processor cores. To achieve this goal, the processor was designed to support different application features with a unified ISA architecture, a unified execution model, and a share-memory that supports cache coherence. Techniques for conquering "memory wall", "power wall", and "reliability wall" challenges are also illustrated. Experimental results show that the prototype chip can achieve a peak performance of more than 1 TFLOPS with 4 MPEs and 256 CPEs.

Although the paper does not provide details about the fabrication of the many-core CPU and its application in high performance computers, it can be expected that a TFLOPS many-core CPU is under design and a world-leading HPC will be built soon.

2.5 Coordinate multi-core DSP YHFT-QMBase: architecture and implementation

The paper titled "Coordinate multi-core DSP YHFT-QMBase: architecture and implementation" presents a multi-core DSP called YHFT-QMBase which is based on Vector-SIMD [23] architecture.

Vector-SIMD architecture has attracted considerable interest owing to its high performance in signal processing applications. At present, there is a major trend toward combining Vector-SIMD and multi-core technology in the architecture design of high performance DSPs.

The Vector-SIMD architecture usually consists of a scalar unit (SU) and a SIMD unit (SIMDU). The SU is mainly responsible for flow control and scalar calculation, while the SIMDU, which contains several parallel lanes is used to further accelerate the calculation speed. To develop high-performance DSPs, Vector-SIMD and multi-core technology such as the well-known AnySP [24] and BBE-128 [25] processors are combined. However, the performance of current Vector-SIMD architectures is still restricted by the

inefficiency of the hardware unit coordination. To address this issue, the authors propose approaches to improve the correlation of traditional multi-core Vector-SIMD architectures. These approaches considered the following four aspects: (1) the cooperation between scalar and SIMD units is redefined by a dynamic coupling execution scheme, (2) the communication among SIMD lanes is enhanced by a matrix-style communication, (3) data sharing among vector memory banks is accomplished by an unaligned vector memory accessing scheme, and (4) the background coarse-grain data transfer among cores is supported by a Qlink-Crossbar scheme. With these optimizations, experimental results show that YHFT-QMBase can achieve an average performance gain of 58.5%, compared with traditional Vector-SIMD architectures.

The YHFT-QMBase DSP was fabricated with 65 nm CMOS technology. When running at 500 MHz, YHFT-QMBase can achieve a peak performance of 32 GFMACS for single-precision float-point multiply-accumulation, and 128 GMACS for fixed-point (16 bits) multiply-accumulation. The typical power consumption for YHFT-QMBase is 8.65 W. For typical DSP applications, the number of cycles required to execute the application in YHFT-QMBase is 4.3 to 17.4 times lower than that of the TI C6000.

2.6 BWDSP100 and its applications

The paper titled "BWDSP100 and its applications" introduces the basic design of a universal DSP chip named BWDSP100, which was developed in the No.38 Research Institute of China Electronics Technology Group Corporation (CETC-38).

DSPs [26–28] are widely used in areas such as radar, electronic countermeasure systems, image processing, and audio/video systems. Through six years of hard work, researchers and engineers in CETC-38 have successfully completed the research and development for BWDSP100. The BWDSP100 is based on VLIW-SIMD [23] architecture. It includes 32 ALUs, 16 multipliers, eight shifters, and four transcendental function units. These 60 calculation units can perform four Radix-4 FFT iterations in one cycle. The 512-bit VLIW instruction can issue as many as sixteen 32-bit operations within one cycle.

The BWDSP100 was fabricated with a 55 nm CMOS technology and ran at a speed of 300 MHz. Its peak performance is 4.8 GFMAC / 19.2 GMAC (16 bits). In addition, a tool kit called ECS 1.0 was developed by CETC-38 for the BWDSP100. A hardware system that includes 30 four-way BWDSP100 boards is also introduced in the paper. The paper implies that this 120-chip system is used in some large scale applications. The paper also reveals that the second generation BWDSP based on 28 nm technology is under design.

3 Key technologies in processor development

The following three papers introduce key technologies in CPU development, including the fusion of different instruction sets through binary translation, verification technology, and clock mesh technology in physical design.

3.1 LoongISA for compatibility with mainstream instruction set architecture

The paper titled "LoongISA for compatibility with mainstream instruction set architecture" presents key features of the Loongson instruction set architecture (LoongISA) introduced by Loongson Technology for the first time.

The software ecosystem of MIPS processors is not as mature as mainstream processors such as X86 processors. This has become the primary obstacle limiting the development of Loongson CPUs that implement the MIPS64 instruction set architecture. In order to push forward the development of Chinese domestic CPUs, Loongson Technology has been dedicated to solving this problem for years. The Loongson Instruction Set Architecture (LoongISA) is one of the landmark achievements of these research efforts.

Binary translation technology [29–31] is one of the most promising methods for achieving compatibility with different architectures such as X86 and ARM. However, because of the differences between X86/ARM and MIPS, the efficiency of binary translation is normally very low. For example, X86's branch

instructions test the EFLAG field to determine branch direction, while MIPS's branch instructions directly compare GPR (General Purpose Register) values to determine branch direction. Simulating the 6-bit EFLAG in MIPS requires more than 50 instructions to execute each X86 calculation instruction that modifies EFLAG. In another example, 5-10 MIPS instructions are required to translate a MIPS virtual address to an X86 physical address for each load and store instruction, owing to the different TLB structures of X86 and MIPS.

LoongISA extends the MIPS instruction set architecture for compatibility with X86 and ARM mainstream instruction set architectures. New instructions, runtime environments, and system states are added to MIPS through the MIPS UDI (User Defined Interface) to accelerate the binary translation of X86 and ARM binary codes to LoongISA binary code. In addition, binary translation systems have been built based on LoongISA to run MS-Windows and its applications, X86 Linux applications, and ARM Android applications. LoongISA has been implemented in the Loongson 3A1500/3A2000, which is the newest four-core CPU product by Loongson Technology. Performance evaluation shows that with hardware support, the binary translation system of LoongISA can achieve very high efficiency. In this paper, it is shown that booting an X86 Linux kernel through the QEMU binary translation system in the Loongson 3A1500/3A2000 is 20 times faster than performing a similar booting procedure with the Loongson 3A1000, which does not support binary translation in hardware.

3.2 Hierarchical and reusable simulation environment for high-performance processor verification

The paper titled "Hierarchical and reusable simulation environment for high-performance processor verification" describes the verification methodology of ShenWei series processors.

Multi-core and SoC integration have become prevalent trends in high-performance processor development; this has made processor design more complex and chip scale even larger. Flat simulation verification environments consume a significant amount of computer resources, which sharply decreases the speed of the simulation, and consequently leads to low simulation efficiency. However, simulation [32–34] is still the most widely used method of processor verification, and processor simulation environments are crucial to simulation efficiency. Based on the processor architecture and the rules for reuse of verification components [35], a hierarchical reusable simulation verification environment can significantly reduce the problems of excessive memory consumption, low simulation speed, and low simulation efficiency. This method can also shorten the establishing and debugging periods, reduce mistakes in the environment, and make the simulation environment more easily reusable for different processor verifications. In the paper, module level, single core level, and chip level simulation environments are built for a sixteen-core CPU.

Though not clearly stated, the author strongly implies that the verification methodology introduced in this paper is applied to the sixteen-core ShenWei-1600 processor introduced in the paper titled "ShenWei-1600: a high-performance multi-core microprocessor" in this special issue.

3.3 Design of a hierarchical clock distribution network with low clock skew and tolerance for process variations

The paper titled "Design of a hierarchical clock distribution network with low clock skew and tolerance for process variations" introduces a novel hierarchical clock distribution network [36,37] called HLGCDN (H-tree-driven local grid clock distribution network). The design aims to address challenges such as on chip variation (OCV) and timing sequence uncertainty caused by the very deep sub-micro process.

The clock distribution network is constructed with a mixed clock structure based on a global H-tree network and regional mesh network. Moreover, the regional mesh network, which is also known as a local mesh grid, is different from conventional global mesh networks. Experimental results show that the clock skew is within 10 ps and the impact of process variations on clock skew is within the ratio of 10%. Therefore, this clock distribution network has a negligible clock skew and a high tolerance for process

variations. This work can be used to further optimize the timing sequence of high-performance processor cores.

The authors imply that the clock-tree methodology introduced in this paper is used in a 1.55 GHz high performance processor, but the fabrication technology is not revealed.

4 Closing remarks

CPUs and DSPs introduced in this special issue represent the highest level of CPU and DSP design in China. Each author presents his or her invaluable experience and lessons learned in practice that could be useful to readers in their own work.

Again, all works introduced in this special issue are based on domestically designed CPU and DSP cores. Introduction of domestically designed SoCs based on licensed CPU or DSP IP is not included in the issue.

These CPUs and DSPs introduced in this special issue have been deployed in Chinese network security and information security, which aptly demonstrates the ambition of Chinese government in developing domestic software and hardware. We look forward to seeing more breakthroughs in the area of processor design and development. Furthermore, we believe that additional progress will be made on Chinese domestic CPU/DSP processors in the future.

Acknowledgements This special issue would not have been possible without the contributions of many people. We sincerely thank all the authors for submitting their work to this special issue. This work was supported by National HGJ Project (Grant Nos. 2009ZX01028-002-003, 2009ZX01029-001-003, 2010ZX01036-001-002, 2012ZX01029-001-002-002, 2014ZX01020201, 2014ZX01030101), National Natural Science Foundation of China (Grant Nos. 61221062, 61133004, 61173001, 61232009, 61222204, 61432016) and National High Technology Research and Development Program of China (863 Program) (Grant Nos. 2012AA010901, 2012AA011002, 2013AA014301).

Conflict of interest The authors declare that they have no conflict of interest.

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